Sundance-Leaders in DSP and FPGA Solutions!

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Complex algorithms find their home at Sundance

When the United States Navy's Advanced Technology Engineering Group needed to find a home for their ultra complex, ultra sophisticated electronic warfare algorithms, Sundance stepped up to the plate and provided a unique hybrid DSP-FPGA hardware and a model based design solution to program it.

Housed inside the Sundance DSP8080-AIMM (Altitude Interference Mitigation Module) system, the Navy's system architecture and algorithms are helping to improve the warfighter's surveillance of the battle space. The DSP8080-AIMM combats communication interferences from unwanted sources and provides pin point accuracy for remote ship, tank and aircraft operators in understanding the source of a signal.

Provided in a compact, lightweight and low cost configuration, the DSP8080-AIMM accommodates beam forming of a high quantity of digital drop receivers (> 100 channels) and can interface to a range of coherent tuners. The system is flexible enough to provide radio direction finding and geo-location by-product, and outperforms its nearest competition in price, performance, size and weight.

Key to making the DSP8080-AIMM a reality for the Navy was the decision to use PARS (Parallel Application from Rapid Simulation) design environment. PARS generated the entire target code including, DSP codes, FPGA codes and all of the inter-processor communication and synchronization codes from a Simulink model. The Navy's algorithms were implemented as either IP cores on FPGAs or optimized DSP code targeting the floating and fixed point DSPs.

The DSP8080 utilizes multiple high-performance DSPs from Texas Instruments, including the TMS320C6416, a fixed-point processor running at 1 GHz, and the TMS320C6713, a floating-point DSP. The system also utilizes several Virtex 4 SX55 Xilinx FPGAs with the processing elements mounted onto a range of integrated Sundance platforms including the SMT374 , SMT364 , SMT318-SX and SMT361Q .

Commenting on the work completed with the Navy and on the DSP8080, Jacob Alamat, marketing manager for high performance processors at Texas Instruments said, "***-we're proud to be part of this unique solution for the Navy.***" So are we!

Want to know secrets of DSP-FPGA design and build?

At Sundance we're proud of having led the development of DSP-FPGA systems for the past 20 years. During this time we've learnt a thing or two about how make these systems work, how to build them and how to design them, and we are now sharing this with the designers across the world through our YouTube channel.

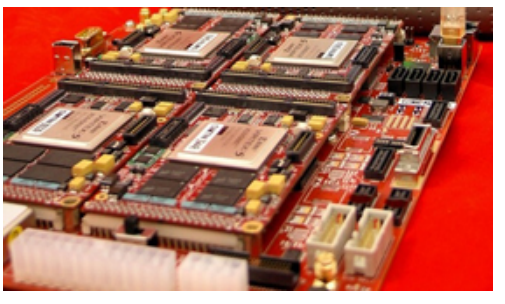
Simply go to YouTube and enter your favourite Sundance product name and you just may be lucky! To give you a head start, we've listed a few of our favourites below. Happy viewing.

- Let Stephen Malchi help you get to grips with PARS
- More PARS video tutorials
- See the guy's at 3L introduce you to multiprocessor design using Diamond
- Watch Kay Crail show you how to build an application using pre-built DSP and FPGA tasks

It's all about performance! Isn't it?

Well at Sundance we're not sure it is. In recent years there has been increasing interest in the role of FPGAs in the supercomputing mix. Yes they are a viable solution, but it's not just about performance. The SuperComputing computation mix is more complex. Power, performance (peak and sustained), communications latency, form factor, footprint, scalability, cooling BOM, energy efficiency, I/O, memory, clock rate, cost and ease-of-design, are some of the variables that are taxing the minds of high performance computing (HPC) designers.

It's with this in mind that we decided to design and build a solution that ticks these boxes for our HPC colleagues. RASS, our high reliability Reconfigurable, Accelerating, Scalable SuperComputing solution incorporates a lot of the know-how and features we have learned from over 2 decades of multiprocessor design.
At the heart of RASS are banks of tightly coupled Xilinx Virtex 5 FPGAs . Sitting on a carrier, the multiple FPGAs can be connected via a Rocket Serial Link (RSL) I/O interface and the architecture is adaptable to different applications and computation demands.



RASS integrates with industry standard processors and computing infrastructure. It features a modular, interchangeable array of high performance FPGAs and GPUs to deliver high performance, low latency and flexibility across single precision and double precision computation applications.

And to mitigate the learning curve and risk of reliance upon proprietary tools and languages, RASS is supported by industry standard design tools and languages. Design support from the The MathWorks , Xilinx, 3L , Impulse , HDL and C/C++ providers offers a readily available development environment. The maturity of this ecosystem enables immediate access to libraries of intellectual property including Navier-Stokes, Black-Scholes, LINPACK, Monte Carlo and Amber,

If you want to know more about RASS and see how it is "mixing" it up in the HPC community go to the RASS page or contact enquiries@sundance.com

Questions or comments?? Please email us at feedback@sundance.com.
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