SUNDANCE - The DSP & FPGA Development Force

eNews

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'Tokyo Drift?'

Tokyo Drift was a member of 'The Fast and The Furious' film franchise, that involved fast cars furiously racing round a street circuit (of Tokyo no less) with the high stakes being, death, honor or glory. Whilst we liked the film we just thought it wasn't fast and furious enough. Not having access to an array of high powered cars (we are working on that) or the streets of downtown Tokyo, we came up with our own 'circuit' solution the SMT702 that features 8 lanes of PXI express. On to this we placed FFT from Dillon Engineering to deliver a package that is seriously fast and furious.

By offering a FFT length up to 64M points, Dillon's core is quite simply streets ahead of the competition. Its IEEE-754 Floating-point FFT core sustains a rate up to 250Msps to deliver a 36 percent faster performance versus comparable cores. Area efficient, Dillon's FFT cores occupy fewer FPGA logic resources in terms of XtremeDSP slices and BRAMs than comparable off-the-shelf FFT cores.

Our circuit, the SMT702, is fitted with the fastest Xilinx Virtex-5 LX110T-3 FPGA that is optimized for high-performance logic with low-power serial connectivity. The FPGA is supported by 2 banks of 64-bit 512Mb DDR2 SDRAM and dual 3GHz ADC that can be combined to deliver 6 Gsps. 8-lanes of PXI Express deliver 16Gb/s of effective bandwidth per direction...and the module can plug in to any PXI Express peripheral slot or any PXI Express hybrid slot.

And as a navigation aid, we threw out the Sat Nav and put in place design support from the 3L Diamond multiprocessor tool suite and a bit-accurate and MATLAB compatible C/C++ model, testbench, datasets and data generators.

If you want to test drive our extreme FPGA FFT processing solution contact your local Sundance sales office or email us at enquiries@sundance.com. It's unbelievably fast and furious, but easy to handle.

PARS Scoops IET Software Design Award

We are absolutely delighted that the Institution of Engineering and Technology (the IET) has recognized the outstanding contribution that PARS has made to multiprocessor design, by naming it winner of the prestigious Software in Design category at the IET's 2008 Innovation Awards.

PARS (Parallel Application from Rapid Simulation) beat off stiff competition from the likes of BAE Systems to claim the winning ticket, and the award is testament to our focus and effort in delivering outstanding DSP+FPGA multiprocessor design solutions. Put simply, PARS enables application designers to generate system target code, including DSP codes, FPGA codes and all of the required inter-processor communication and synchronization codes from a Simulink model. Created as a value-add companion to The MathWorks model-based design flow, PARS boasts multiple design wins and also supports The Mathworks RTW-EC and HDLCoder.

1. PARS accepts a Simulink model as input, and helps users partition the Simulink model into several tasks that will be placed on different DSPs, GPPs and/or FPGAs. PARS helps users calculate the size and type of all data transfers between different tasks and then generates the C source code with all necessary inter-task/ inter-processor communication functions.
2. PARS then compiles, links and configures the tasks to build a single application file that can be downloaded into the parallel processing network. All the booting and task placement information is built into the application file together with all bit streams for the FPGAs in the system.
3. PARS also checks the Simulink model for the presence of any possible deadlock, and in case it finds any deadlock in the model, PARS tries to resolve them. In cases where the deadlock cannot be resolved automatically, it will report the source of deadlock and guide the user to resolve it manually.

If you have a multiprocessor design in your schedule, or are scratching your head with your current design, check out PARS, it might just help!

For more information email enquiries@sundance.com or contact your local Sundance Office.

Ultra Wide Band Modular Design

One of the most tangible benefits of our modular design philosophy is the ability our customers have to drop-in replacements, or upgrade core modules and functionality without having to redesign their system. This was what the guys at MIT found out when they used Sundance to help build an Ultra Wideband (UWB) communications development platform.

The backbone of the MIT system was our SMT118 carrier that implemented amongst other things the com port interface and the hardware reset for all the connected modules. Housed on one of the SMT118's CPU TIM sites was the SMT391-VP that served as reprogrammable signal processing module. Featuring a Virtex2Pro VP30-6, it had direct access to the output from the connected ADC that was capable of digitally sampling two independent input signals at 1 Gsample/sec. On the second and third TIM sites the team connected a custom carrier board to connect the control FPGA and discrete transmitter to the SMT118 carrier.

Add to this a Discrete Down Converter, oscillator, USB-Host link and advances in technology and changing specifications, and you can see why modular design makes sense from a financial and technical perspective.

The MIT team found that the combination of a modular design and an easy-to-use interface promised to make the UWB development platform an effective tool for both developing and demonstrating cutting edge UWB communication systems. And we agree with them.

One final thought, if the MIT team were able to achieve what they did using Virtex2 Pro FPGA for their signal processing module, imagine the possibilities if they revisited their UWB design using the latest Sundance 'Radio Giga' solution that features Virtex 5 Xilinx FPGAs, Dual C Series TI DSP engines with 260MBytes/ s Serial RapidIO (SRIO) communication links, Power PC processor cores and 6 channels of low power GHz ADC. If you'd like to take the 'imagine' and convert it to 'reality', get a Radio Giga system and get in touch!