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EVP6472 Intech Demo

Abstract

Camera demonstration application based on EVP6472 and SMT949

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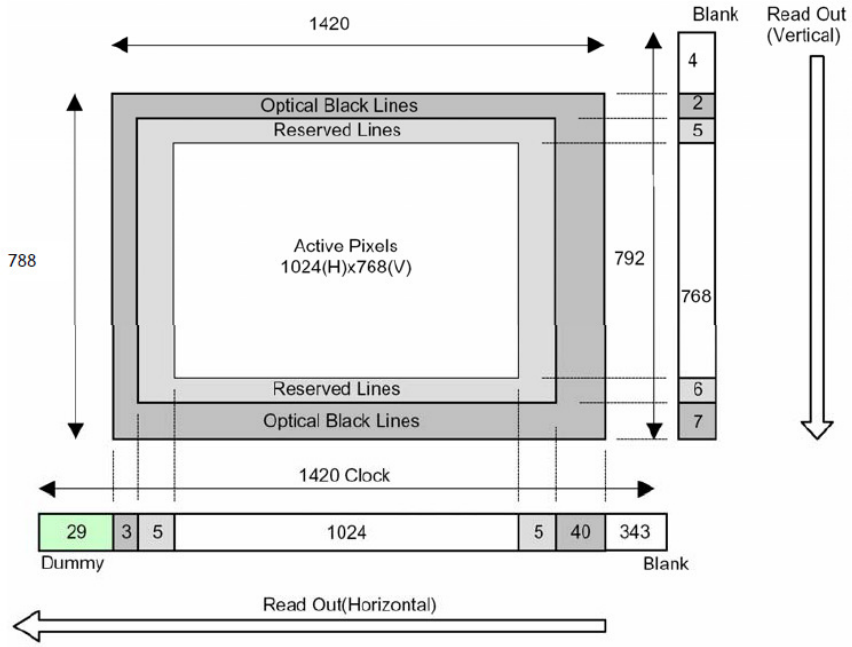
1. Features and Requirements

To run the application:

1. CameraLink camera:

   The application is designed for the JAI CV-M 9CL camera and applicable for all other CameraLink cameras. In default, the camera works at 1024×768 resolution with 33 MHz frame frequency, and uses base mode transmission (three channels, 24-bit RGB data). The frame timing is pictured as below.



2. Sundance hardware:

   SMT372T, SMT111 and SMT949

3. Sundance Software:

   SMT6002 (flash programing) and SMT111 driver

4. Cables:

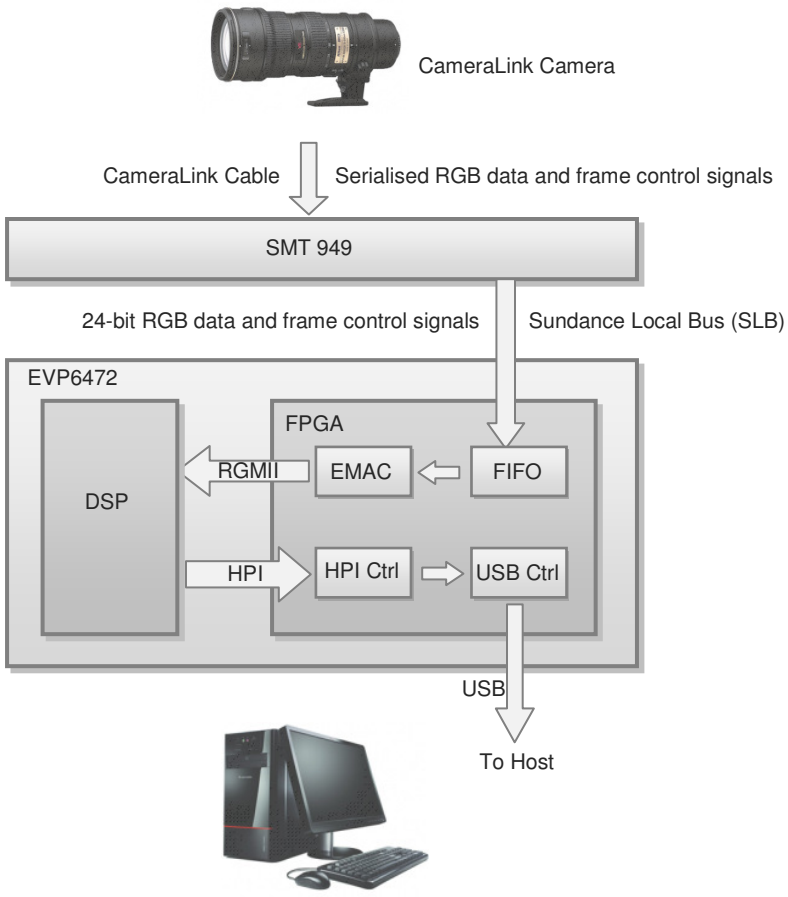
   CameraLink cable, USB cable, SMT111 power cable and Xilinx JTAG cable

To develop the application

1. Xilinx software tools: Xilinx EDK, SDK (12.3)
2. Taxes Instrument software tools: Code Composer Studio (CCS) (4.24)
3. Visual Studio or other host compiling kit (2008)

   *Source code is generated with the version in the bracket

2. Data Path



1. The camera captures pictures and transmits it to the SMT949 via CameraLink cable
2. The SMT949 converts the serialised data into 24-bit parallel RGB data and 3 frame control signals (line synchronization, frame synchronization and data valid) and sends it to the FPGA via the Sundance Local Bus (SLB)
3. The FPGA starts sampling pixel data depending on the frame control signals. Sampled pixels are buffered in the FPGA FIFO. Once the received data size meets the Ethernet package size, the pixels are transmitted to the DSP via the RGMII link.
4. The DSP receives the pixels and stores it in its 256M DDR RAM.
5. Once an entire frame is sampled, the FPGA starts fetching pixels stored in the DDR RAM through Host-Port Interface (HPI), and sends them to the host PC through the USB cable.
6. The picture is saved as ppm format, which can be viewed by the provided ppm viewer.

3. How the system works

After device configured:

1. After boot, the FPGA is automatically configured by the bitstream in the flash memory. The FPGA is configured as an embedded processor (MicroBlaze), and its peripherals used for accessing various interfaces.
2. MicroBlaze reads the DSP code from Flash memory.
3. MicroBlaze writes the DSP code to the DSP program memory through the HPI interface.
4. MicroBlaze sets up the DSP configuration through HPI interface.
5. MicroBlaze resets and starts the DSP.
6. MicroBlaze configures its frame capturer peripheral e.g. EMAC package size and package numbers.
7. MicroBlaze starts the frame capturer.
8. After one package size of pixels sampled, the frame capturer starts one EMAC transmission.
9. After the all required packages are transmitted (one frame is completed) DSP can start processing the image.
10. MicroBlaze starts fetching the pixels stored in the DDR RAM through the HPI and transmit to the host PC via USB.
11. The Host PC saves the incoming pixels as ppm format, which can be viewed by ppm viewer.

4. How to run the demonstration

Every time the EVP6472 boots up, it is self configured by loading the application code (bitstream for the FPGA and binary code for the DSP) from the flash memory. Therefore we need to program the flash for the very first time.

After flash programmed, the EVP6472 automatically starts working every time it boots up.

4.1 First time flash programming/recovery

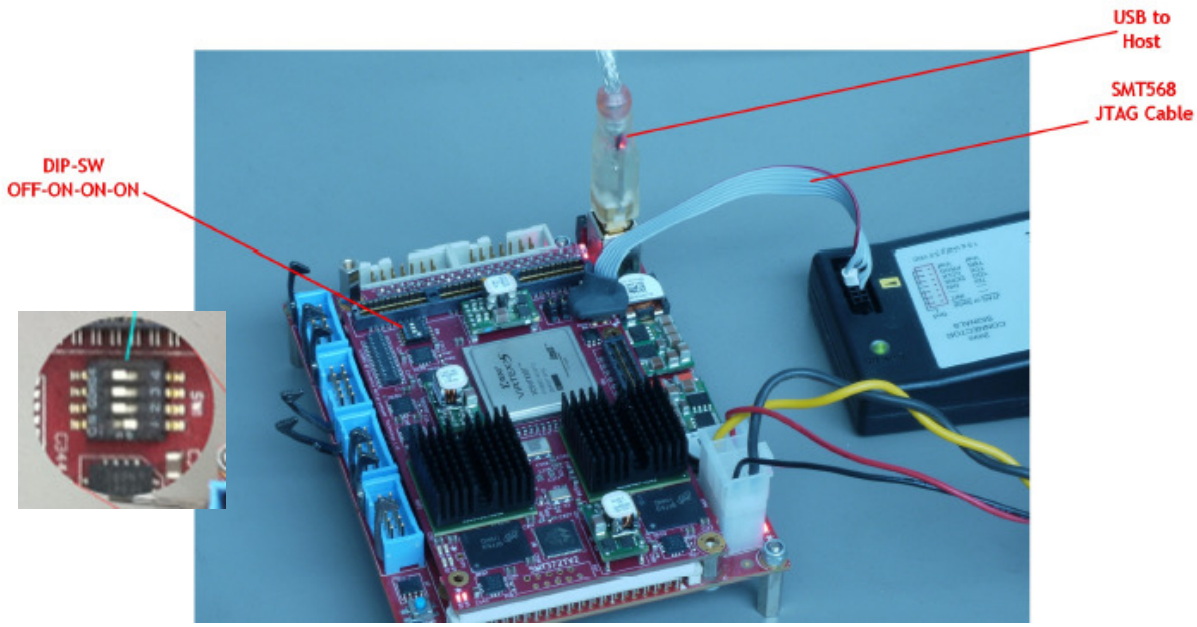
To program the flash, we use JTAG to load the bitstream to the FPGA, which communicates with the host through the USB.

The bitstream used for programming flash is the same one used for our normal application. It performs one of the actions depending on the first bit of the DIP switch (1 for programming flash and 0 for normal application). To programme the flash, steps are followed.

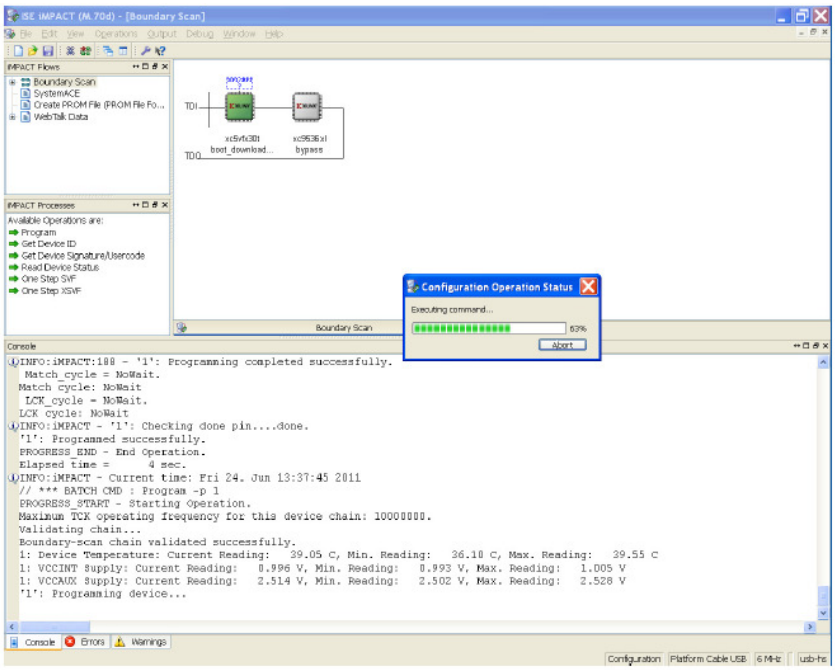
Ensure that the DIP-SW is set as shown above (position 1 OFF, the others ON).

Connect the USB cable from the SMT111 to the Host PC.

Connect the Xilinx programming pod to the SMT372T using an SMT568 JTAG cable.

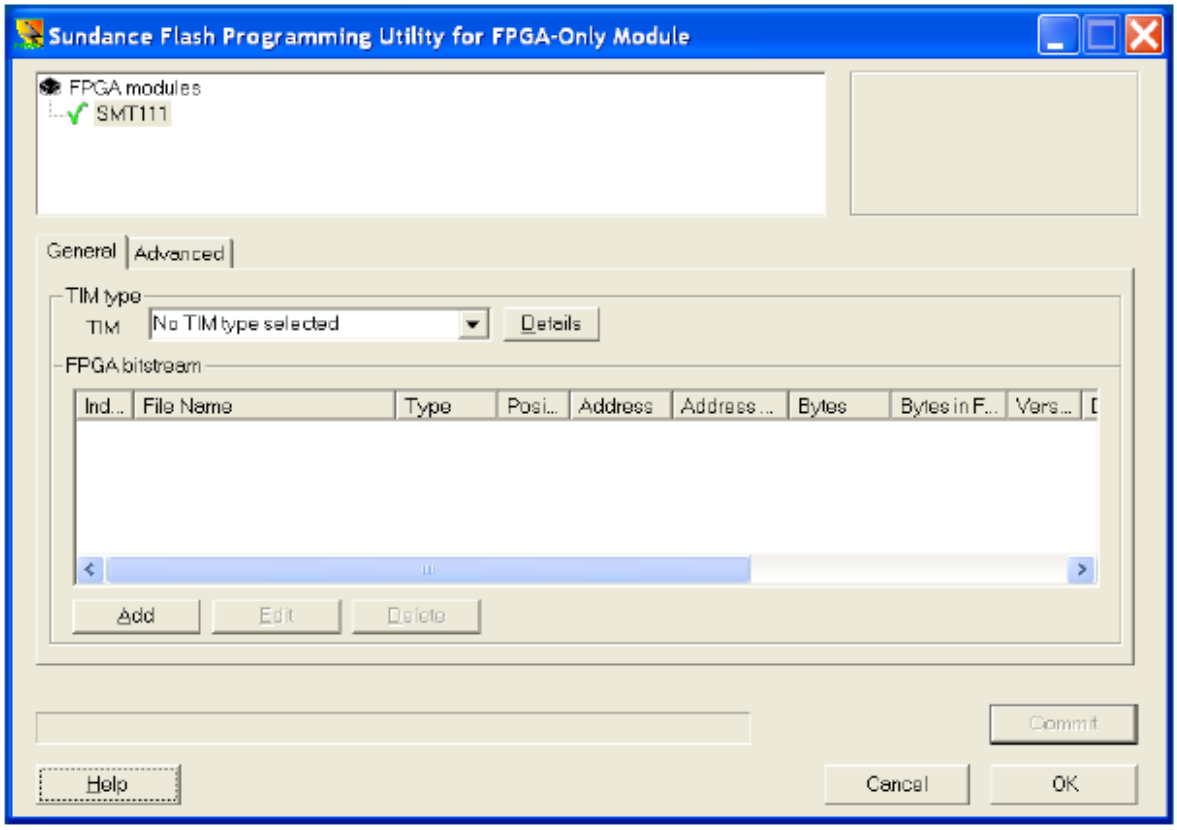


Run Xilinx impact programming tool and select boot_download.bit as the configuration file for the XC5VFX30T of the SMT372T.

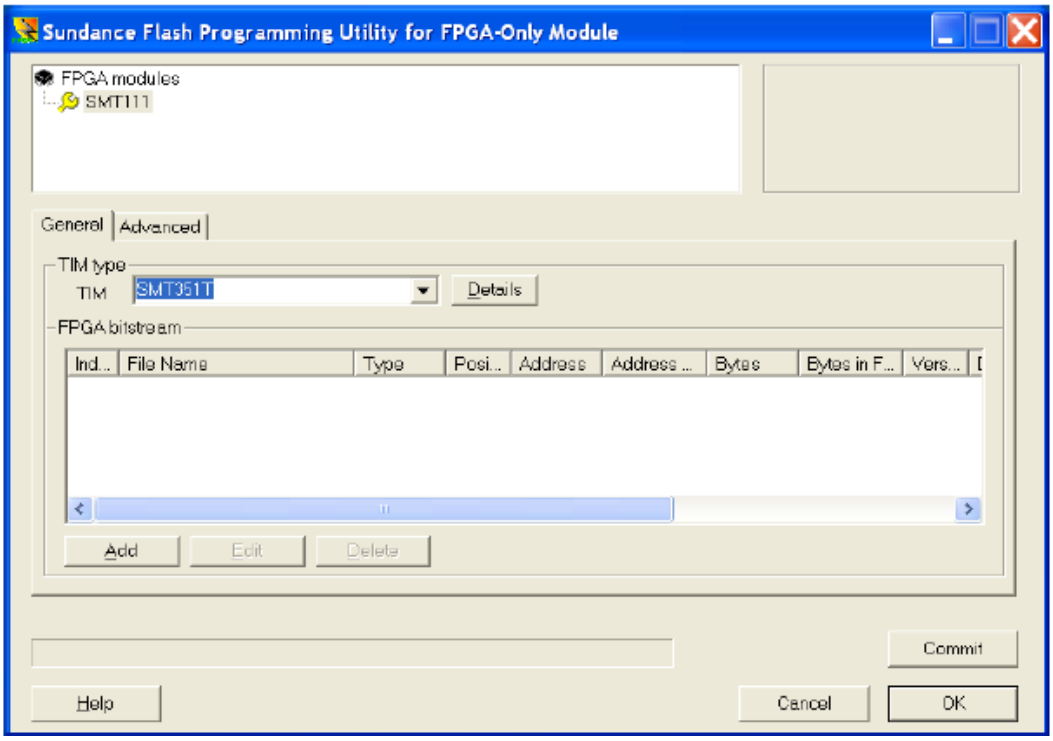


Configure the FPGA. When configuration is complete press the reset button on the SMT111. Do NOT power off the EVP system.

Run the SMT6002 application.



Select the TIM type as SMT351T.

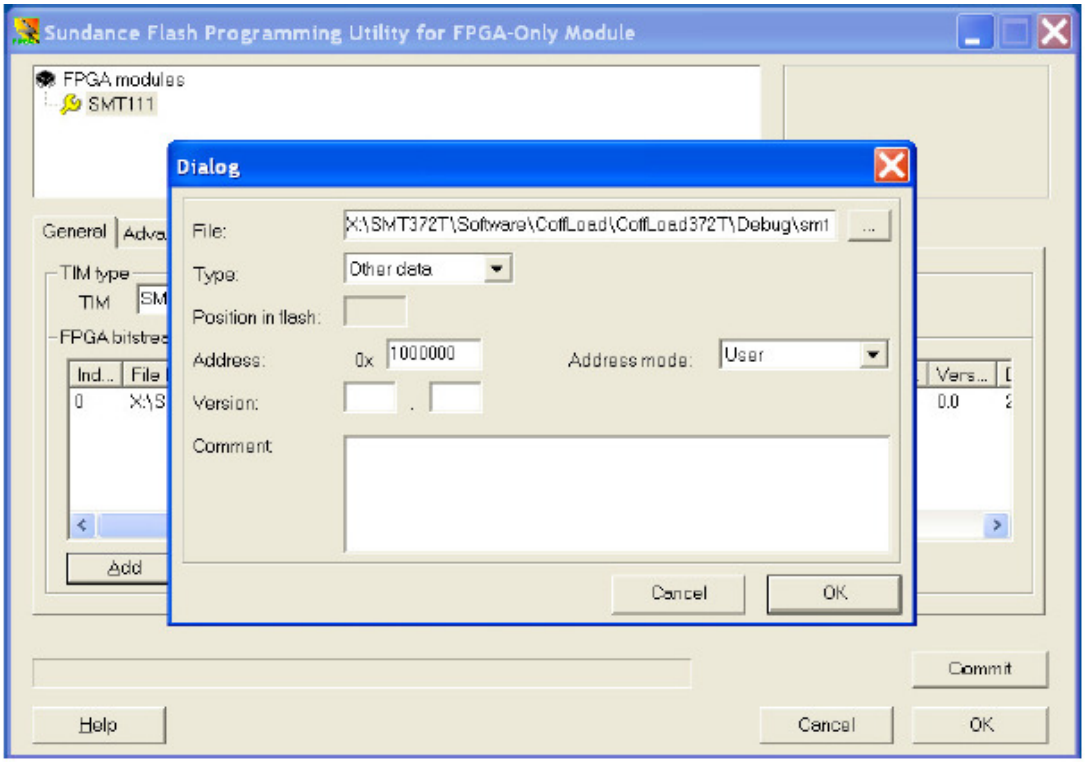


Add the boot_download.bit bitstream:

Type: Bitstream; address 0x0; address mode: basic.

Then add the smt372t.bin DSP application:

Type: other data; address 0x1000000; address mode: user.



Click OK, then Commit. When programming has finished close SMT6002.

4.2 Run the application

Set the DIP-SW as “1111” for normal application.

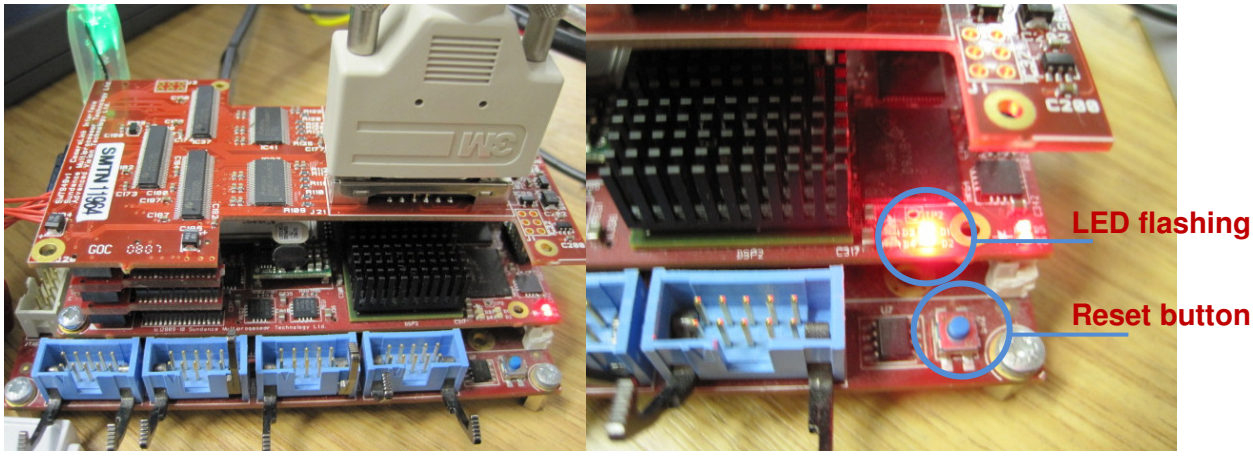
Power off the board, plug in SMT949, and connect CameraLink camera with the bottom CameraLink port, as shown in the picture.

Power on the board, press the reset button to reset the DSP (if success, the LED flashes for 1 second).

Run the host program (HostCmd.exe), after the command window close, a ppm file should be generated.

Open the ppm viewer to see the picture. If not clear, re-focus the camera.

To capture another picture, press the reset button (do not power off), and re-open the host program. The ppm file is overwritten.



Below is the a captured picture example (under the ppm folder) using CV-M 9CL camera with 1024×768 resolution