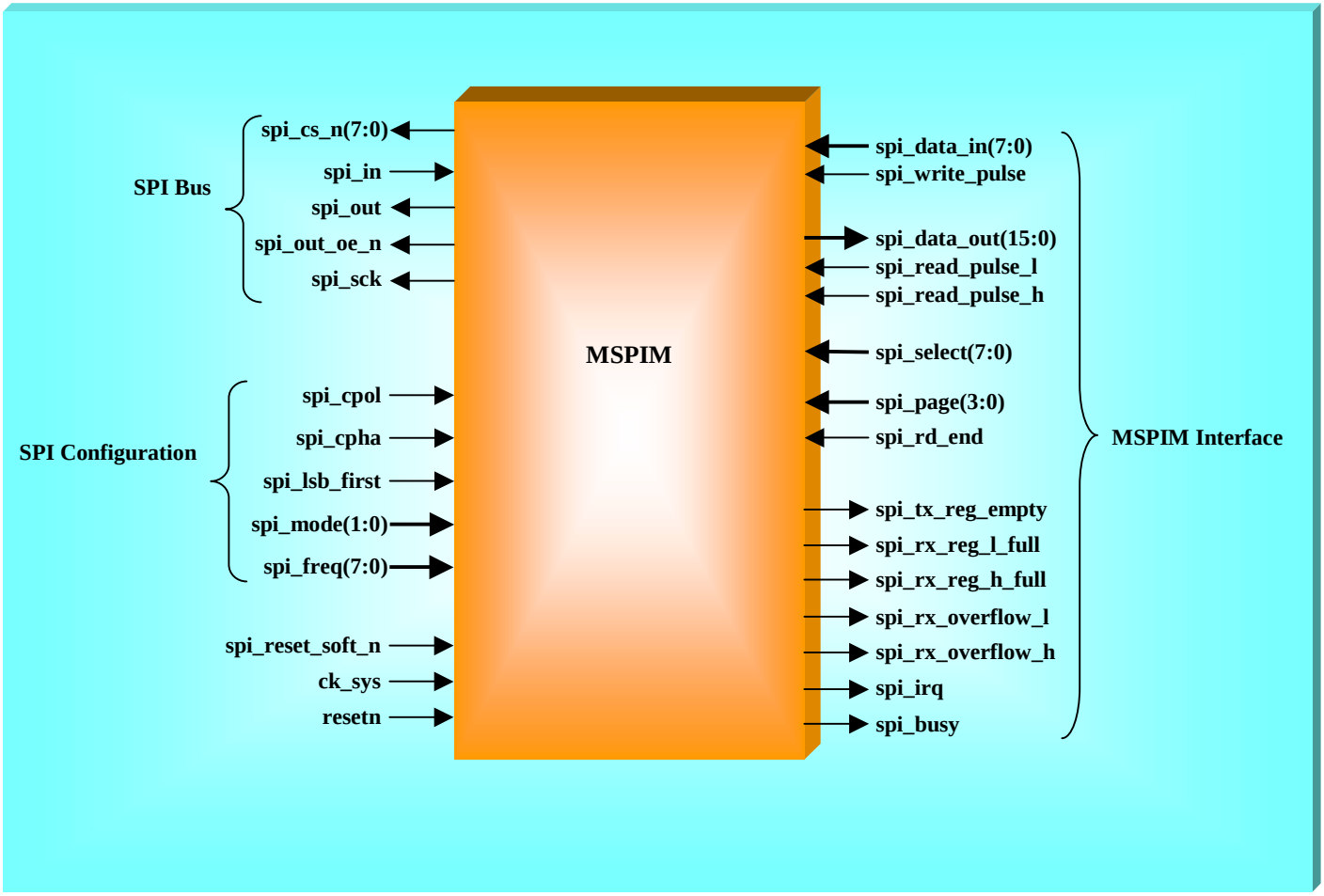
SPI Master
Serial Parallel Interface Master in standard mode
Serial EEPROM Controller in extended mode
VHDL *IP*

Product Brief

December 06 – Ver. 1.0



Features

- Single-chip synchronous SPI Master IP in FPGA
- Designed to be included in high-speed and high-performance applications
- Direct Connection to CPU register set
- High frequency rate
- Two run-time mode : Standard SPI mode and Extended SPI mode as SPI EEPROM controller
- Synchronised on system clock
- Serial clock programmable with polarity and phase
- Serial clock period can be at least 6 system clock period
- FPGA speed grade operating frequency dependant
- Available in VHDL source code format for ease of customization
- **DO254** documentation available
- Can be customized by Logic Design Solutions

Design Package

Device Family	Any FPGA	
LUT/FF	222 LUT4 / 131 FF *	160Mhz *
Tiles / Frequency ProAsic3	471 *	125Mhz *
Tiles / Frequency ProAsic+	572 *	87Mhz *
I/O	75 **	
Package file	**VHDL Source code** **VHDL Test Bench** for behavioural and gate level simulation. **Data Sheet** and **Reference Guide** **User's guide :** Simulation, Synthesis and Place and Route procedures. **Constraint File**	
Design Tool Used	VHDL synthesis from FPGA founder software. VHDL ModelSim simulation tool from ModelTech. Place and Route software according FPGA technology.	
Support	Support provided by Logic Design Solutions 1 year e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User Macro modifications. Maintenance Contracts available.	

* Rounded Number.
****** Assuming all IP signals are routed off chip.

General Description

The MSPIM IP implements a synchronous a single-chip SPI Master IP capable of high speed serial data transfer with up to 8 SPI slave. The MSPIM IP can be programmed to run either in standard SPI mode where bidirectional one byte transactions are implemented, or in extended SPI mode where frame transactions are implemented as an SPI EEPROM Controller. The MSPIM IP controls all SPI-bus specific sequences, protocol and timing. This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with Serial SPI, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The IP can be easily integrated into hierarchical VHDL designs.

Available Support Products

Support products available from Logic Design Solutions.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Related Information

Logic Design Solutions
106 Boulevard de la Résistance
93460 Gournay sur Marne – France.
Phone : +33 (0) 1 45 92 24 47
Fax : +33 (0) 1 45 92 22 10
E-mail : info@logic-design-solutions.com
WEB: http://www.logic-design-solutions.com