

Rapid Industrial Prototyping Heterogeneous Plate-form : 3G/4G Wireless Systems

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Abstract

Nowadays, high complexity processing algorithms are required in 3G and 4G wireless systems, giving great challenges to real time implementations. Programmable heterogeneous multi-components plate-form can provide suitable target solutions. This project involves the design and implementation of a platform for 4G air-interface system. It allows a modular design of systems with reconfigurable, interchangeable and reprogrammable software and hardware components.

1. Introduction

The rapid growth in wireless standards governs wireless communications, to name a few, CDMA-2000 for 3G cellular networks; IEEE 802.11 a/b/g for wireless local area networks; IEEE 802.16 for wireless wide area networks (Wimax). The evolution from 2G to 3G corresponds to adopting a new air interface but most of all to a change of focus from voice to multimedia. In order to satisfy the need of customer's mobility, SDR is the evolving technology to support this high data rate and high mobility access, thought to build flexible radio systems, multiservice, multistandard, reconfigurable and reprogrammable by software [1]. The multicarrier CDMA (MC-CDMA) air interface is being extensively studied for potential adoption in beyond 3G or 4G cellular networks. Today, there is an urgent necessity to start thinking about 4G [21] in order to offer high data rates over broadband radio channels for future multimedia services (Internet, video transmission, data transfer, etc...) which require the transmission of very high data rates over broadband radio channel. Thus, 4G is seen as not only an extension of 3G cellular networks but will also allow the convergence of mobile cellular networks and future Wireless Local Area Networks (WLAN).

Designing efficient architectures for these complex communication systems is of essential industrial and academics importance. The used of specific circuits (ASIC) is no more compatible with short time designs, need for reprogramming and capacity improvements. Due to increased complexity applications, achieving high performances solutions is no more guaranteed by fully software implementation, using General Purpose Processors (GPP) or Digital Signal Processors (DSP), or fully hardware implementation on ASIC. Thus, heterogeneous architectures, based on the combined use of components as FPGA and reprogrammable software processors such as DSP represent attractive solutions for complex SDR systems implementation and rapid prototyping. In this paper, we propose a multi-carriers transceiver configurable

to different transmission schemes. We present the SUNDANCE heterogeneous motherboard hardware platform used for the transceiver. It is build around DSP, FPGA for the digital front end processing, ADC, DAC for the IF stage. The RF front end interfaces to the IF stage (not presented in this short paper). This platform can be configured to support both single carrier systems (SC) and multi-carriers systems different modulation schemes (OFDM, MC-CDMA, ...). It can be extended from SISO (Single Input single Output) to MIMO (Multiple Input Multiple Output) schemes. Simulation results and validation measurements will be shown.

2. Hardware plate-from overview

A possible generic downlink transmission scheme of the MC-CDMA system is depicted in Figure 1. The Figure 2 shows an overview of our transceiver system based on heterogeneous components as DSP, FPGA DAC and ADC. The system consists of a transmitter and a receiver. In the transmitter, one FPGA and one DSP are available to implement the algorithms. The system is made of one SMT375 and SMT398 modules held on a SMT310Q PCI carrier board. The transmit clock is used by the FPGA as a clock reference to generate the carrier one and the sampling frequency for the DACs. The samples are computed with a signed format of 14 bits. The samples are then provided to two available converters ANALOG DEVICES AD9772A at the rate of 20 MHz. We configure them in IF direct mode with the "zero stuffing" option activated. Thus, the output signal is generated with a sampling frequency of 80 MHz and, while suppressing the original baseband image, the upper and lower in-band images can be selected according to the RF front end. The receiver system is made of two single ADC input channels. One FPGA and one DSP are available for the data processing. The system is made of one SMT398, one SMT335 modules held on a SMT310Q PCI carrier board. The ADCs are synchronized together to all start sampling at the same time.

The mother boards SMT310Q exchange data with the PC through a PCI interface through shared memory available on the PC.

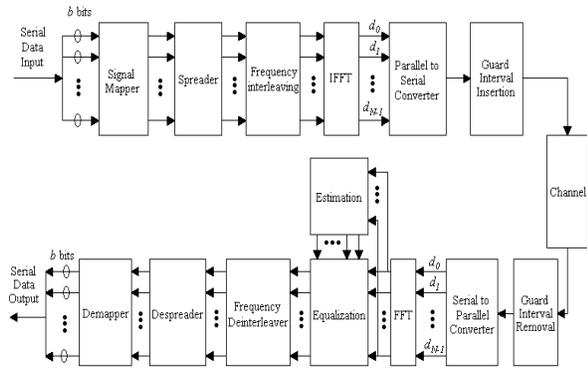


Figure 1 : MC-CDMA transmitter/receiver

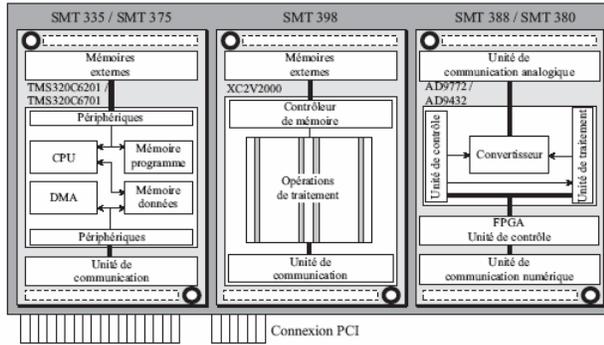


Figure 2 : MC-CDMA hardware transmitter/receiver

3. System Parameters & Results

Two basic MC-CDMA configurations, which parameters set is summed up in Table 1, are available. They are based on HIPERLAN Type 2 specifications with a 20/50 MHz system frequency. These parameters can be changed on the fly according to the channel environment, by using the configuration of the different IP of the system, or by using dynamic reconfiguration of modules. Different simulations have been performed using the configurations I and II [3], which illustrate the main advantages of MC-CDMA modulation. Figure 3 illustrates the transmitted MC-CDMA signal, both in frequency and time domain. In Figure 3.a, we observe the MC-CDMA frame, with one symbol for synchronisation and 6 OFDM data user. In Figure 3.b, we observe the MC-CDMA spectrum, in IF band before filtering the images.

Parameters	Conf I	Conf I
Sampling frequency/Used Bandwidth	20 MHz/15.4 MHz	20 MHz/37.5 MHz
Bit rate per user	6/3/1.5 Mbps/s	6/3/1.5 Mbps/s
Sub-carrier spacing (Δf)	321.5 kHz	321.5 kHz
Number of users (N_u)	4-8-16	4-8-16
Number of total / used sub-carriers (N_c / N_{cu}) / Spread Factor L_c	64 / 48 / 16	64 / 48 / 16
Symbol / Guard interval duration (T_u / T_g)	3.2 μ s / 0.8 μ s	3.2 μ s / 0.8 μ s

Table 1: Transceiver parameters

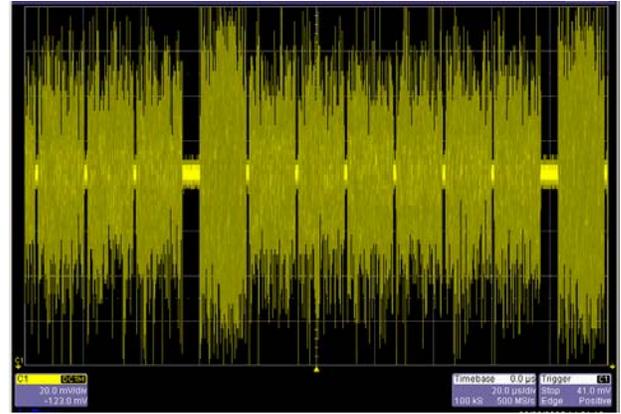


Figure 3.a : MC-CDMA transmitted frame

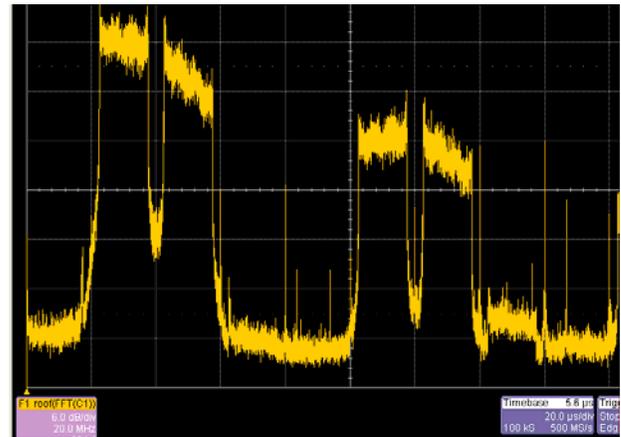


Figure 3.a : MC-CDMA spectrum in IF

4. Conclusion

In this project, we have presented the MC-CDMA transceiver scheme developed for the PALMYRE platform. Implementation of digital parts and validation measurements have been shown. Further work will include an extension of the transmission scheme to a MIMO 2x2 system then 4x4.

5. References

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