Sundance Multiprocessor Technology Limited **Design Specification**	Form : QCF51 Dated : 20 June 2003 Revision : 6

Unit / Module Name:	High Speed Image Processing Module
Unit / Module Number:	SMT339
Used On:	SMT114,SMT310,SMT310Q,SMT145,SMT300,SMT300Q
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Revision History

Issue	Changes Made	Date	Initials
0.9	Initial Draft	15/12/04	AJP
0.91	Corrections and Block description	06/01/05	AJP
0.92	Corrections	07/01/05	AJP
0.93	Corrections	10/01/05	TJW
0.94	Re-Write FPGA functional description	10/01/05	AJP
1.0	Proof Read	10/01/05	TJW
1.1	Minor corrections	11/01/05	AJP
1.2	ZBT used instead of QDR	10/02/05	AJP
1.3	General Update	04/06/05	AJP
1.4	Minor updates	24/11/05	SP
1.5	Added 64Mbytes option to SDRAM	9/12/05	AJP
1.6	Added ZBT description	17/03/06	AJP

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1 Introduction

The SMT339 is a dedicated second generation high speed image processing module for use in a wide range of image analysis systems, replacing the SMT319 introduced in 2002. The module can be plugged into a standard TIM single width slot and can be accessed by either a standard ComPort, or Rocket Serial Link (RSL) Interface. The module can also operate in a "stand-alone" mode for us in SMART camera and SMART monitor applications.

The image processing engine is based upon the 'Texas Instruments' TMS320DM642 Video Digital Signal Processor. It is fully software compatible with C64x using Code Composer Studio.

The DM642 runs up to a clock rate of 720Mhz. It features a two level cache based architecture. There are 16K Bytes of level one program cache (Direct mapped), 16K Bytes of level one data cache (2-Way Set-Associative) and 256K Bytes of level two cache that is shared program and data space (Flexible RAM/Cache Allocation). The DM642 can perform 4, 16 x 16 Multiplies or 8, 8 x 8 Multiplies per clock cycle.

A powerful Vitrex-4 FPGA (XC4VFX60) is used onboard as the FPGA processing unit for image data. Upto 8 Mbytes of ZBT SRAM is provided as a FPGA memory resource. Processing functions such as Colour Space Conversion (CSC), Discrete Cosine Transforms (DCT) , Fast Fourier Transforms(FFT) and convolution can be implemented, without using any of the DSP's resources. If required, the Virtex 4 has 2 Power PC hardware cores that can be incorporated into the system design.

The Module features a single 'Philips Semiconductors' SAA7109AE/108AE video decoder/encoder that accept most PAL and NTSC standards, and can output processed images in PAL/NTSC or VGA (1280x1024, or HD TV Y/Pb/Pr)

The DM642 has 64 or 128 Mbytes of high speed SDRAM (Micron MT48LC64M32F2S5) available onboard for image processing and an 8Mbyte FLASH device is fitted to store programs and FPGA configuration information.

The module supports a full Sundance LVDS Bus (SLB) interface for use with mezzanine cards providing the flexibility for other image formats to be accepted and other output formats to be generated.

1.1 Related Documents

Sundance **L**VDS **B**us (*SLB*) Specifications – Sundance.

TIM specifications.

Xilinx Virtex 4 FPGA's XC4VFX40.

MMCX Connectors – Hubert Suhner.

2 Functional Description

2.1 DSP Unit

As illustrated in Figure 1 the SMT339 is based around the TMS320DM642 Video Imaging Processor. The processor is based around the second generation VelociTI Texas Instruments TMS320C6000 generation of processors. This processor has 3 built-in video imaging ports (each 20 bit) which each have 2 channels capable of sample rates upto 80MHz over a 10 bit bus, the direction of each channel being configurable as input or output. This allows Images to be DMA'ed directly to the SDRAM for processing, while the processed image can be viewed on one of the output channels. Input YCbCr formats with embedded sync information can be accepted by the video ports as well as RAW data modes.

The DM642 DSP has 64 or 128Mbytes of high speed SDRAM memory available for program and data space, a 8Mbyte FLASH allows FPGA configuring data and DSP program data to be stored. The DSP's EMIF bus is also routed to the Virtex 4 FPGA, which allows the mapping of the ComPorts and the RSL directly into the DSP's memory map.

The EMAC, serial ports and Audio channels are routed from the DSP to the Virtex 4, this allows the EMAC, SLB or Audio physical interfaces to be added to the system if required.

Software development and real-time debugging can be achieved using Code Composer Studio (Texas Instruments) via the JTAG interface.

Full specifications for the DSP can be downloaded from

http://focus.ti.com/lit/ds/symlink/tms320dm642.pdf

2.1.1.1 Flash

An 8Mbyte flash memory is provided with direct access by the DM642. This device contains boot code for the DSP and the configuration data for the FPGA.

This is a 16-bit wide device.

The flash device can be re-programmed by the DM642 at any time. There is a software protection mechanism to stop most errant applications from destroying the device's contents.

Note that the flash memory is connected as a 16 bit device, but during a DM642 boot (internal function of the C6x) only the bottom 8 bits are used.

2.2 Virtex 4 Pro FPGA

Some of the FPGA's features are listed below.

- The Virtex-4 enhanced PowerPC™ 405 core delivers 680 DMIPS performance at 450 MHz and the new Auxiliary Processor Unit (APU) controller
- 400+ MHz clock rates

- From 2.5Mbits to 6.7Mbits of internal block RAM available depending on part selected.
- Up to 444 18X18 embedded multipliers
- Extensive library of DSP algorithms
- DSP tools such as The MathWorks MATLAB™/Simulink™, the Xilinx System Generator for DSP, and Cadence SPW

2.3 ZBT RAM

There is just over 8Mbytes of high speed, no turnaround, (Nt) SRAM is connected to the FPGA allowing high speed data storage capability to FPGA cores that require external memory. The memory is based on two separate Samsung K7N321801M devices which are each 2M by 18-bit devices, allowing independent access of each device

2.4 Video Encoder/Decoder

The encoder/decoder is based on the 'Philips Semiconductors' SAA7109AE/108AE. This provides decoding of PAL, NTSC and SECAM signal standards. On-board scaling circuitry allows the output image size to be specified by the DSP using the I^2C interface. Two inputs are available through on-board connectors. These can be defined as 2x CVBS or 1 Y/C channel, again configured over the I^2C interface.

Image data from the decoder flows through the FPGA, for potential pre-processing, before being routed to the DSP video ports.

The video encoder section of the device allows data from the DSP (which can be post processed by the FPGA) to be displayed in a number of different output formats. These include PAL, NTSC and VGA with resolutions upto 1280x1024 at 60Hz. Alternatively the encoder can output High Definition (HDTV) resolution images of 1920x1080 interlaced (or 1920 x 720 progressive) at 50Hz or 60Hz. The input format to the encoder is selectable between YCrCb and RGB.

The encoder also has output look-up tables and a hardware cursor sprite to be implemented.

2.5 SLB Header

The **S**undance **L**VDS **B**us (*SLB*) is a dual-port parallel interconnection link that is capable of supporting data transfers at up to 700 MHz. Each port can be assigned with a 16-bit differential bus, a clock and an over range differential lines.

The *SLB* is a link for data and clocks but also for control signals; it is based on a Samtec QSH/QTH-DP series (0.5mm pitch) connectors.

The use of the SLB means that other customer specific input or output methods can be supported without the need for re-design of the DSP/FPGA foundations. Some examples of IO interfaces are listed below.

Input

Camera Link

Firewire

CMOS Sensor

Fiber Channel

Output

USB

IDE

Fiber Channel

LCD/Plasma Display drivers

2.5.1 SLB Power Supplies

When using the SLB interface a separate SLB power header (BKT) is used to supply the Daughterboard. Details of this connector pinout can be found in the SLB Reference Guide.

2.6 Block Diagram

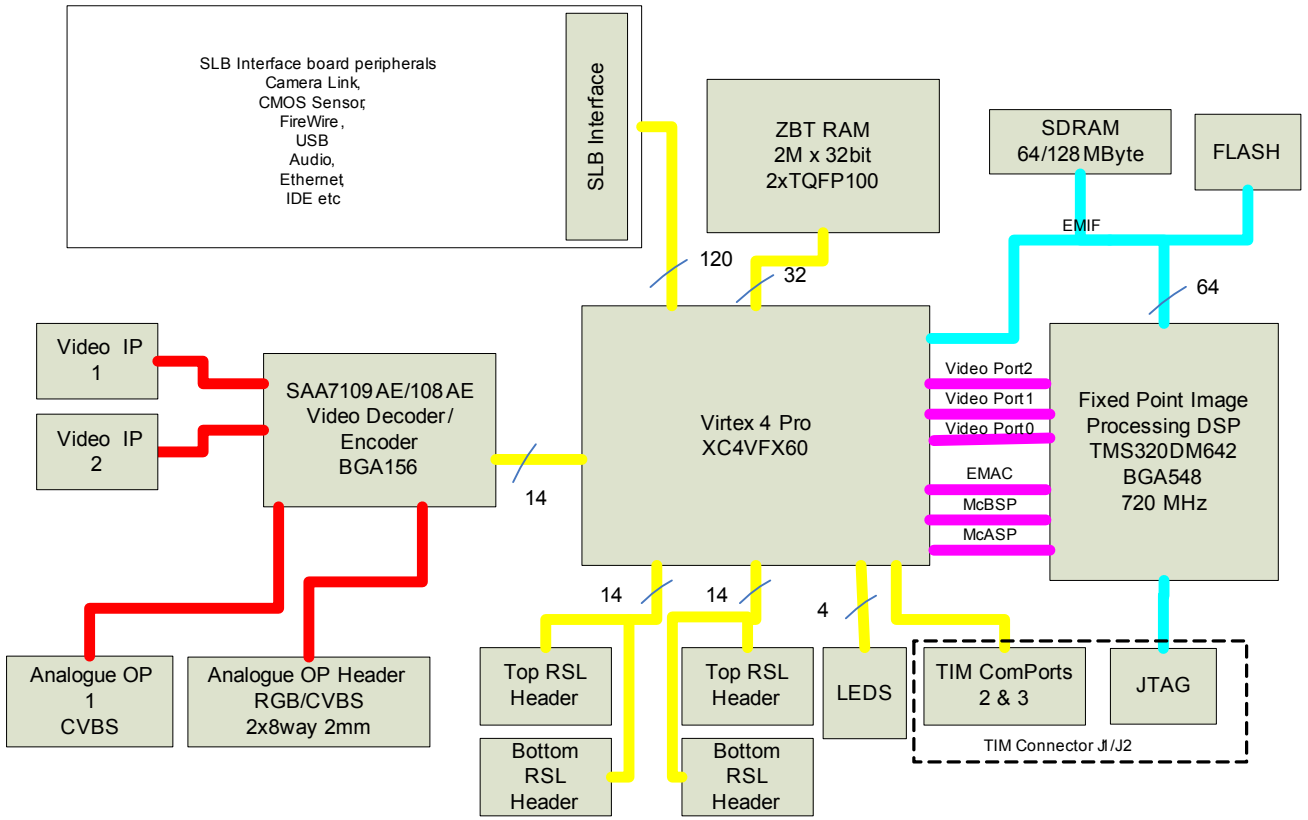


Figure 1 : SMT339 Block Diagram

3 Mechanical Interface

This module conforms to the TIM standard (**T**exas **I**nstrument **M**odule, See TI TIM specification & user's guide.) for single width modules.

The module sits on a carrier board.

The carrier board provides power, Ground, communication links (Comport links) between all the modules fitted and a pathway to the host, for a non stand-alone system.

The SMT339 requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards), which must be provided by the two diagonally opposite mounting holes.

3.1 Video Input Connectors

Video input signals are all connected to the *SMT339* via MMCX connectors.

3.2 Video Output Connectors

3.2.1 Single CVBS Output

Video single CVBS output signal uses a MMCX connectors.

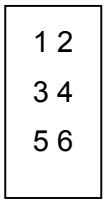
3.2.2 Mixed RGB/VGA channel Output

A 6 way (1 by 6) 2mm locking header is used to connect to the RGB/CVBS output signals.

4 Electrical Interface

4.1 JP5 Virtex JTAG Header

Pin #	Description
1	3.3V
2	TCK
3	TMS
4	TDI
5	TDO
6	GND



4.2 JP7 Connector

Mixed RGB/VGA channel Output

The pinout of the connector is show below.

Pin #	Description
1	GND
2	Red/Cr/CVBS 1
3	Green/Y/ CVBS 2
4	Blue/Cb/ CVBS 3
5	V Sync
6	H Sync

For pinout and information of the SLB signal and power connectors see :

Sundance **L**VDS **B**us (*SLB*) Specifications – Sundance.

For pinout and information of the TIM signals see :

TIM specifications.

4.3 PSU Requirements

This module must have 5V supplied through the TIM connectors. In addition, a 3.3V supply is required and should be supplied through the TIM mounting holes.

Contained on the module are linear regulators for the DM642 and FPGA.

The DM642 core voltage is provided through a linear regulator from 3.3V.

All supplies a guaranteed to meet the worst possible requirements of the FPGAs.

5 Verification Procedures

The verification procedure for the module is as follows.

5.1 DSP verification

Code Composer Studio is run and a boot application is loaded via JTAG. The program runs in internal memory which allows the on-board FLASH and SDRAM to be verified using “walking 1’”, “ramp” and random test patterns.

5.2 FPGA verification

The DSP will perform a number of accesses to the internal VIRTEX 4 registers. And also test the ZBT memories.

5.3 ComPort Interface

Using a SMT310/SMT310Q the PC host will transfer test data to and from the PC to the DSP via the comports.

5.4 RSL Interface

The two RSL headers are connected via a RSL lead. A test packet of 10Mbytes is transferred and verified, in both directions, at 2.5 Gbps.

5.5 Video Encoder/Decoder

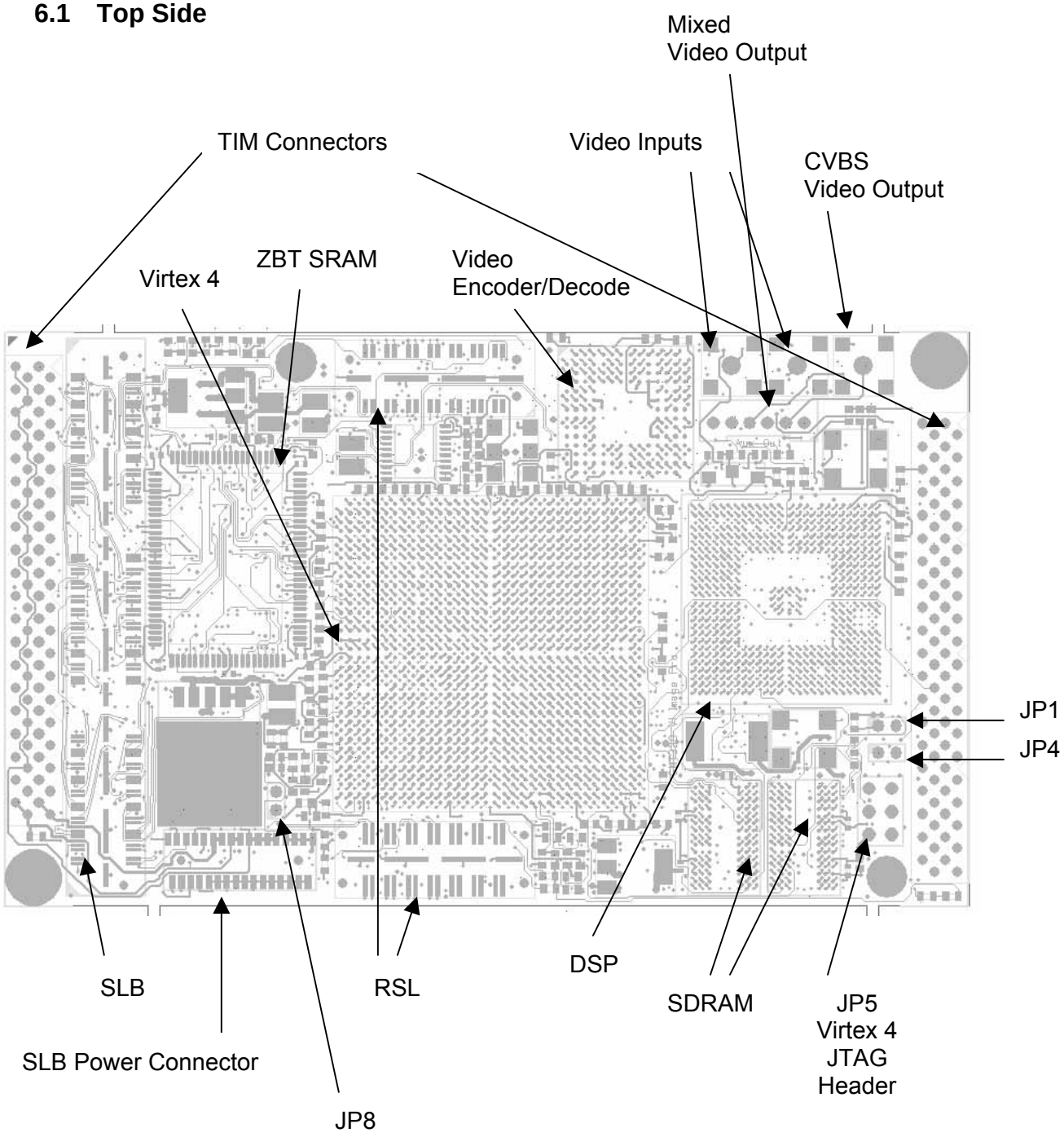
A number of test patterns are generated by the DM642 and saved into SDRAM. Two DMA channels are then opened over two of the DM642 video ports. The test patterns are transmitted via the video encoder. The encoder output is connected to the decoder input, via the video loop back lead, where it is transferred back into the SDRAM. A pixel value tolerance is used in the verification procedure to account for ADC/DAC conversion errors.

5.6 SLB Interface

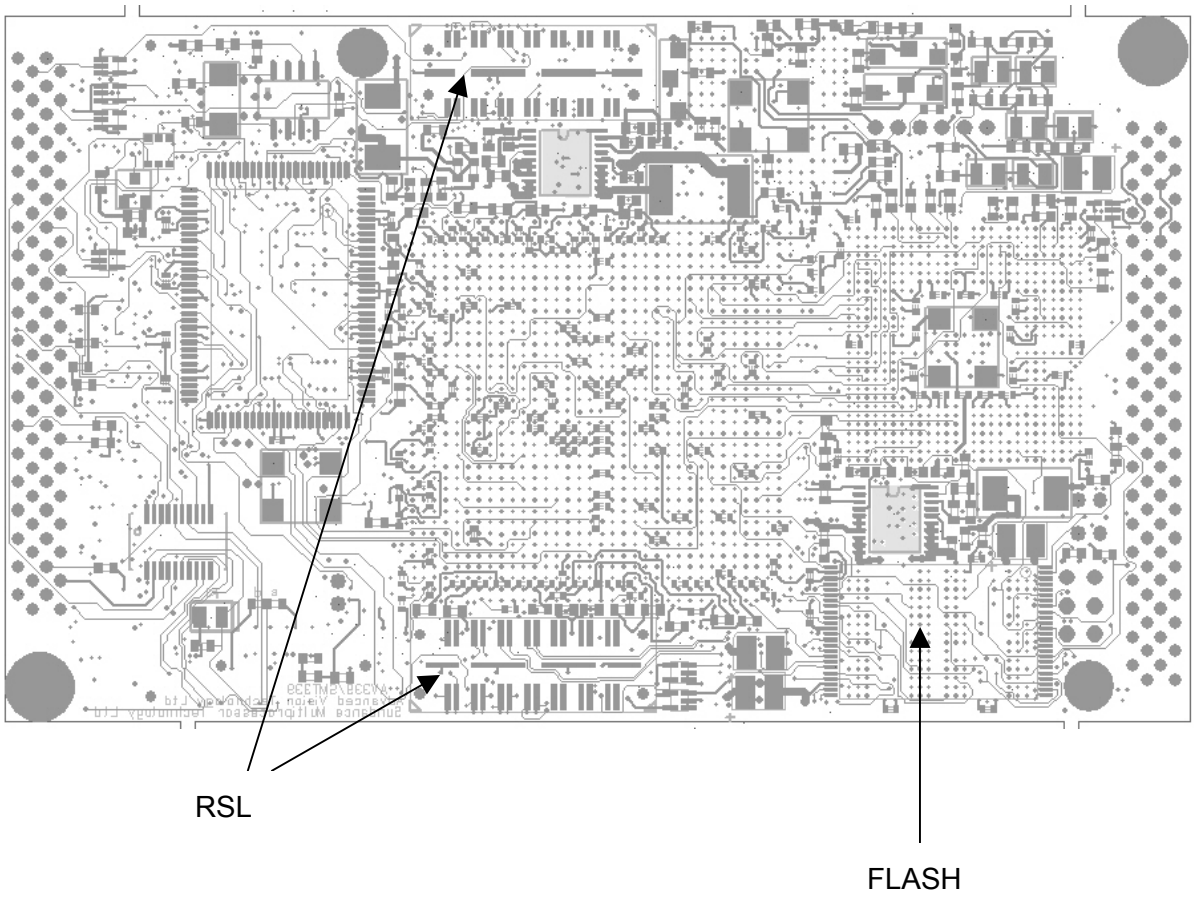
This is tested with a SLB LED test unit.

6 PCB Layout Details

6.1 Top Side



6.2 Bottom Side



7 Jumpers

JP1 Flash Write Protect : Must be jumpered to allow FLASH write accesses

JP4 Virtex Erase : This takes the Virtex 4 Prog line low when removed. It allows the fpga to be erased during development if a latch-up situation occurs.

JP8 SLB JTAG Bypass : When inserted the TDI, TDO signals on the SLB header are connected together. This allows the DSP JTAG chain to be completed when no DSP is present on a SLB DSP expansion card.

8 Safety

This module presents no hazard to the user.

9 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.