SMT349

User Manual

Certificate Number FM 55022

Revision History

Date	Comments	Engineer	Version
09/01/2006	First release, COMLAB' specifications	SM	1.0
18/01/2006	Minor modification	SM	1.1
30/01/2006	Added initial photo, cleanup diagrams, text	BV	1.2
04/07/2006	Changed photos, SHB table, LEDs, JTAG pinout corrected, connector locations added, added registers information, document numbering	PSR, AL	1.3
20/07/2006	Figure 6 removed FPGA speed changed to –4 RSSI removed Table 3 removed	PSR, AL	1.4
31/07/2006	Connector idents corrected on block diagram and connector location diagram.	PSR	1.5
19/11/2006	Auto-tune function added	PSR	1.6
24/11/2006	Diagram Updated	PSR	1.7
26/07/2007	Control Word structure corrected	PSR	1.8
20/11/2007	Ordering information added	PSR	1.9
08/01/2008	External Clock characteristics added	PSR	2.0
15/09/2008	Linear Output Power corrected	PSR	2.1

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Contacting Sundance

You can contact Sundance for additional information by login onto the Sundance support forum**.**

1 Notational Conventions

1.1 SDB

The term SDB will be used throughout this document to refer to the Sundance Digital Bus interface.

1.2 SHB

The term SHB will be used throughout this document to refer to the Sundance High-speed Bus interface.

1.3 Comport

The term Comport will be used throughout this document to refer to the 8-bit communication port following the TIM C40 standard.

Precautions

In order to guarantee that the *SMT349* functions correctly and to protect the module from damage, the following precautions should be taken:

- The *SMT349* is a static sensitive product and should be handled accordingly. Always place the module in a static protective bag during storage and transition.

- Make sure that the heat generated by the system is extracted e.g. by the use of a fan extractor or an air blower at all times. Sundance recommends and uses PAPST 12-Volt fans (Series 8300) producing an air flow of 54 cubic meters per hour (equivalent to 31.8 CFM). The Fan should be placed in front of the SMT349.

2 Outline Description

The SMT349 is an IF/RF module, size 1 TIM offering the following features:

- Support two antennas transmit or receive in the same frequency,
- Two Sundance High-speed Bus (SHB) connectors,
- Two comports,
- Low-jitter system clock,
- Xilinx Virtex-II FPGA (XC2V1000-4)
- 50-Ohm analogue RF/IF inputs and outputs and external clock (option) via MMBX (Huber and Suhner) connectors,
- User defined pins for external connections,
- Compatible with a wide range of Sundance modules via ***SHB*** connectors,
- TIM standard compatible,
- Default FPGA firmware implementing all the functions described in this documentation.

The technical specifications for the IF/RF part are:

- Input signals are filtered by 1st IF tuned to 70MHz ± 8MHz,
- RF output signal is in the 2.4–2.5 GHz ISM band,
- RF input signal is in the 2.4–2.5 GHz ISM band,
- IF output signal is 70MHz ± 8MHz,
- The 70MHz IF is converted to a 2nd IF of 374 MHz.

3 Block Diagram

The following drawing shows the block diagram of the SMT349 module.

Each RF chain is build from 3 sub-modules:

- **up-converter**,
- **down-converter**,
- **RF**.

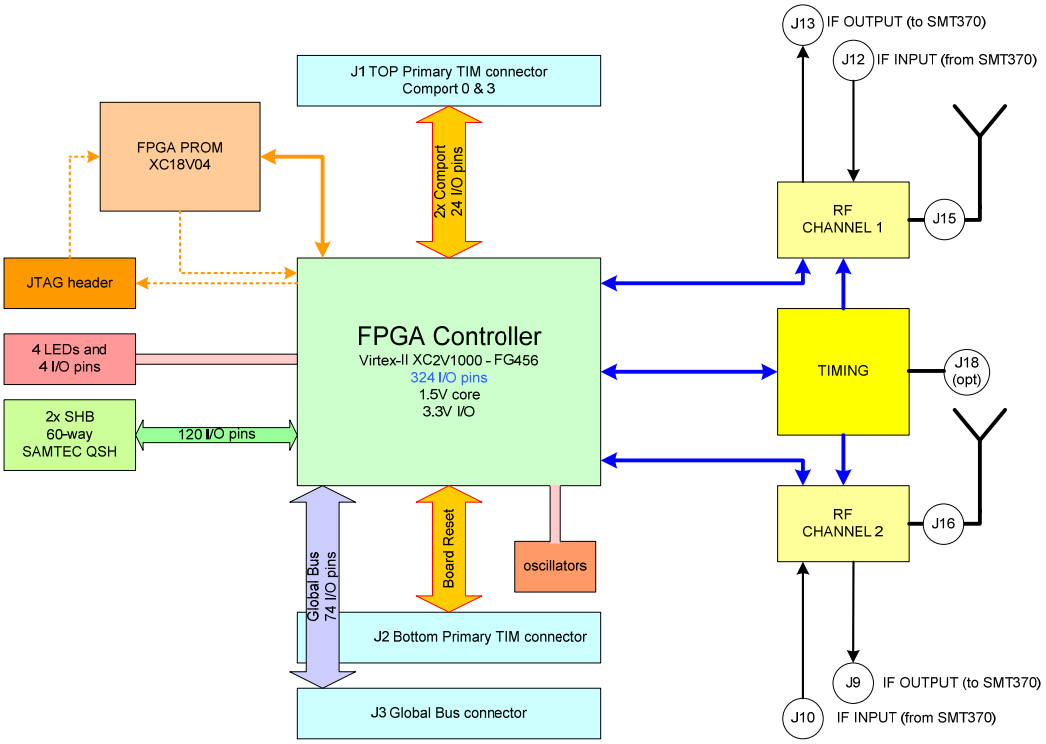

Figure 1: SMT349 Block Diagram

4 Architecture Description:

The SMT349 is an **IF/RF front-end module** that completes the transmission and reception paths of Sundance Digital Radio systems. The design is compatible with the other Sundance modules such as the SMT370, which operates on SMT8036 hardware platform and complies with the TIM40 specifications.

The digital section of SMT349 is based on the SMT370 digital section design. The analogue section of SMT349 includes two RF transceiver modules, operating in the 2.4 GHz ISM band. The RF centre frequency of both transceivers is controlled by one synthesizer which can be set by the FPGA. The FPGA also controls the AGCs (attenuators) and TX/RX switch for each of the two IF/RF sections. The FPGA can communicate with other Sundance modules via the SHB, or via the Comports, through the TIM connectors.

4.1 TX up-converter module

The up conversion from the 70MHz IF to the 2.4 GHz is done in two stages:

- The first stage converts the 1st IF to 374 MHz
- The second stage converts to the RF frequency

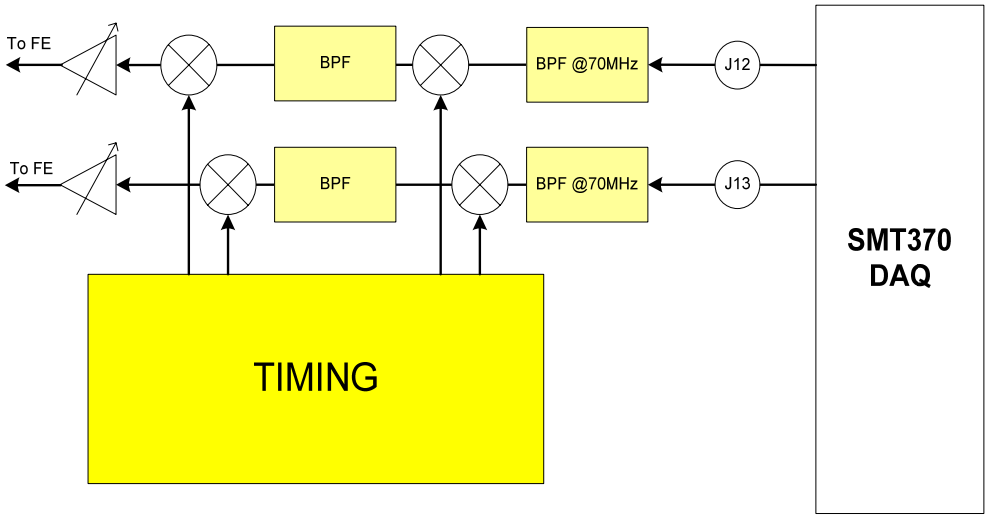

Figure 2: TX up-converter sub-module

4.2 Technical specifications of the TX up converter sub-module:

Linear Output Power ..... -20dBm, average
Output power at 1dB compression ..... 0dBm, minimum
RF frequency Range ..... 2400 to 2500 MHz
Gain Control ..... 31dB, in 1dB steps
Gain control accuracy……..±2dB maximum

4.3 Driving the inputs from a DAQ module:

To drive the two inputs of the SMT349 from a single SMT370 one can provide low IF signal to the input of the module. An example of low IF frequency of 14 MHz planed to provide 3rd replica of the signal that will be captured and filtered in to the module is illustrated in Fig. 3. Other frequency plans are possible as well.

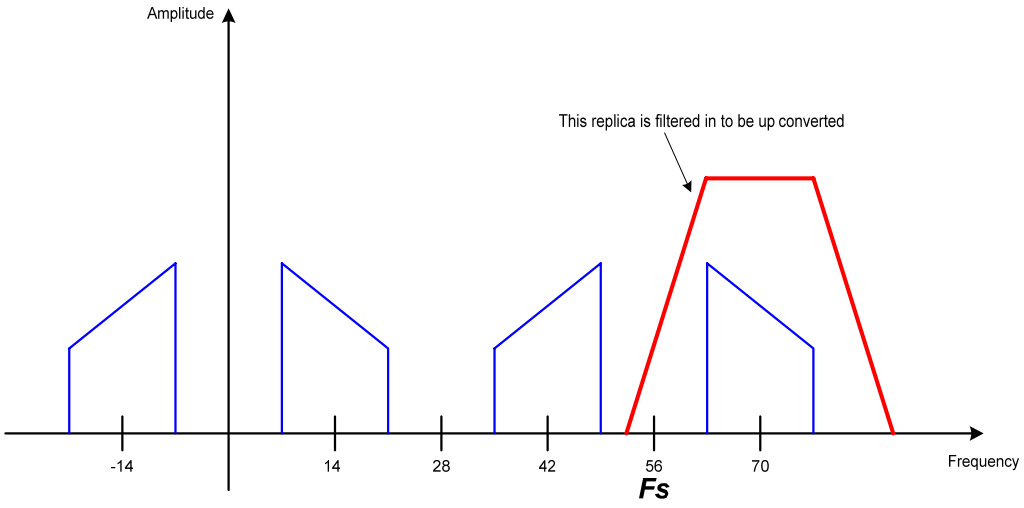

Figure 3: Spectrum of input signal

4.4 RX down-converter

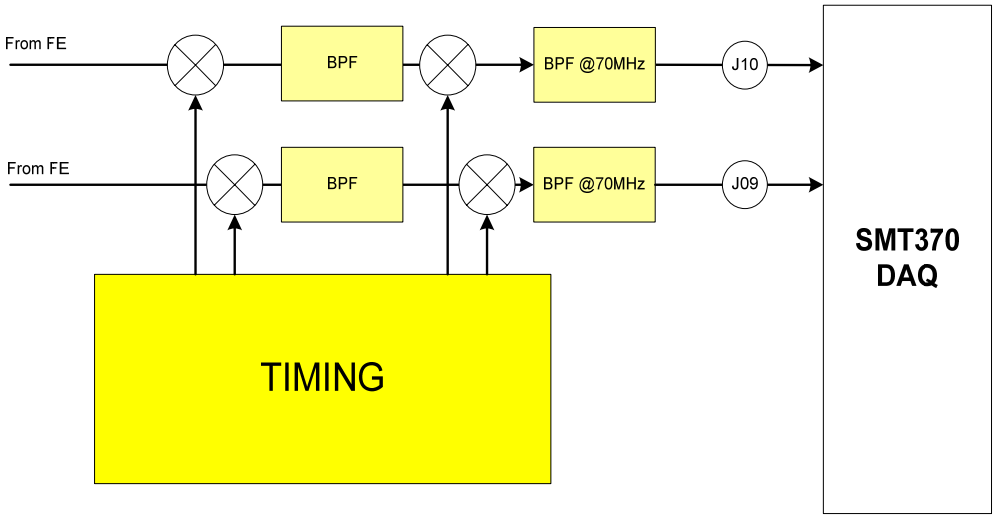

Figure 4: RX down-converter

4.5 Technical specifications of the RF down converter:

Sub-System Noise Figure ..... 7dB maximum
LO leakage..... -35dBm
1st IF image rejection..... 20dB
Input IP3..... -8dBm minimum
Down converter gain ..... 40dB, AGC at minimum
AGC range ..... 60dB, at 1dB steps
RF frequency Range ..... 2400 to 2500 MHz
IF frequency ..... 374 MHz

4.6 RF

The RF sub module provides the necessary pre-conditioning for amplifying and filtering the RF signal at 2.4-2.5GHz. The module contains the RF power amplifier and the low noise amplifier, with the necessary RF pre-selector filter.

The amplifier provides the necessary RF output power. Two identical RF sub-modules are implemented in the SMT349 module.

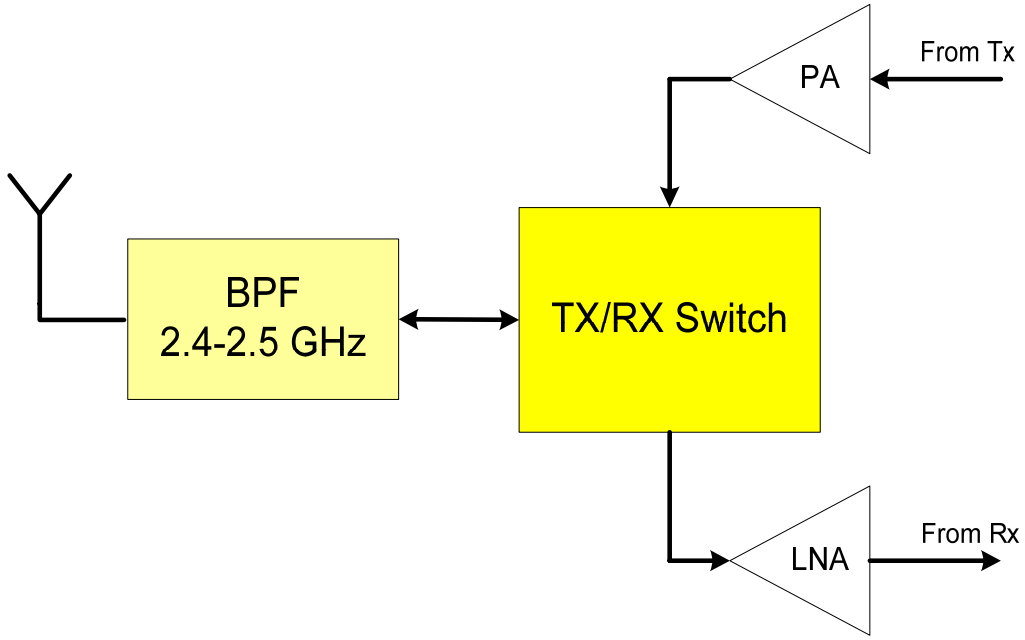

Figure 5: 2.4GHz RF sub-module

4.7 Technical specifications of the RF sub-module:

Tx Section

Linear Output power ..... 2mWatt minimum
Gain ..... 25dB minimum
Power OFF ..... 35dB minimum isolation

Rx Section

Noise Figure	3dB maximum
Input IP3	0dBm minimum
Maximum input, no damage	+20dBm, minimum
RF bandwidth	100MHz (1dB) or 150MHz (3dB)
RF rejection BW	15dB minimum @ -/+ 100MHz off band-edge. 25dB minimum @ -/+ 500MHz off band-edge

5 Timing module

5.1 Technical specifications of the timing module:

LO phase noise

At 1 kHz	-40dBc/Hz
At 10 kHz	-55dBc/Hz
At 100 kHz	-65dBc/Hz
At 300 Khz	-70dBc/Hz
At 1MHz	-80dBc/Hz

LO switching time	100nsec maximum to ±20ppm
Synthesizer minimum step	4 kHz

XO reference

Nominal frequency	10.0000MHz
Frequency accuracy	±2ppm over the temperature range

5.2 On-board reference crystal (standard SMT349)

The standard **SMT349** board comes with a 16-MHz on-board crystal (Rakon – IVT5300B) as a reference to the clock synthesizer.

5.3 External Reference (Option)

Optionally (**SMT349-EXTREF**), the on-board reference crystal can be replaced by an external reference using connector J18, in which case a signal of frequency within the range 2-50MHz and amplitude 0.2-3.3V can be applied to J18.

6 General specifications

6.1 Digital control specifications

RX-AGC - done using 2x31 dB att. 1dB resolution
(10 digital control bits, 5x2)
TX-AGC – done using 1x31 dB att. 1dB resolution
(5 digital control bits)
Frequency setting
(3 wires serial interface)
Switches and mode configuration Rx/Tx switch
(1 digital control bit)

6.2 Signal filtering performances of the SMT349:

70MHz BPF characteristics
-1dB ..... +/-8 MHz
-20dB BW ..... +/-12 MHz
-50dB BW ..... +/-15 MHz
Pass Band Ripple ..... 1dB maximum
Fix RF group delay variation ..... 100nSec maximum, any 1MHz band

IF BPF characteristics
-1dB BW ..... +/-8 MHz
-20dB BW ..... +/-20 MHz
-50dB BW ..... +/-30 MHz
Group Delay variation ..... 100nSec maximum
Ripple ..... 1dB maximum

7 Communication resources

It is strongly advised to read the Sundance help file to understand the principle of the Sundance communication resources and their connectivity principles.

7.1 Comports

The FPGA module has two comports, numbered 0 and 3. **The default firmware only implements CP3**

The addresses of the Comport registers are described in the SMT6400 help file . Control commands from the host are received via comports.

7.2 SHB

The SMT349 has two SHB connectors, both of which are connected to the FPGA to give 2x 16-bit SDB interfaces. These interfaces operate with a fixed clock rate of 100MHz.

SDB0 and SDB1 on the FPGA are presented on the TIM's SHB connectors, SHBA and SHBB respectively. The interface for these connectors is not implemented in the default firmware since it is not used for standard application.

7.3 LED

The SMT349 has 7 LEDs. LED5 displays the state of the FPGA DONE pin. This LED is off when the FPGA is configured (DONE=1) and on when it is not configured (DONE=0). This LED should go on when the board is first powered up and go off when the FPGA has been successfully programmed, using the contents of the on-board PROM. If the LED does not light at power-on, check that you have the mounting pillars and screws fitted properly. If it stays on, the DSP is not booting correctly, or is set to boot in a non-standard way.

There are 4 LEDs connected directly to the FPGA as standard IO. LED1 is flashing constantly (except when FPGA kept reset) at the on-board crystal rate (50MHz). LED2 ON means that the IF/RF clock synthesizer has successfully locked after being programmed. LED3 and LED4 are respectively address bits 1 and 0 of the last control word received.

Two LEDs (6 and 7) show that the power supplies of 3.3V and 5 are working.

7.4 Standard LVTTL IO pins

There are two set of pins (J17 and JX6) which are connected to the FPGA and can be accessed by the user. These pins are compliant with the LVTTL standard.

The default FPGA design provided routes the IF/RF clock synthesizer lock signal to pin5 of JX6 in order to be probed if necessary. A ‘1’ means the IF/RF clock synthesizer has locked successfully after being programmed.

7.5 FPGA

The SMT349 is populated with a Xilinx Virtex FPGA (*XC2V1000-4*). This device controls major functions on the module, like Comports communications, memory and clock management. SHB connectors can also be controlled through it, but they are not in the default software.

This FPGA requires configuration after power-up and after a module reset. This operation is possible due to the on-board Xilinx PROM. This operation can be done automatically when jumper JX2 is fitted. If JX2 is not fitted, the FPGA is not automatically loaded, and the JTAG interface may be used to program the FPGA without conflict.

The PROM is originally programmed with a default bit stream, which implements the features described in this document.

7.6 Memory

The *SMT349* is also populated with some NtSRAM memory. It is 32-bit wide and to store two 16-bit samples at the same address at up 160 MHz. Its size is 1

Megawords of 32-bits. The interface for this memory is not implemented in the default firmware since it is not used for standard application.

8 Application Development

Depending on the complexity of your application, you can develop code for SMT349 modules in several ways.

An application note on how to configure the FPGA can be downloaded from our website. On the SMT349, the FPGA is paired with a PROM. At power-up and on each TIM reset received by the module, the contents of the PROM is reloaded into the FPGA. The FPGA/PROM/JTAG connectors are identical to the SMT370 module. Please refer to the following link in case the SMT349 needs to be reprogrammed:

http://www.sundance.com/docs/SMT370%20Reprogramming.pdf

8.1 FPGA - SMT6500

This is the support package for the FPGA. It may be used to develop your application in the FPGA of the module.

- Troubleshooting

Our Knowledge data base and FAQ sections may help you to resolve some known issues.

At power-up, the FPGA is not configured and is waiting for a bitstream to be loaded. The default bitstream is stored into the PROM and it is loaded into the FPGA at power-up and after every TIM reset, provided that jumper J1 is fitted.

9 Operating Conditions

9.1 Safety

The module presents no hazard to the user.

9.2 EMC

The module is designed to operate within an enclosed host system that provides adequate EMC shielding. Operation within the EU EMC guidelines is only guaranteed when the module is installed within an appropriate host system.

The module is protected from damage by fast voltage transients introduced along output cables from outside the host system.

Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.

9.3 General Requirements

The module must be fixed to a TIM40-compliant carrier board.

The SMT349 TIM is in a range of modules that must be supplied with a 3.3V power source. In addition to the 5V supply specified in the TIM specification, these new generation modules require an additional 3.3V supply to be presented on the two diagonally-opposite TIM mounting holes. The lack of this 3.3V power supply should not damage the module, although it will obviously be inoperable; prolonged operation under these circumstances is not recommended. A 12V power rail is also required in order for the module to function properly.

The SMT349 is compatible with all Sundance TIM carrier boards. It is a 5V tolerant module, and as such, it may be used in mixed systems with older TIM modules, carrier boards and I/O modules.

The external ambient temperature must remain between 0°C and 40°C, and the relative humidity must not exceed 95% (non-condensing).

9.4 Power Consumption

The power consumption of this TIM is dependent on the operating conditions in terms of core activity and I/O activity. The maximum power consumption is 10W.

9.5 Weight

SMT349 weighs approximately 75 grams.

10 Board Photographs

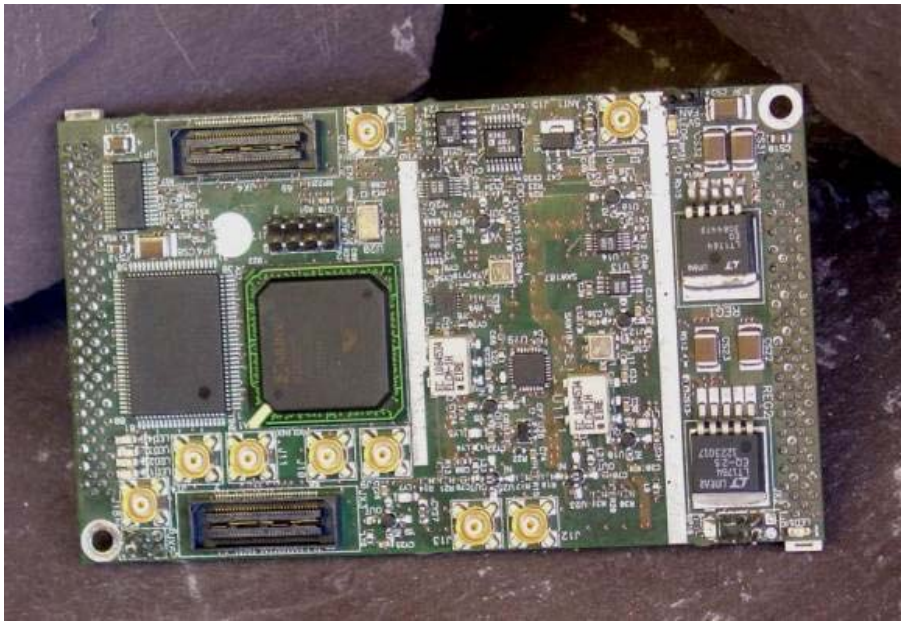

Figure 6 Top view

Figure 7 Bottom view

11 Connectors Location

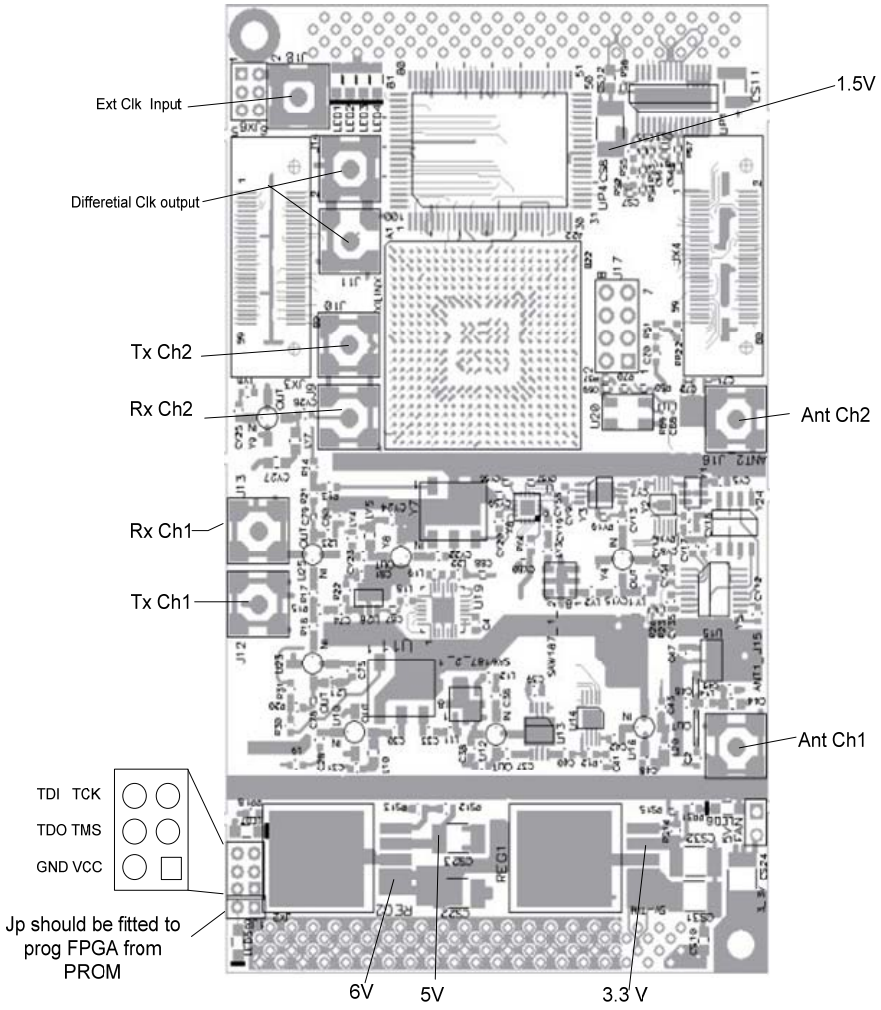

Figure 8 Connectors locationPROM and FPGA JTAG

The PROM and the FPGA appear in the same JTAG chain.

The following shows the pin-outs for JP (FPGA) JTAG connectors:

Signal	Pin	Pin	Signal
V33	1	2	GND
TMS	3	4	TDO
TCK	5	6	TDI

Table 1 JTAG programming connector

11.1 FPGA configuration

You can configure the FPGA by programming the PROM via the JTAG connector using for instance the Xilinx parallel cable IV.

12 Control Register Settings

The Control Registers control the complete functionality of the *SMT349*. They are set up via the Comport 3. The settings of the IF/RF synthesizer, attenuators and RF switches can be configured via the Control Registers.

12.1 Control Packet Structure

The data passed on to the *SMT349* over the Comport must conform to a certain packet structure. Only valid packets will be accepted and only after acceptance of a packet will the appropriate settings be implemented. Each packet will start with a command (4 bits – 0x1 for a write operation – 0x2 for a read operation) information, followed by a register address (8 bits), followed by a 20-bit data. This structure is illustrated in the following figure:

	Byte Content							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
3	Command 3	Command 2	Command 1	Command 0	Address 7	Address 6	Address 5	Address 4
2	Address 3	Address 2	Address 1	Address 0	Data 19	Data 18	Data 17	Data 16
1	Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0

Table 2- Setup Packet Structure

12.2 Reading and Writing Registers

Control packets are sent to the *SMT349* over Comport 3. This is a bi-directional interface. The format of a ‘Read Packet’ is the same as that of a write packet.

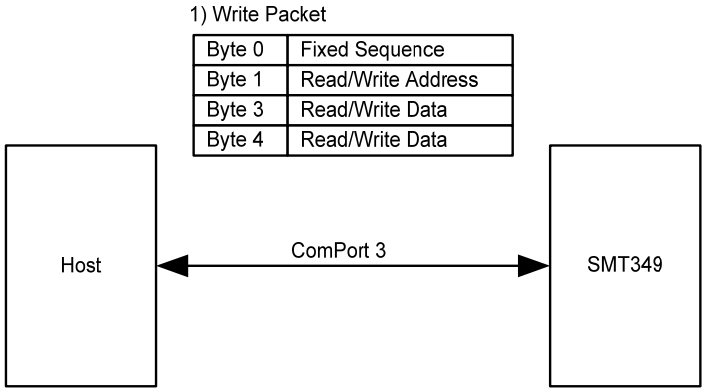

Figure 9 – Control Register Read Sequence.

12.3 Memory Map

The write packets must contain the address where the data must be written to and the read packets must contain the address where the required data must be read. The following figure shows the memory map for the writable and readable Control Registers on the *SMT349:*

Address	Writable Registers	Readable Registers
0x00	Reset Register.	Status Register.
0x01	Transceiver1 Register (0x0).	Read-Back Transceiver1 Register (0x0).
0x02	Transceiver2 Register (0x1).	Read-Back Transceiver2 Register (0x1).
0x03	IF/RF Synthesizer Reg 0x0	Read-Back IF/RF Synthesizer Reg 0x0
0x04	IF/RF Synthesizer Reg 0x1	Read-Back IF/RF Synthesizer Reg 0x1
0x05	IF/RF Synthesizer Reg 0x2	Read-Back IF/RF Synthesizer Reg 0x2
0x06	IF/RF Synthesizer Reg 0x3	Read-Back IF/RF Synthesizer Reg 0x3
0x07	IF/RF Synthesizer Reg 0x4	Read-Back IF/RF Synthesizer Reg 0x4
0x08	IF/RF Synthesizer Reg 0x5	Read-Back IF/RF Synthesizer Reg 0x5
0x09	IF/RF Synthesizer Reg 0x6	Read-Back IF/RF Synthesizer Reg 0x6
0x0A	IF/RF Synthesizer Reg 0x7	Read-Back IF/RF Synthesizer Reg 0x7
0x0B	IF/RF Synthesizer Reg 0x8	Read-Back IF/RF Synthesizer Reg 0x8
0x0C	Reserved	Reserved
0x0D	Register Update	Reserved
0x0E	Reserved	Reserved
0x0F	Reserved	Reserved

Table 3 Memory map

12.4 Register Descriptions

12.4.1 Reset Register – 0x0.

	Reset Register (Write) – 0x0							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Auto-retune	RF/IF Synthesizer
Default	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'1'

	Reset Register – 0x0	
Setting	**Bit 0**	**Description**
0	0	RF/IF Synthesizer working in normal mode.
1	1	RF/IF Synthesizer working powered down.

	Reset Register – 0x0	
Setting	**Bit 1**	**Description**
0	0	Auto-retune function off.
1	1	Auto-retune function on – Forces the IF/RF clock synthesizer in case of the loss of the lock signal.

Note: The Reset bits don't get cleared automatically, so a device can remain reset while not used to reduce the global power consumption.

	Reset Register (Read-Back) – 0x0							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RF/IF Synthesizer AUXSEL
Default	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'1'

	Reset Register – 0x0	
Setting	**Bit 0**	**Description**
		See below for selection among Clock Synthesizer Internal Registers. AUXSEL (Bits 12 and 12 - IF/RF Synthesizer Register 0 – 0x03)

12.4.2 Transceiver1 Register – 0x1.

Any value written in this register can be read-back to check that the Comport used works properly.

	Transceiver1 Register – 0x1							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved						Tx/Rx Switch	
Default	Reserved						‘00’	
1	Reserved	Attenuation Receiver RF					Attenuation Receiver IF	
Default	‘0’	‘11111’					‘11’	
0	Attenuation Receiver IF			Attenuation Transmitter				
Default	‘111’			‘11111’				

	Transceiver1 Register – 0x1
Setting **Bit14…10 (Rx/RF)** **Bit9…5 (Rx/IF)** **Bit4…0 (Tx)**	**Attenuation (Receiver RF/IF and Transmitter)**
‘00000’	No attenuation (Min).
‘00001’	1 dB attenuation.
‘00010’	2 dB attenuation.
…	…
‘11111’	31 dB attenuation (Max).

	Transceiver1 Register – 0x0
Setting TX/Rx Switch **Bit17…16**	**Tx/Rx Switch**
‘11’	Tx and Rx OFF
‘10’	Tx ON and Rx OFF
‘01’	Tx OFF and Rx ON
‘00’	Tx and Rx OFF

Attenuations (Receiver IR/RF and Transmitter) are coded on 5 bits (binary).

12.4.3 Transceiver2 Register – 0x2.

Any value written in this register can be read-back to check that the Comport used works properly.

	Transceiver2 Register – 0x2							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved						Tx/Rx Switch	
Default	Reserved						‘00’	
1	Reserved	Attenuation Receiver RF					Attenuation Receiver IF	
Default	‘0’	‘11111’					‘11’	
0	Attenuation Receiver IF			Attenuation Transmitter				
Default	‘111’			‘11111’				

	Transceiver2 Register – 0x2
Setting **Bit14…10 (Rx/RF)** **Bit9…5 (Rx/IF)** **Bit4…0 (Tx)**	**Attenuation (Receiver RF/IF and Transmitter)**
‘00000’	No attenuation (Min).
‘00001’	1 dB attenuation.
‘00010’	2 dB attenuation.
…	…
‘11111’	31 dB attenuation (Max).

	Transceiver2 Register – 0x2
Setting **TX/Rx Switch** **Bit17…16**	**Tx/Rx Switch**
‘11’	Tx and Rx OFF
‘10’	Tx ON and Rx OFF
‘01’	Tx OFF and Rx ON
‘00’	Tx and Rx OFF

Both Attenuations (Receiver and Transmitter) are coded on 5 bits (binary).

12.4.4 IF/RF Synthesizer Register 0 – 0x3.

For more details, refer to Si4136 datasheet.

	IF/RF Synthesizer Register 0 – 0x03							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved	Reserved	AUXSEL		IFDIV		Reserved	Reserved
Default	'0'	'0'	'00'		'00'		'0'	'0'
0	Reserved	XIN DIV2	LPWR	Reserved	Auto PDB	Reserved	Reserved	Reserved
Default	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

	IF/RF Synthesizer Register 0 – 0x03	
Setting	**Bit 3**	**Description – Auto PDB (Auto power Down)**
0	0	Software powerdown is controlled by IF/RF Synthesizer Register 2.
1	1	Equivalent to setting all bits in IF/RF Synthesizer Register 2 to '1'.

	IF/RF Synthesizer Register 0 – 0x03	
Setting	**Bit 5**	**Description – LPWR (Power level for IF Synthesizer Circuit)**
0	0	Rload < 500 Ohms – Normal Power Mode.
1	1	Rload > 500 Ohms – Low Power Mode.

	IF/RF Synthesizer Register 0 – 0x03	
Setting	**Bit 6**	**Description – XIN DIV2 (Divide by 2 Mode)**
0	0	Xin not divided by 2.
1	1	Xin divided by 2.

	IF/RF Synthesizer Register 0 – 0x03	
Setting	**Bit 11&10**	**Description – IFDIV (IF output divider)**
0	'00'	IFout = IFvco frequency.
1	'01'	IFout = IFvco frequency/2.
2	'10	IFout = IFvco frequency/4.
3	'11'	IFout = IFvco frequency/8.

	IF/RF Synthesizer Register 0 – 0x03	
Setting	**Bit 13&12**	**Description – AUXSEL (Auxiliary Output Pin Definition)**
0	'00'	Reserved.
1	'01'	Force Output Low.
2	'10	Reserved.
3	'11'	Lock Detect (LDETB).

12.4.5 IF/RF Synthesizer Register 1 – 0x4.

For more details, refer to Si4136 datasheet.

	IF/RF Synthesizer Register 1 – 0x04							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved							
Default	'00000000'							
0	Reserved		Kpl		Kp2		Kp1	
Default	'00'		'00'		'00'		'00'	

	IF/RF Synthesizer Register 1 – 0x04	
Setting	**Bit 1&0**	**Description – Kp1 (RF1 Phase Detector Gain Constant)**
0	'00'	N Value < 4096.
1	'01'	N Value between 4096 and 8191.
2	'10'	N Value between 8192 and 16383.
3	'11'	N Value > 16383.

	IF/RF Synthesizer Register 1 – 0x04	
Setting	**Bit 3&2**	**Description – Kp2 (RF2 Phase Detector Gain Constant)**
0	'00'	N Value < 2048.
1	'01'	N Value between 2048 and 4095.
2	'10'	N Value between 4096 and 8191.
3	'11'	N Value > 8191.

	IF/RF Synthesizer Register 1 – 0x04	
Setting	**Bit 5&4**	**Description – Kpl (IF Phase Detector Gain Constant)**
0	'00'	N Value < 2048.
1	'01'	N Value between 2048 and 4095.
2	'10'	N Value between 4096 and 8191.
3	'11'	N Value > 8191.

12.4.6 IF/RF Synthesizer Register 2 – 0x5.

For more details, refer to Si4136 datasheet.

	IF/RF Synthesizer Register 2 – 0x05							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved							
Default	'00000000'							
0	Reserved						PDIB	PDRB
Default	'000000'						'0'	'0'

	IF/RF Synthesizer Register 2 – 0x05	
Setting	**Bit 0**	**Description – PDRB (Powerdown RF Synthesizer)**
0	'0'	RF Synthesizer powered down.
1	'1'	RF Synthesizer on.

Setting	**Bit 1**	**Description – PDIB (Powerdown IF Synthesizer)**
0	'0'	IF Synthesizer powered down.
1	'1'	IF Synthesizer on.

12.4.7 IF/RF Synthesizer Register 3 – 0x6.

For more details, refer to Si4136 datasheet.

	IF/RF Synthesizer Register 3 – 0x06							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved						NRF1	
Default	Reserved						'0'	
1	NRF1							
Default	'00000000'							
0	NRF1							
Default	'00000000'							

	IF/RF Synthesizer Register 3 – 0x06	
Setting	**Bit 17…0**	**Description – NRF1 (N Divider for RF1 Synthesizer)**
0		NRF1 > 992

12.4.8 IF/RF Synthesizer Register 4 – 0x7.

For more details, refer to Si4136 datasheet.

	IF/RF Synthesizer Register 4 – 0x07							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved							NRF2
Default	Reserved							'0'
1	NRF2							
Default	'00000000'							
0	NRF2							
Default	'00000000'							

	IF/RF Synthesizer Register 4 – 0x06	
Setting	**Bit 16…0**	**Description – NRF2 (N Divider for RF2 Synthesizer)**
0		NRF2 > 240

12.4.9 IF/RF Synthesizer Register 5 – 0x8.

For more details, refer to Si4136 datasheet.

	IF/RF Synthesizer Register 5 – 0x08							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	NIF							
Default	'00000000'							
0	NIF							
Default	'00000000'							

	IF/RF Synthesizer Register 5 – 0x08	
Setting	**Bit 16…0**	**Description – NIF (N Divider for IF Synthesizer)**
0		NRF2 > 56

12.4.10 IF/RF Synthesizer Register 6 – 0x9.

For more details, refer to Si4136 datasheet.

	IF/RF Synthesizer Register 6 – 0x09							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved			RRF1				
Default	'000'			'00000'				
0	RRF1							
Default	'00000000'							

	IF/RF Synthesizer Register 6 – 0x09	
Setting	**Bit 12…0**	**Description – RRF1 (R Divider for RF1 Synthesizer)**
0		RRF1 : 7 to 8189 if Kp1 = ‘00’ 8 to 8189 if Kp1 = ‘01’ 10 to 8189 if Kp1 = ‘10’ 14 to 8189 if Kp1 = ‘11’

12.4.11 IF/RF Synthesizer Register 7 – 0xA.

For more details, refer to Si4136 datasheet.

	IF/RF Synthesizer Register 7 – 0x0A							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved			RRF2				
Default	‘000’			‘00000’				
0	RRF2							
Default	‘00000000’							

	IF/RF Synthesizer Register 7 – 0x0A	
Setting	**Bit 12…0**	**Description – RRF2 (R Divider for RF2 Synthesizer)**
0		RRF2 : 7 to 8189 if Kp2 = ‘00’ 8 to 8189 if Kp2 = ‘01’ 10 to 8189 if Kp2 = ‘10’ 14 to 8189 if Kp2 = ‘11’

12.4.12 IF/RF Synthesizer Register 8 – 0xB.

For more details, refer to Si4136 datasheet.

	IF/RF Synthesizer Register 8 – 0x0B							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved			RIF				
Default	'000'			'00000'				
0	RIF							
Default	'00000000'							

	IF/RF Synthesizer Register 8 – 0x0B	
Setting	**Bit 12…0**	**Description – RIF (R Divider for IF Synthesizer)**
0		RIF : 7 to 8189 if Kpl = '00' 8 to 8189 if Kpl = '01' 10 to 8189 if Kpl = '10' 14 to 8189 if Kpl = '11'

12.4.13 Update Register – 0xD.

	Update Register – 0xD							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved						Reserved	RF/IF Synthesizer Update
Default	'000000'							'0'

	Update Register – 0xD	
Setting	**Bit 0**	**Description**
0	0	Normal Mode.
1	1	Loads RF/IF Registers into the Synthesizer.

Note: The Update bits get cleared automatically.

Default	'00000000'

12.4.14 LEDs.

There are 4 LEDS on the SMT349. Here are how they are used within the standard firmware:

LED0: Flashing on the on-board crystal. Should start flashing as soon as the FPGA is configured with standard formware

LED1: AuxBit from the IF/RF device. ON means that the synthesizer has locked.

LED2: Connected to bit0 of register address.

LED3: Connected to bit1 of register address.

13 Application Example

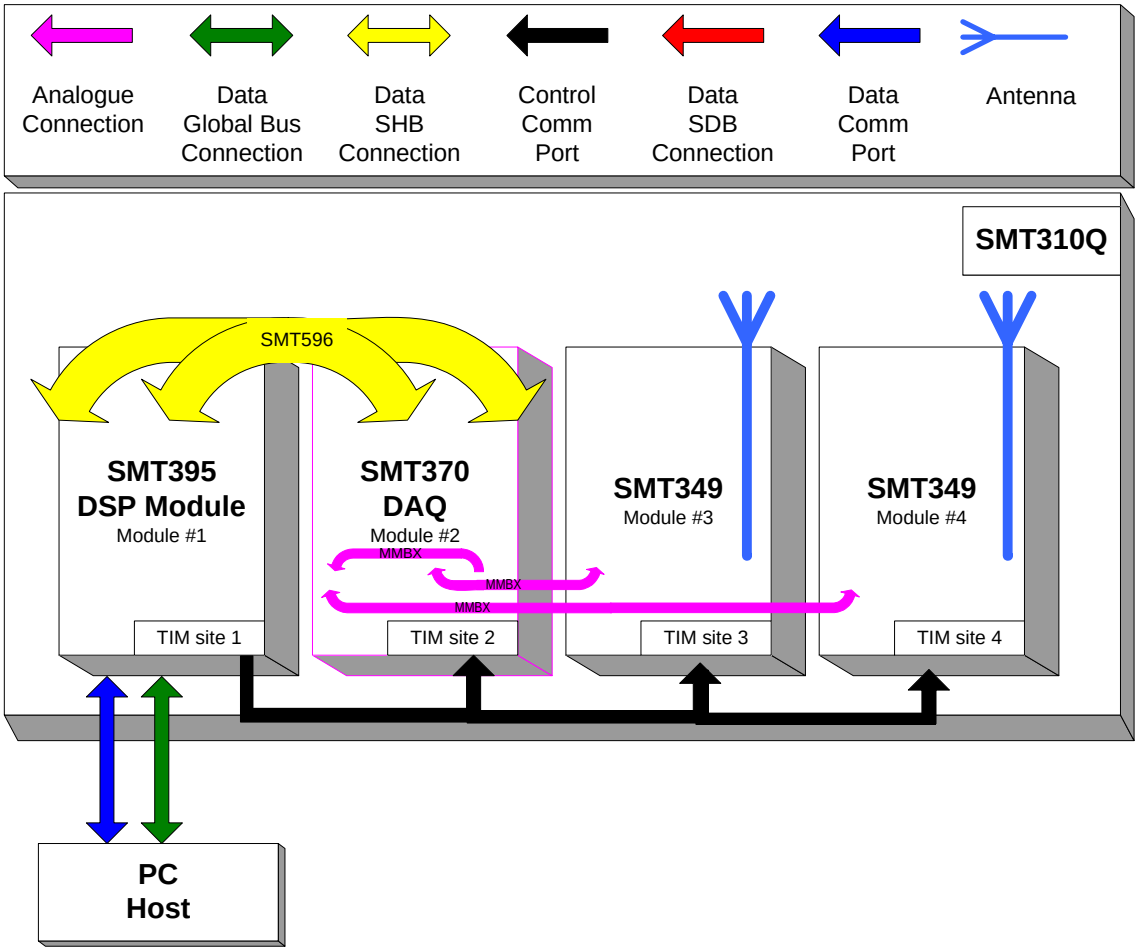

Figure 6 System example

The diagram shows an example of a system where an SMT310Q carrier board has four modules plugged on it. The first module, SMT395 will be controlling the data from/to the second module SMT370 via SHB connectors. The host application will configure the SMT370 to generate a pattern of 16MHz sinusoidal signal sampled at 54 MHz such that a replica centred around 70MHz is also generated. (similar case as the one shown in to figure 3). This signal is sent via MMBX-MMBX coaxial cable to one of the SMT349s configured as transmitter. The last module, configured as receiver, will pass the received signal back to the SMT370 via another MMBX-MMBX coaxial cable and from there to the host through the SMT395.

14 Ordering Information

The standard SMT349 board comes with a 16-MHz on-board crystal (Rakon – IVT5300B) as a reference to the clock synthesizer.

It is also possible to use an external reference clock (2-50 MHz) but it has to be specified when ordering the board as it requires some extra circuitry to be populated.

It is one option (on-board crystal) or the other (external reference).

SMT349 : on-board reference (standard product).

SMT349-EXTREF : external reference via MMBX connector.

15 Bibliography

1. Sundance Help file
2. SMT6400 help file (DSP support package) and SMT6500 help file (FPGA support package)
3. TIM-40 MODULE SPECIFICATION Including TMS320C44 Addendum
4. SDB Technical Specification
5. SHB Technical Specification
6. Xilinx Virtex-II datasheet