Unit / Module Description:	FPGA TIM with DDR memory
Unit / Module Number:	SMT351T
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Product Specification for SMT351T

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Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	12/9/06	GKP
1.1	General update.	2/11/06	GKP
1.2	Update with larger Virtex 5.	21/2/07	GKP
1.3	Updated RSL section.	25/4/07	GKP
1.4	Updated block diagram. Added ordering info and options.	12/7/07	GKP
1.4.1	Title corrected.	20/8/07	GKP
1.4.2	Corrected DDR rate to 250MHz.	11/9/07	GKP

Table of Contents

1 Introduction

The SMT351T is a Virtex 5 based TIM.

Using a Xilinx Virtex 5 device in an FF1136 package, the following interfaces can be provided;

- Two 64-bit wide data banks of DDR2 memory. Each bank using 4 x 2Gbit devices from Micron (1Gbit parts can be used), thus providing 1Gbytes per bank. Running this memory at 250MHz provides a maximum access speed of 4Gbyte/s per bank.
- Sundance SLB bus. This provides LVDS and LVTTL parallel interfaces which will accept a range of Sundance SLB mezzanine modules (ADC, DAC, etc).
- Sundance RSL serial interfaces (up to 16).

2 Related Documents

Sundance SLB specification (hyperlink).

Sundance RSL specification (hyperlink).

Xilinx Virtex5 datasheets (hyperlink).

3 Acronyms, Abbreviations and Definitions

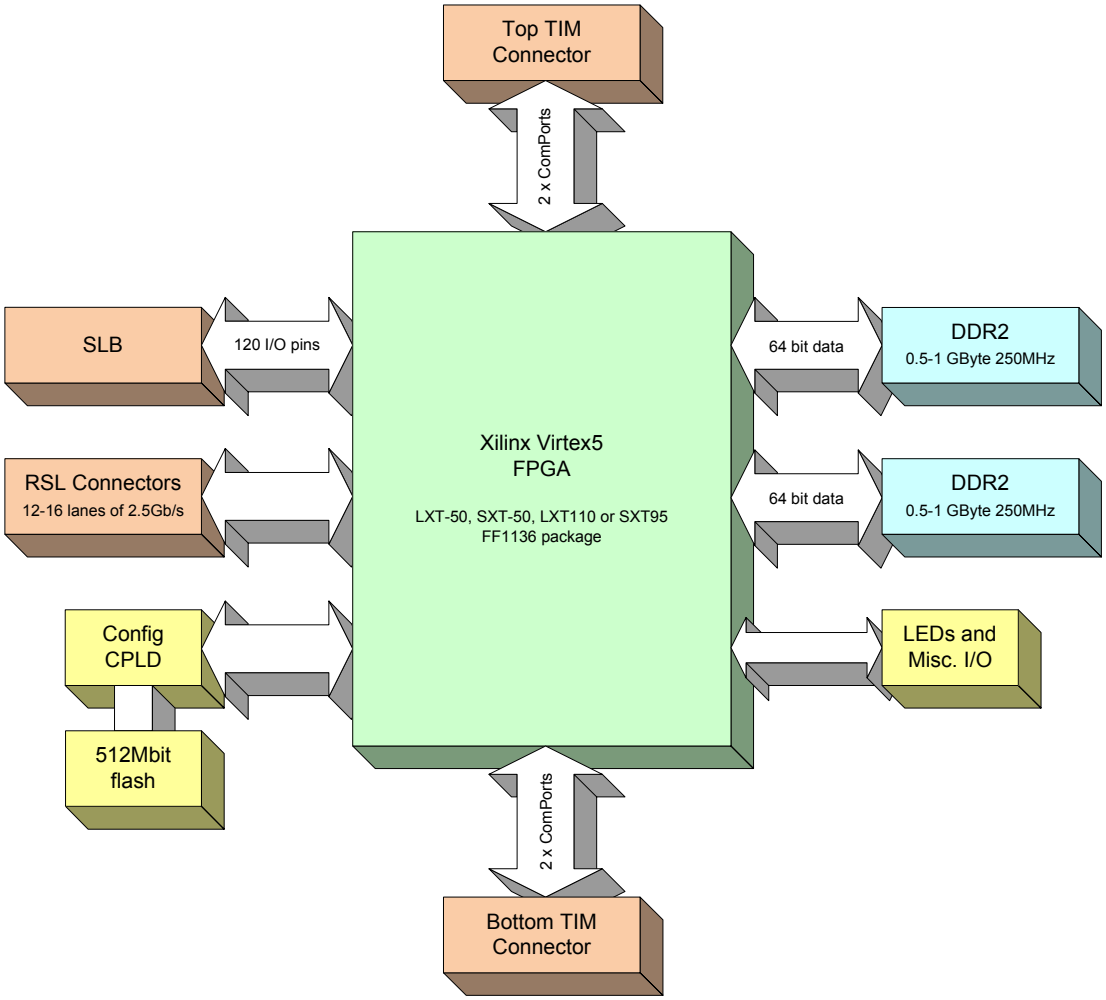
A list of acronyms etc (hyperlink).

RSL, MGT and GTP are used interchangeably within this document.

4 Functional Description

The major elements of the SMT351T are shown in the block diagram below.

4.1 Block Diagram



4.2 Module Description

4.2.1 FPGA

The SMT351T module uses a Xilinx Virtex 5 LXT or SXT to implement the interfaces the board provides.

Any of the devices available in the FF1136 package may be used, but only the LX110T and SX95T provide all 16 MGTs.

Configuration of the FPGA is from one of two sources; on-board flash memory or data from a ComPort using the CPLD.

4.2.2 DDR2

Four devices per bank are used to implement this memory. Each bank is fully and independently connected to the FPGA.

A 250MHz 64-bit data bus is used to transfer data at 4Gbyte/s.

4.2.3 SLB

This connector provides 4 8-bit LVDS interfaces, or 2 16-bit LVDS interfaces. Each 16-bit interface has independent differential clocks, triggers and control.

Several other differential triggers and enables are provided, and 21 LVTTL pins are also available.

4.2.4 RSL

The LXT series devices from Xilinx provide up to 16 high speed (>3Gbps) serial links.

The SMT351T incorporates 4 RSL connectors each providing 4 RSL links.

Two RSL connectors are mounted on the top of the module, and two on the underside.

The LX50T and SX50T FPGAs do not provide all 16 RSL links. Only two RSL links on each of the top mounted RSL connectors are provided when using these FPGAs.

4.2.5 Flash

This memory contains configuration code for the FPGA.

4.2.6 CPLD

The Xilinx CPLD is connected to ComPorts 0 and 3. It is capable of configuring the FPGA using data provided on these ComPorts or using data from the flash memory.

4.2.7 ComPorts

ComPorts 0, 1, 3 and 4 are connected to the FPGA.

ComPorts 2 and 5 are looped together.

5 Verification, Review & Validation Procedures

To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

6 Timing Diagrams

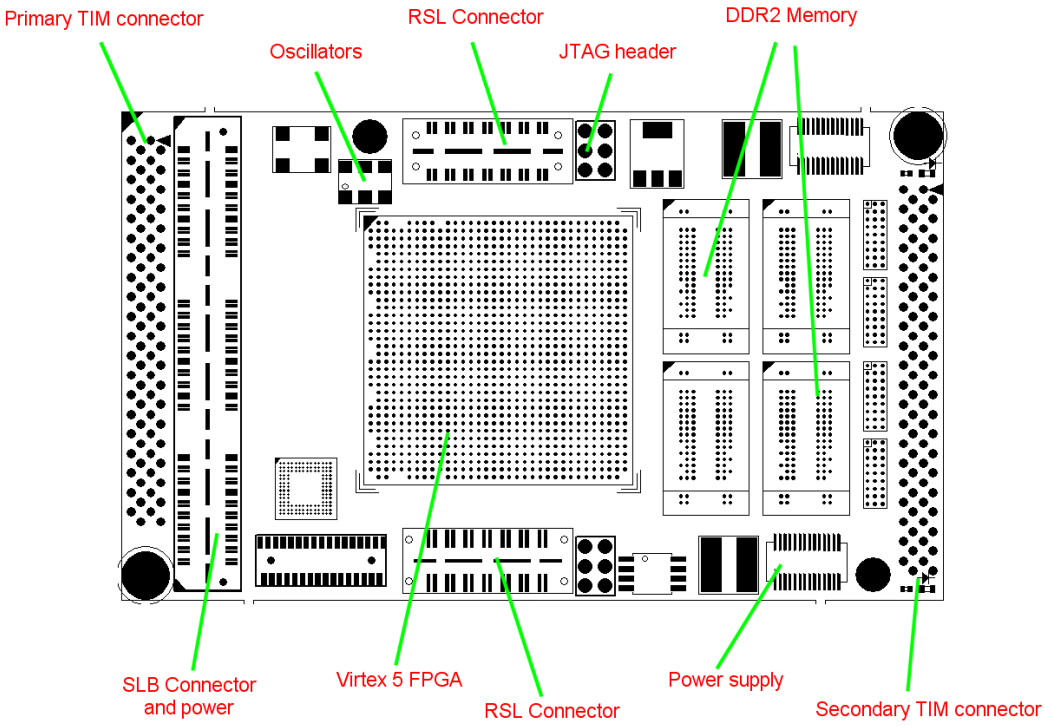
7 Circuit Description / Diagrams

8 FPGA Pin Allocation

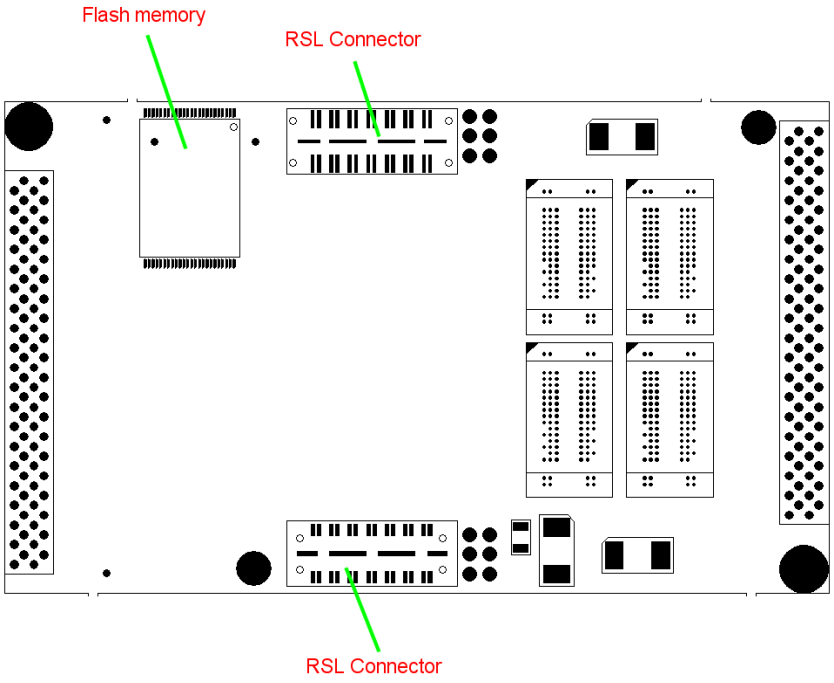
Sub-system	Pin name	Pin count	Instances	Sub-total	Total
SLB	Data	64	1		109
	Control	21			
	Clocks	16			
	Misc	8			
Comm ports	Data	8	4	32	48
	Control	4		16	
Clock	All	1	2	2	2
PXI	Clock	1	1	1	5
	Trig	4		4	
DDR	Data	64	2	64	204
	Address	19		38	
	Control	21		42	
	Misc	4		8	
TTL & LEDs	All	8	1	8	8
TIM Interrupts	NMI/IACK/IIOF	6	1	4	4
TIM timers	TCLK	2	1	2	2
TIM reset	RESET	1	1	1	1
TIM C4x	CONFIG	1	1	1	1
CPLD	All	16	1	16	16

9 Footprint

9.1 Top View



9.2 Bottom View



10 FPGA Pinout

11 Support Packages

12 Physical Properties

Dimensions	4.2”	2.5”

Weight	

Voltage	Current
+12V	0
+5V	SLB supply only.
+3.3V	6A estimated
-5V	0
-12V	0

MTBF	

13 Safety

This module presents no hazard to the user when in normal use.

14 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

15 Ordering Information

Four variations of this product are available.

SMT351T-LX50-x-1	Fitted with an XC5VLX50T and 1Gbyte of memory.
SMT351T-LX110-x-2	Fitted with an XC5VLX110T and 2Gbytes of memory.
SMT351T-SX50-x-1	Fitted with an XC5VSX50T and 1Gbyte of memory.
SMT351T-SX95-x-2	Fitted with an XC5VSX95T and 2Gbytes of memory.

x represents the FPGA speed grade.

Note that the LX50 and SX50 options only provide 12 RSL links. See RSL section for more details.