SUNDANCE

SMT358

User Manual

Certificate Number FM 55022

Revision History

Date	Comments	Engineer	Version
10 Feb 1999	Initial Release	E.Puillet	Version1.0
20 Sept 1999	Overall update to SMT358 User Manual	E.Puillet	Version1.1
12 Oct 1999	SDB connector Pins renamed. Addition of Global Clock Buffer signal assignments	E.Puillet	Version1.2
08 Nov 1999	Modification of the FSM for the FPGA Reconfiguration.	E.Puillet	Version 1.3
22 Nov 1999	Addition of TIM Connectors and mounting holes' position	E.Puillet	Version 1.4
08 Dec 1999	Clarification of the FSM and explanations for the FPGA Configuration and Reconfiguration.	E.Puillet	Version 1.5
07 Jan 2000	SDB bi-directional clock drawing in Figure 4 corrected	E.Puillet	Version 1.6
28 Jan 2000	SDB Connector Pins correspondence between SMT373 and SDB standard.	E.Puillet	Version 1.7
15 Feb 2000	Description of the Installation and configuration of the SMT358	E.Puillet	Version 1.8
07 March 2000	Addition of a WARNING for customers with SMT358 boards delivered before 07.03.00.	E.Puillet	Version 2.0
22 March 2000	Addition of the memory addressing scheme for a memory Bank.	E.Puillet	Version 2.1
20 July 2000	Figure 3 modification of SDB bi-directional signal number for SDB C and D	E.Puillet	Version 2.2
26 October 2000	Table 3 is modified and becomes Table 1.General modifications to adapt the User Manual to VirtexE	E.Puillet	Version 2.3
06 January 2001	Table 1 is modified to remove parts, which won't be fitted on SMT358. Addition of new conversion software.	E.Puillet	Version 2.4
23 January 2001	Addition of power consumption considerations for the SMT358	E.Puillet	Version 2.5

The FPGARESET signal must be tied to ground in any FPGA design for SMT358s received before 07.03.00.

SMT358s received after 07.03.00 see the FPGA constraint file modified for Comm-Port 3 and any FPGA design must use the FPGARESET signal as a global reset active low.

Table of Contents

LIST OF FIGURES

LIST OF TABLES

Scope

This document describes the architecture, the function, the use and the interface considerations for the SMT358. This document is intended for both the users of the SMT358 and the designer who is interested in designing the FPGA provided on the Board.

SMT358 Versions

The SMT358 comes under 4 standard versions, highlighted in red in Table 1. A Virtex or Virtex E is fitted and the ZBTSRAM is in the pipelined version.

The total amount of memory on the board is either 4 MBytes or 8 Mbytes or 16 Mbyte.

Depending on the amount of on-board memory required, the Virtex/E fitted on-board, the SMT358 can be implemented in 18 subversions, which can be adapted to a wide range of application needs and costs.

Other configurations are possible depending on the speed of the application, as shown in Table 2 and Table 3.

Table 1 summarises the various board configurations offered.

SMT358					
	Virtex/E	**XCV400**	**XCV600**	**XCV800**	**XCV1000E**
ZBT SRAM					
4MBytes		SMT358-400-4	SMT358-600-4	SMT358-800-4	SMT358-1000E-4
8 MBytes		SMT358-400-8	SMT358-600-8	SMT358-800-8	SMT358-1000E-8
16 MBytes		SMT358-400-16	SMT358-600-16	SMT358-800-16	SMT358-1000E-16

Table 1: Virtex/E-ZBT SRAM Combinations

SMT358 Power consumption Considerations

The SMT358 power consumption is mostly dependant on the Virtex fitted and its usage.

When using a SMT3581000E, sufficient cooling is provided on-board for the voltage regulator and for the Virtex 1000E, nevertheless a correct airflow MUST prevail in your PC.

The larger and the faster the Virtex FPGA design is, the higher the Virtex power consumption is.

For example, considering a shift register using 50% of the LUTs of a Virtex 1000E at 100 Mhz with data toggling at every clock cycle will have the effect of drawing more current than the voltage regulator can provide and will make the voltage regulator fail (safely) and the FPGA will loose its configuration.

Therefore, we advice customers to use Xilinx power estimator to determine the worst-case power consumption of their design AND to consult.

The Excel program can be found at:

http://support.xilinx.com/support/techsup/powerest/virtex_power_estimator_v15.xls

The user guide on how to use this program can be found at:

http://support.xilinx.com/xapp/xapp152.pdf

Technical description

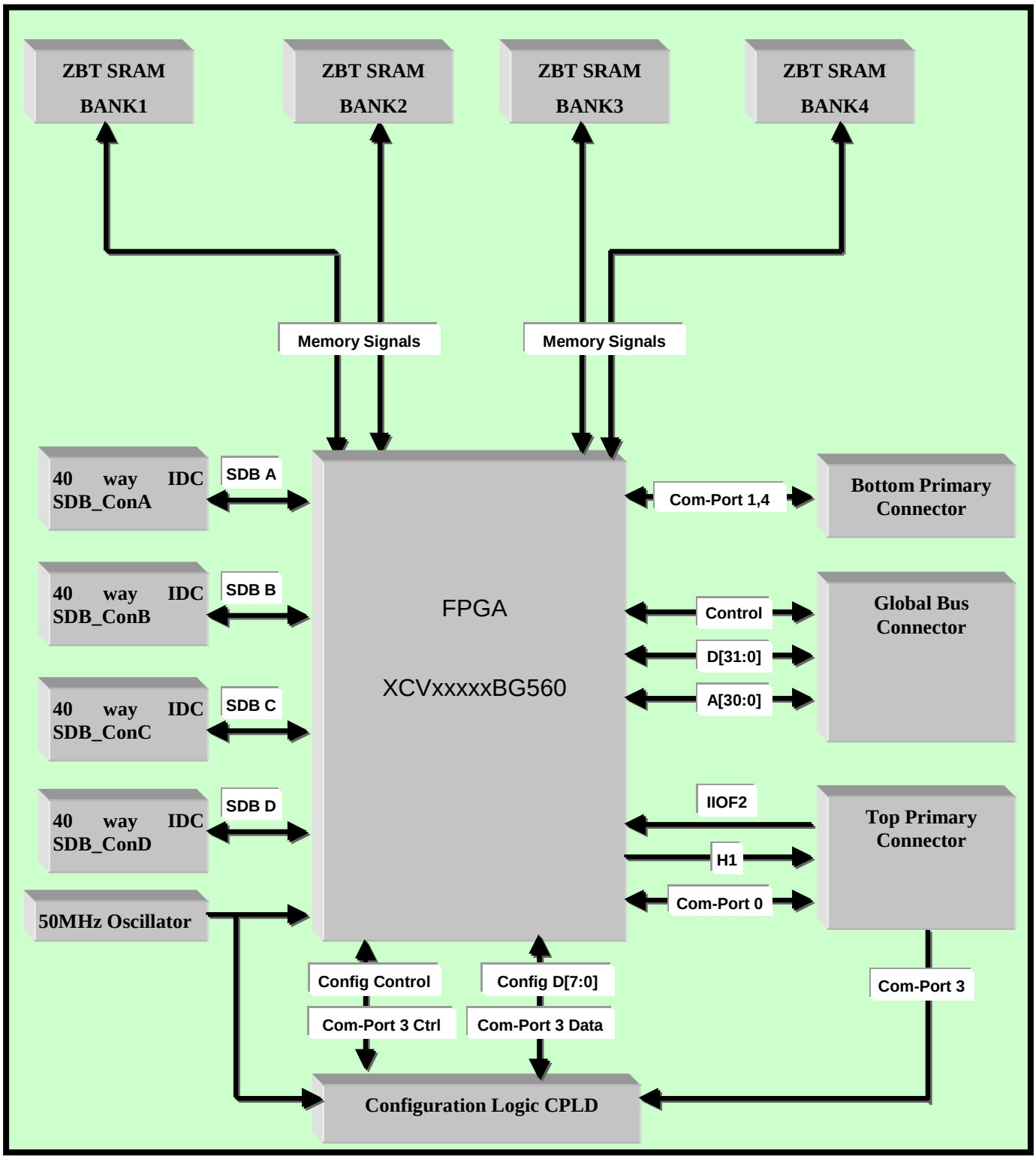


Figure 1: SMT358 Block diagram

Figure 1 shows the block diagram of the SMT358 I/O module. The following section describes the SMT358 from a user's point of view. Reference is made to the different blocks of Figure 1 in the next Figures.

On-board SRAM

The SMT358 provides the user with pipelined or Flowthrough ZBT (Zero Bus Turnaround) SRAM from Micron. Therefore this type of SRAM is optimised for a 100 percent bus utilisation eliminating any cycle when transitioning from READ to WRITE or vice versa. Three Chip Enables allow easy depth expansion so that the SMT358 total amount of memory can vary from 4 MBytes up to 16 MBytes.

Micron 4,8 or 16 Mbit ZBTSRAM have compatible inputs and outputs. FPGA designers can find the general description and a Pin description in the latest data sheets on Micron's Web Site at http://www.micron.com/mti/msp/html/zbtds.html

The on-board memory is divided into four banks (bank 1 to 4) accessible on a 72-bit bus (4 18-bit busses) and can be run at frequencies up to 166Mhz and.

Each of the 4 SRAM banks is independently accessible (Control, Data and Address are independent for every bank) and share the same Clock signal. To ensure high performance, the clock signal can be de-skewed inside the FPGA using DLLs as reproduced in Figure 2. As a result, a high-speed de-skewed clock drives the controller inside the FPGA and the ZBT SRAM.

The Virtex provides four programmable DLLs to produce waveforms with a wide range of frequencies and duty cycles.

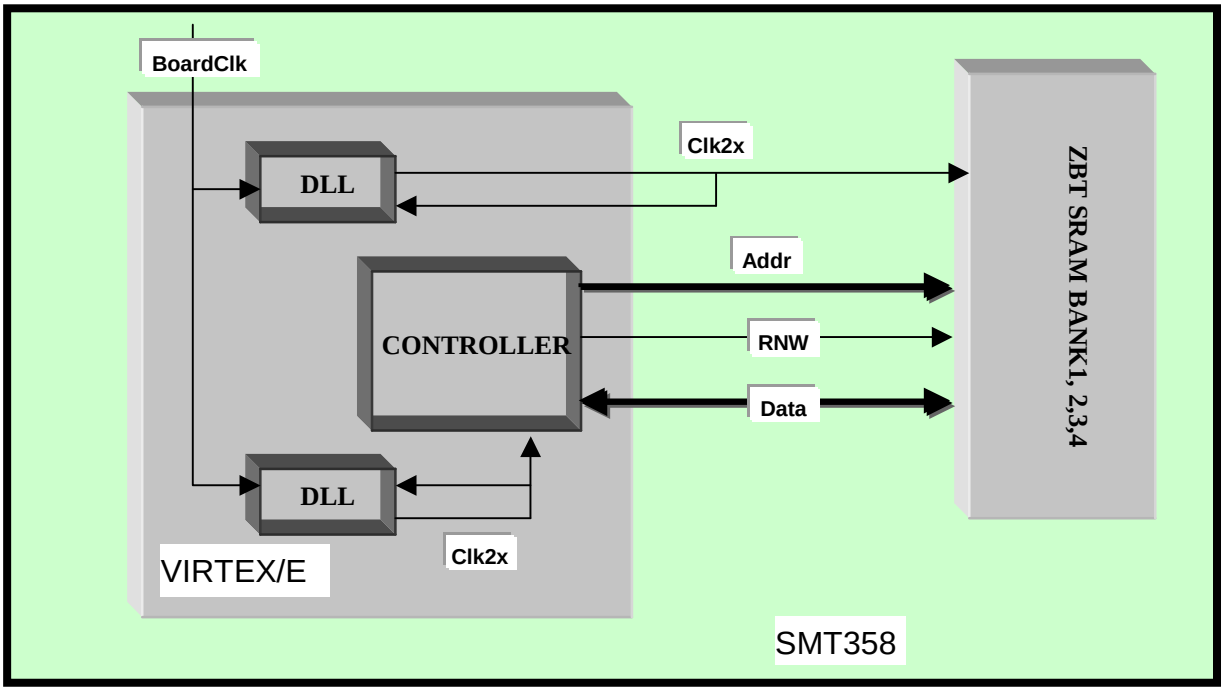


Figure 2: ZBT SRAM Clock signal

A simple Virtex/E interface to ZBTSRAM is provided by Xilinx and is described in Xilinx's Application Note: xapp136.

The on-board SRAM can be extended of another 8Mword bank present on a Mezzanine card which connects on two of the four SMT358 SDB connectors shown in Figure 3.

Figure 3 is a detailed view of the memory signal connections to the FPGA.

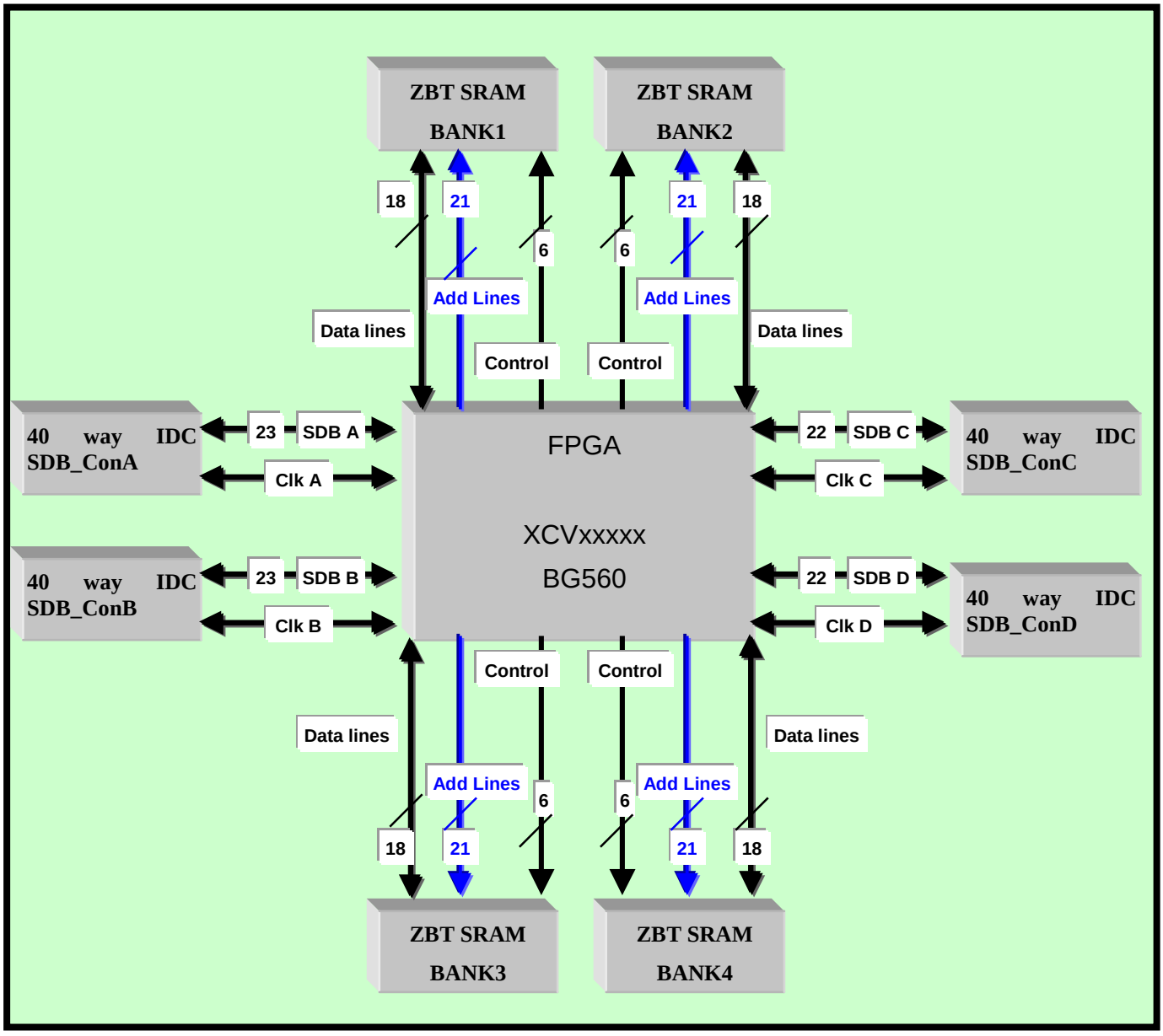


Figure 3: FPGA, Memory and SDB Communication Channels

As shown in Figure 4 each ZBTSRAM Bank is composed of a Low Bank and a High Bank which are selected by Address[20].

- Addr[20] = 0 selects the Low bank
- Addr[20] = 1 selects the High bank

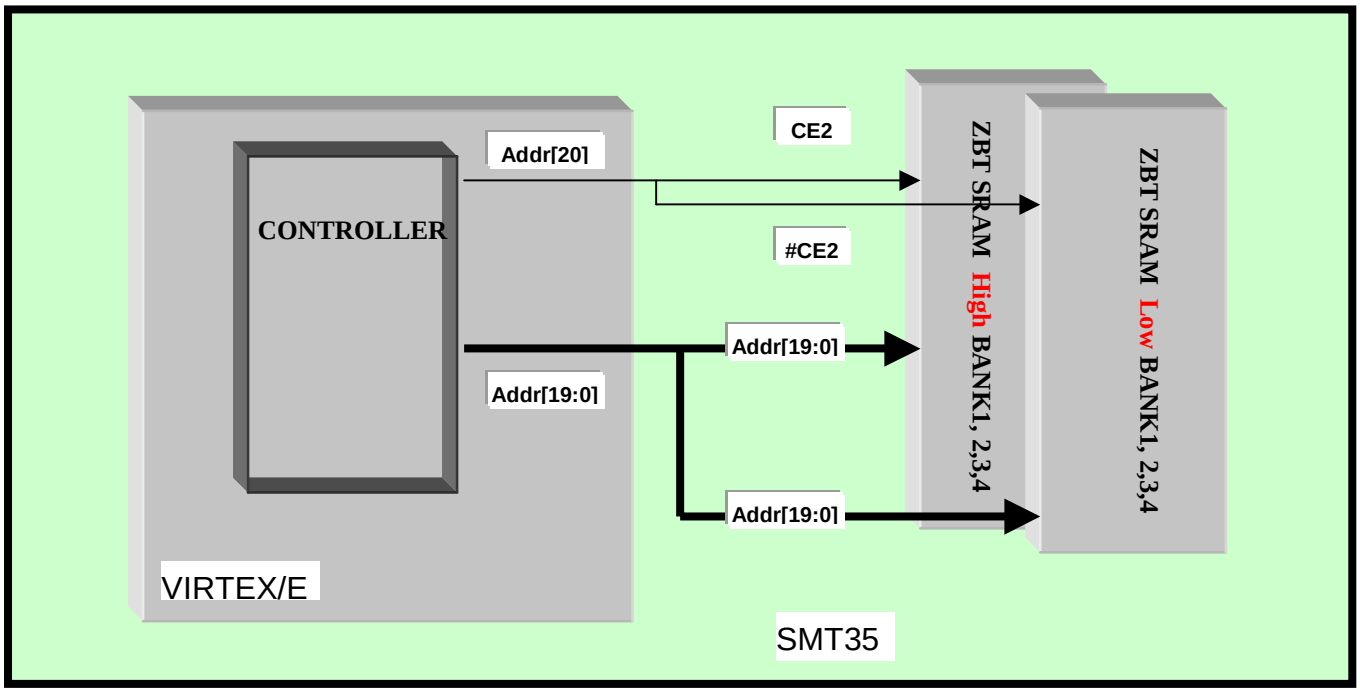


Figure 4: Memory Addressing

Sundance Digital Bus (SDB)

The four 40-way miniature IDC connectors' primary function is to provide bi-directional 16-bit data paths between TIMs with data transfer rates over 200 MBytes/s.

Data rates of 200 MBytes/second through a connector have been achieved using a ground interlaced signal cable.

Each high speed Sundance Digital Bus (SDB) Interface can transfer 16-bit data, to and from the TIM, at such a transfer rate.

400 MBytes/Second Data rates can be reached using in parallel 2 (SDB) Interfaces to send a 32-bit data every clock cycle at 100 MHz

The SDB Interface packs the 16-bit data transmitted into a 32-bit Word and stacks them into a FIFO ready to be used.

The transmission can be fully bi-directional.

Many of Sundance TIM modules are being designed with this interface.

A SDB Interface is available from Sundance Multiprocessor Technology IP Centre.

Alternatively, the Sundance Digital Bus links can be extended to external interconnection by connecting them to the **SMT373** mezzanine card.

With this card, TTL signals are converted to Low-Voltage Differential signals and can connect two systems several meters apart.

It provides two bi-directional 20-bit channels that can transfer up to 2 Gbytes/s through forty SN65LVDM176 transceivers. Each channel provides 16 bit of data, a clock and a clock-enable signal with their direction controlled by one signal. Two other signals can be used for the bus arbitration in a bi-directional application. The direction of each of them can be controlled independently.

All the signals controlling the direction are connected to the SMT358 FPGA through the connectors and so can be controlled by software.

SMT358-DSP Communication channels

The global bus or Comm-Port 0,1,3 or 4 are communication channels of the SMT358 used to interfaced to T.I.'s DSP processors.

The 'C4x Protocol defines Byte-wide links which can theoretically transmit at 20MBytes/second asynchronously between TIMs.

The Global Bus is only available when the SMT358 is connected onto the SMT350PB mother board.

The SMT350PB provides a non-blocking global bus interconnection between any source TIM site and any other destination TIM site. It provides a sustainable throughput of 50 MBytes/s between any of the module sites even with three modules accessing the same destination module. Access to the PCI bus takes place through TIM site 1. Please see our Web Site at http://www.sundance.com/

Figure 5 shows the various dedicated DSP communication channels available on the SMT358 for inter-TIM data transfers.

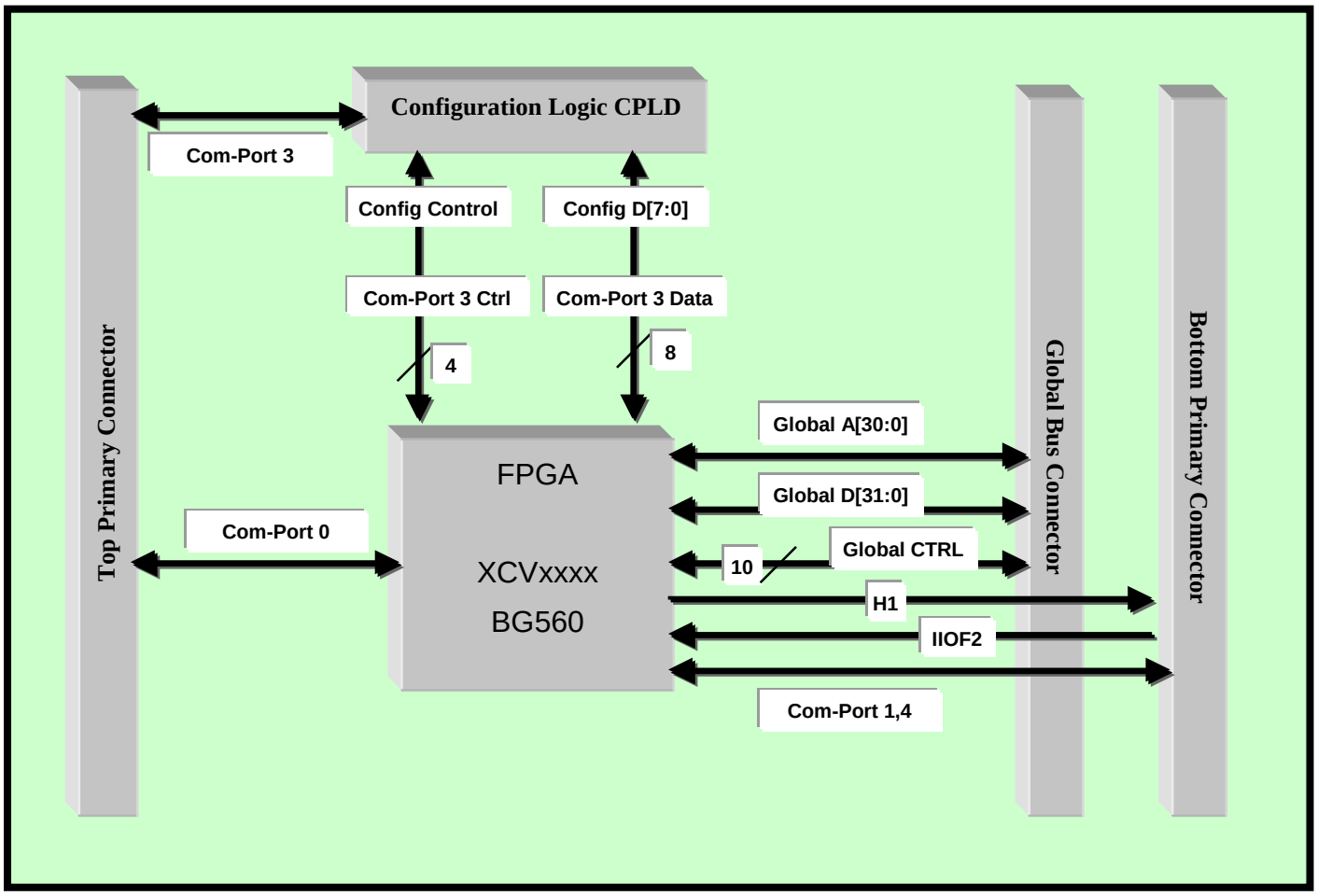


Figure 5: FPGA-DSP Communication Channels

For developers who want to interface a SMT358 to a C4x or C6x TIM like the SMT302, SMT331 or SMT332 via Comm-Ports or the Global Bus, a Comm-Port interface and a Global Bus interface are available from Sundance Multiprocessor Technology IP Centre.

Sundance Datapipe Links

The Comm-Port connections provided on the SMT358 can be used as Sundance Datapipe Links for fast data transfers between SMT338V2-SMT358 or ‘C6x TIM based boards like the SMT335.

An SDB interface is used and offers up to 100 MHz on copper and 50 MHz on flat-ribbon cables like the FMS used on the Sundance range of carrier boards.

FPGA

The FPGA is to be configured over Comm-Port 3 via the CPLD. The configuration bitstream is sent by a host, a ‘C6x or ‘C4x processor. This feature will allow a system to dynamically change the FPGA firmware. The configuration LED indicates that configuration is complete.

The FPGA drives 4 LEDs, and is connected to it’s own local oscillator package.

The FPGA firmware will be user defined, and can be done on demand.

Typical functions that can be implemented in the FPGA are:

- Full bi-directional global-bus interface
- Full bi-directional Comm-Port interface
- Bi-directional SDB Interface
- RAM, FIFOs, Dual port RAMs up to a total of 16K Bytes
- Communication protocols
- DSP pre-processors
- Any digital function that will fit in this size device

The SMT358 TIM can typically be used to interface with a SMT338 Frame Grabber over the SDB connectors. The SMT358 can then perform customer specific data formatting before sending it to a nearby DSP TIM via Comm-Port or SDB.

Due to the parallel nature of an FPGA it is well suited to handle multiple high-speed I/O lines. The FPGA can then provide a cleaner bus-interface to the associated DSP processors.

Global Clock Buffers

The Virtex/E provides four independent Global Clock Buffers, which allow the use of 4 or 8 (for a Virtex E) programmable DLLs to produce waveforms with a wide range of frequencies and duty cycles.

Figure 6 shows the signals assignment to each Global Clock Buffer.

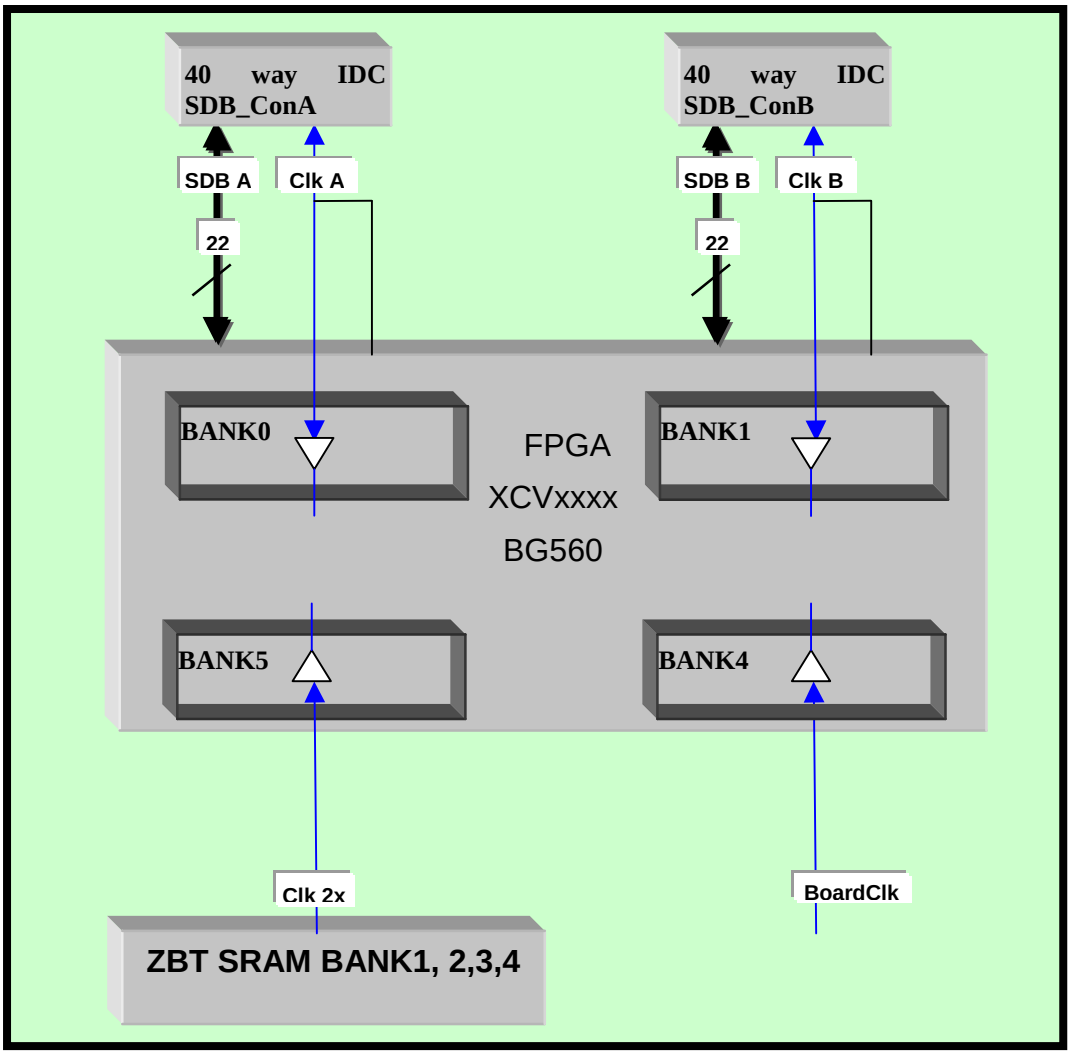


Figure 6: Global Clock Buffers assignments in the Virtex/E

Installation

The minimum system requirements needed to run a SMT358 on a PC is a C4x TIM-based carrier board and a C4x or C6x TIM with at least a Transmit Comm-Port (Comm-Port 0,1 or 2) at Reset.

The goal is to connect one of the processors Comm-Port to Comm-Port 3 of the SMT358.

Follow these steps to install the SMT358 module on a Host system:

1. Remove the carrier board from the host system.
2. Place the SMT358 module into one of the TIM sites on the carrier board.
3. Make sure the that the board is firmly seated, then provide the 3.3V to the board by screwing the SMT358 on the two main mounting holes with the bolts and screws provided with the board.
4. Fit the processor-based board on the carrier board. To do so, please follow the installation procedure of that specific board. In the case of a SMT320 carrier board, the C4x or C6x board MUST be placed on the first TIM slot (TIM slot 0) of the SMT320.
5. Connect at least Comm-Port 3 of the SMT358 to one of the transmit Comm-Port (at Reset) available on the Processor-based board.
6. Connect the SDB links as well if required by your application.
7. Replace the carrier board in the host system.

Configuration

The FPGA configuration is done by a software routine running on a host, ‘C6x or ‘C4x processor that downloads a bitstream to the Virtex/E via the CPLD using Comm-Port 3(on the SMT358). After configuration, the CPLD gives the hand to the FPGA, which becomes the owner of Comm-Port 3.

The CPLD does the handshake with the Comm-Port and communicates with the FPGA as well.

The following description is referring to Figure 7.

Hardware Sequence of events

<u>At power-up.</u>

1) The CPLD polls Comm-Port 3 until it receives the keyword 0xBCBCBCBC. (WAITFORCMD State)

2) On receiving the start-of-bitstream keyword 0xBCBCBCBC, The CPLD reads out the FPGA bitstream from Comm-Port 3 and configures the FPGA (CONFIG State).

3) The FPGA releases its DONE pin when the configuration phase is finished. At this time LED1 goes on (LED1 is directly driven by DONE). Then, the FPGA completes its startup sequence and the design downloaded is now ready to start.

- If the design inside the FPGA instantiates Comm-Port 3: it must be kept reset while the bitstream finishes to be downloaded. To do so, use the FPGARESET pin as a global reset for the Comm-Port interface in particular and for the whole design in general. FPGARESET is a bi-directional active low signal. The CPLD asserts FPGARESET low until it receives the end-of-bitstream word BCBCBC00 defining the end of the configuration process and enters an IDLE State waiting for an interrupt (general TISRESET from the PCI or FPGARESET coming from the FPGA this time).
- If the design inside the FPGA doesn't instantiate Comm-Port 3: The CPLD asserts FPGARESET low until it receives the end-of-bitstream word 0xBCBCBC00 defining the end of the configuration process and enters an IDLE State waiting for an interrupt (general TISRESET from the PCI or FPGARESET from the FPGA). Meanwhile, the FPGA design can start if it doesn't use FPGARESET as a global reset. (but a good practice is to use FPGARESET as a global reset).

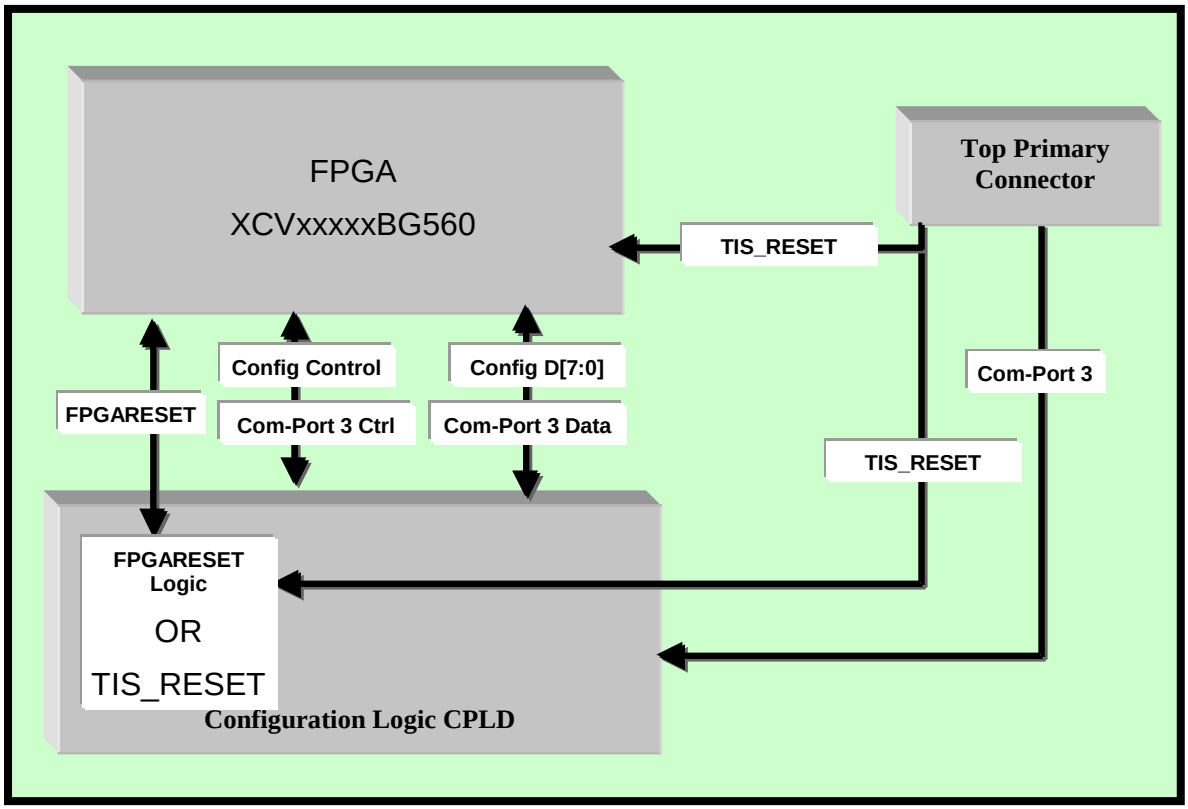


Figure 7: Global Reset routing. Use of FPGARESET as a global reset for designs.

FPGA Reconfiguration

The following description is referring to Figure 8.

Once configured.

When a TISRESET is received by the SMT358, the CPLD and the FPGA are reset.

4) The CPLD owns Comm-Port 3 and can configure the FPGA with a new bitstream (repeat step 2).
5) The CPLD can leave Comm-Port 3 available to the FPGA and enter an Idle state on receiving the command BCBCBC00.

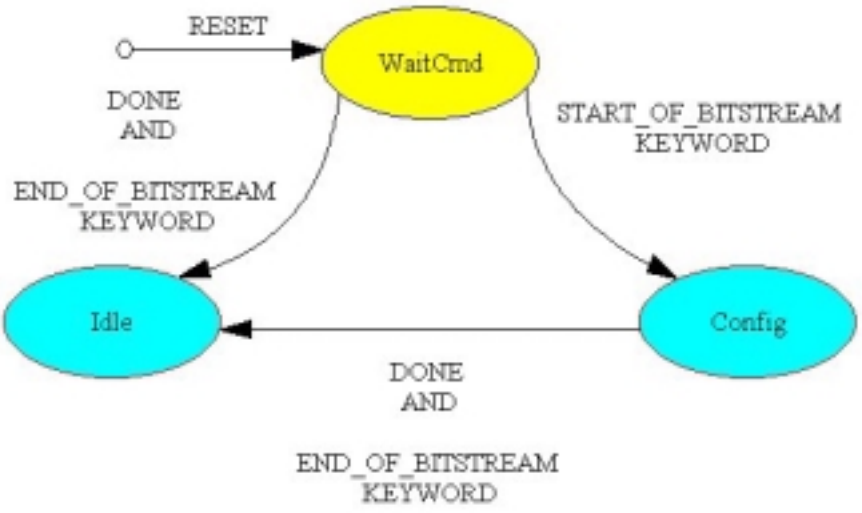


Figure 8: FPGA reconfiguration

FPGA Reconfiguration in real time

The SMT358 can be reprogrammed on-the fly by sending a new bitstream to the Virtex/E FPGA.

It is possible to reconfigure the Virtex/E dynamically by sending a reconfigure command to it.

The circuit recognizing a reconfiguration request must be implemented in the FPGA, so any user-defined command can be sent over a Comm-port for instance.

An example design is provided in the software package for the SMT358 (SMT6358).

The design makes use of a Comm-port to pass the reconfigure command to the SMT358 FPGA and waits for a 1 on the LSB of this Comm-Port.

If another Comm-port than Comm-port 3 is used, the pins corresponding to Comm-port 3 on the FPGA must be tied to “1” in the FPGA (As designed in the reconfiguration example design)

The following description is referring to Figure 8.

6) The FPGA reads the command and then warns the CPLD by sending an interrupt (FPGARESET low) that it decoded a reconfigure command. The FPGA goes into a RESET state and leaves Comm-port 3 available for the CPLD. (in case Comm-port3 is used by the design).
7) On receiving the FPGARESET interrupt, the CPLD goes into the WAITCMD State and polls Comm-port 3 for a keyword. (0xBCBCBCBC or 0xBCBCBC00)
8) On receiving the keyword,
    - If it is the end-of-bitstream keyword 0xBCBCBC00, the FPGA DOES NOT get reconfigured, the CPLD leaves Comm-port 3 available for the FPGA and enters into an IDLE state to wait for the next interrupt.
    - If it is the start-of-bitstream keyword 0xBCBCBCBC, repeat step 2 to 3).

Software tools

The SMT6358 is a suite of software support for the SMT358.

It contains:

- A library of IP cores: a Comm-port Interface, an SDB interface and a ZBT Controller.
- Design examples of Comm-Port, SDB and memory applications.
- The pin allocation file for the Virtex/E: VIRTEX_TOP.ucf.
- 2 conversion softwares needed AFTER a bitstream has been generated to download it in the SMT358 FPGA.

Some additional software is required:

- A CAD platform to create a schematic or VHDL design.
- A simulator to simulate the hardware designs.
- Xilinx Place & Route software such as M3.3i.
- Texas Instrument C compiler or 3L parallel C compiler.

The bitstream that is used to configure the Virtex/E on the SMT358 is built using Xilinx Design implementation tools for FPGAs such as M2.1i.

Follow these steps to build a bistream that can be executed on the SMT358:

1. Select your design available in edif format (filename.edf) with the Xilinx tools.
2. Target the constraint file provided with the SMT358 to map your design to the Virtex/E 's I/O pins (comment out all the I/Os that your design doesn't use)
3. Run Xilinx Design implementation tools.
4. Next the bitstream is generated (Entityname.bit). The bitstream is a binary image of the VHDL core.

The Bit to Dat Conversion

5. Format the Entityname.bit to an Entityname.dat file with the standalone application bit2dat.exe. To do so, you need to modify the Bit2dat.dat file.
   - Place the file Entityname.bit in the folder containing the executable file Bit2dat.exe.
   - Edit the file Bit2dat.bat file.
   - Replace "bit2dat bitfilename bitfilename " by "bit2dat Entityname Entityname". Note that the extension ".bit" is not necessary.
   - Save and double click the bit2dat.bat file. The executable is called and generates a ".dat" file.
6. At this point the hardware core is ready for implementation in an application.
7. With an application running on the Processor-based board which the SMT358 is connected to, send the file Entityname.dat through the Comm-port connected to Comm-Port3 on the SMT358.

The Dat to Obj conversion

Users need to have CCStudio installed, even if they prefer working with 3L as the dat to obj conversion requires an executable installed under CCStudio. (Asm6x.exe)

The reason for this conversion is that the download over JTAG (using CCStudio) of the .dat bitstream can take several minutes with CCStudio and around 30 secs using 3L but it will be instantaneous with the method described below.

The ". Dat" needs to be converted in an ". obj" file so that it can be added to the ".out" application that is run under CCStudio or to the ".app" application that is run under 3L for configuring the SMT358 FPGA.

Then the download of the bitstream is speeded up because the bitstream is read out of the on-board memory of the DSP board instead of being read out of the Hard Drive.

The download is instantaneous if the following method is used:

Format the Entityname.dat to an Entityname.asm file with the standalone application Dat2asm.exe. To do so, you need to modify the Dat2asm.bat file.

a. Place the file Entityname.dat in the folder containing the executable file Dat2asm.exe.

b. Edit the file Dat2asm.bat file.

c. Replace “Dat2asm bitfilename.dat bitfilename.asm ” by “Dat2asm Entityname.dat Entityname.asm”. Note that the extensions “. dat” and “. Asm” are necessary.

d. Replace “asm6x bitfilename.asm” by “asm6x Entityname.asm”. (The asm6x executable is included in CCStudio).

e. Save and double click the Dat2asm.bat file. The executable is called and generates a “. obj” file.

Once the .obj file is generated, it can be linked with the configuration program (xxx.out for CCStudio or xxx.app for 3L)

Interface

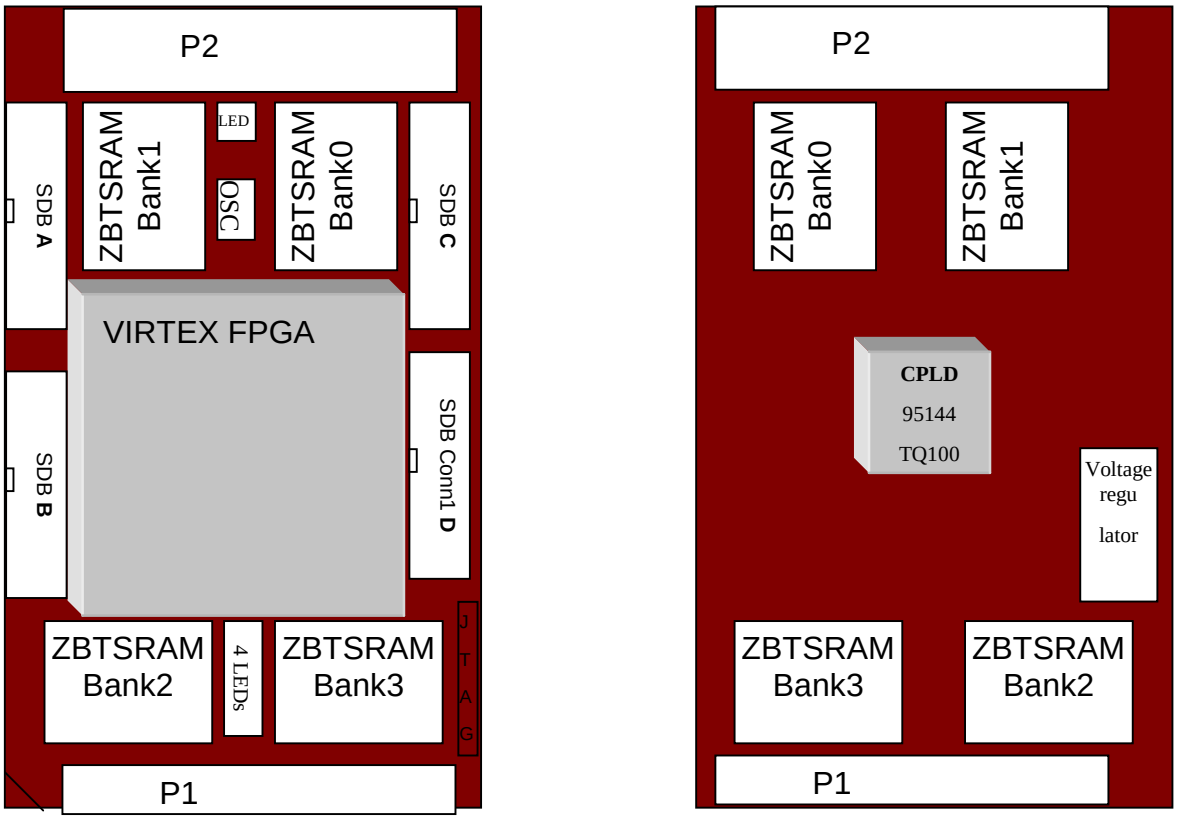


Figure 9: SMT358 Layout

Figure 9 shows the Physical Layout of the SMT358, indicating the external connectors with their location and numbering.

Connector definitions are as follows:

SDB A,B,C,D	:	Digital Data & Clock Input /Output Signal – Sundance Digital Bus High Density ODU connector A (40-way High Density IDC Connectors).
JTAG	:	JTAG Signals – 6-way connector.
P1	:	Top Primary connector.
P2	:	Bottom Connector. (Bottom Primary and Global Expansion Connectors)

Table 2: SMT358 connector reference table

TIM Connectors' Position

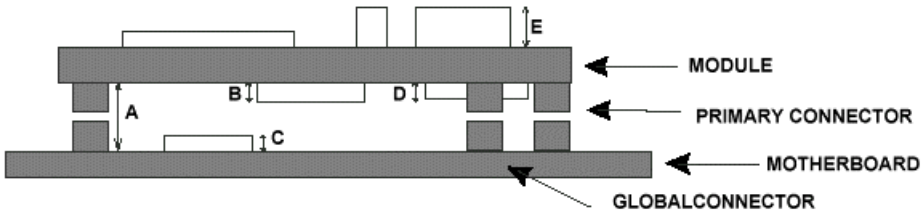
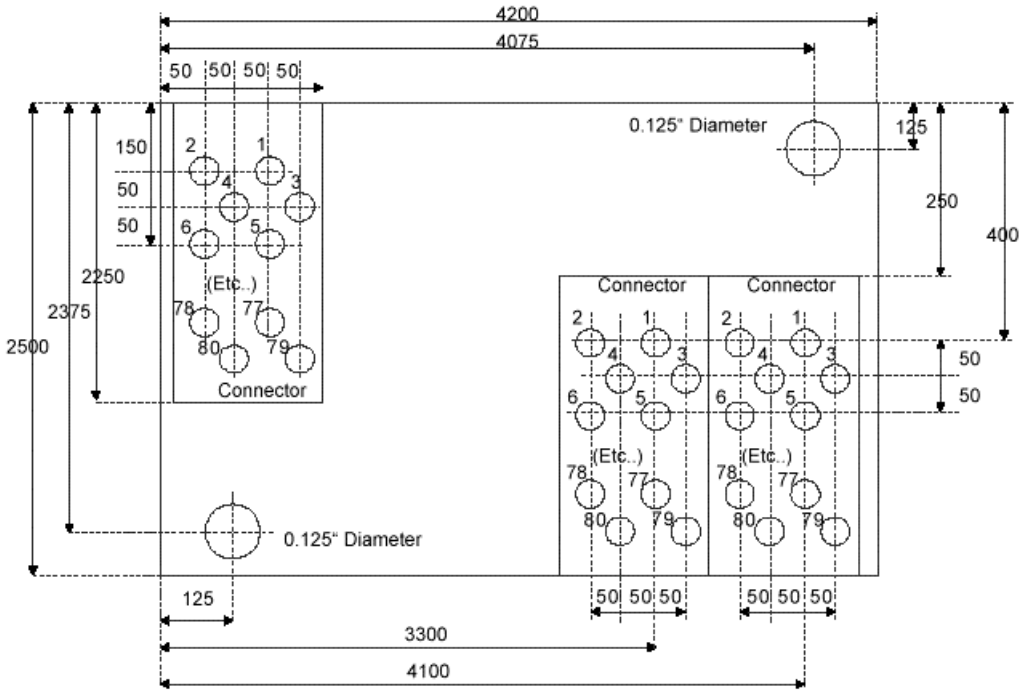


Figure 10: Tim Connectors' position



- All dimensions in 0.001" units.
- Connectors on module are of type FX4C1-80P-1.27DSA without flanges and are placed on the underside of the module.
- Holes for J1, J2, and J3 pins should be 0.024" (0.6mm) diameter.
- A silkscreen trianle should be printed in the corner near the J1 connector.
- The two mounting holes should be 0.125" diameter, suitable for M3 fixing bolts.
- No tracks or components should be placed within 0.125" of the centre of the mounting holes on outer layers of the board.

Figure 11: TIM dimensions and Mounting holes positions

Function	Pin	Pin	Function
GND	2	1	CLK
GND	4	3	D0
GND	6	5	D1
GND	8	7	D2
GND	10	9	D3
GND	12	11	D4
GND	14	13	D5
GND	16	15	D6
GND	18	17	D7
GND	20	19	D8
GND	22	21	D9
GND	24	23	D10
GND	26	25	D11
GND	28	27	D12
GND	30	29	D13
GND	32	31	D14
GND	34	33	D15
DIR0	36	35	USER_0
REQ/DIR2	38	37	WEN
ACQ/DIR1	40	39	USER_1

Table 3: 40 Way SDB Connector Pins

DIR0 sets the direction of the line USERDEF0, DIR1 of the line USERDEF1 and DIR2 of lines D0 to D15, CLKIN and WEN when the SMT373 PiggyBack board is used.

Otherwise, REQ, ACK signals are used for the bus exchange as in the SDBs transfer standard.

Function	Pin
VCC	1
GND	2
TCK	3
TDO	4
TDI	5
TMS	6

Table 4: JTAG Connector