# SMT364

## User Manual

## Revision History

| Date | Comments | Engineer | Version |
|------|----------|----------|---------|
| 31/07/03 | First release | PSR | 1.0 |
| 29/10/03 | External trigger specifications corrected | PSR | 1.1 |
| 12/05/04 | Power Consumption detailed | PSR | 1.2 |
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## Contacting Sundance.

You can contact Sundance for additional information by sending email to support@sundance.com.

## Notes.

- *SMT364* denotes in this document *SMT364*. The board in available in two options: AC or DC-coupled inputs (ADC). It is to be specified when placing an ordering.

- *SHB* stands for **S**undance **H**igh-speed **B**us.

- *ComPort* denotes an 8-bit communication port following the TI C4x standards.

## Precautions.

In order to guarantee that the *SMT364* functions correctly and to protect the module from damage, the following precautions should be taken:

- The *SMT364* is a static sensitive product and should be handled accordingly. Always place the module in a static protective bag during storage and transition.

- The *SMT364* reaches a temperature close to the maximum temperature ratings of the ADCs, FPGA and DC/DC when operated in a closed environment. By mounting a fan inside the PC case, it increases the airflow and therefore reduces the board temperature down, away from the maximum ratings. It is to the customer's responsibility to make sure that a minimum airflow circulates along the carrier board where the SMT364 seats.

## Outline description.

The *SMT364* is a quad high-speed ADC module offering the following features:

- Four 14-bit ADCs ([AD6645-105](#)) sampling at up to 105MHz,

- Single width module,

- Two **S**undance **H**igh-speed **B**us (SHB) connectors,

- Four 20 MegaByte/s communication ports,

- Low-jitter on-board system clock,

- Xilinx Virtex-II FPGA,

- 50-Ohm terminated analogue inputs and outputs, external triggers and clocks via MMBX (Huber and Suhner) connectors,

- User defined pins for external connections,

- Compatible with a wide range of Sundance *SHB* modules,

- TIM standard compatible,

- Default FPGA firmware implementing all the functions described along this documentation.

- Power consumption: 10.95 Watts in total, which is 700mA under 12 Volts, 180mA under 5Volts and 500mA under 3.3Volts.

## Block Diagram - Architecture.

The following diagram shows the architecture of the *SMT364*.
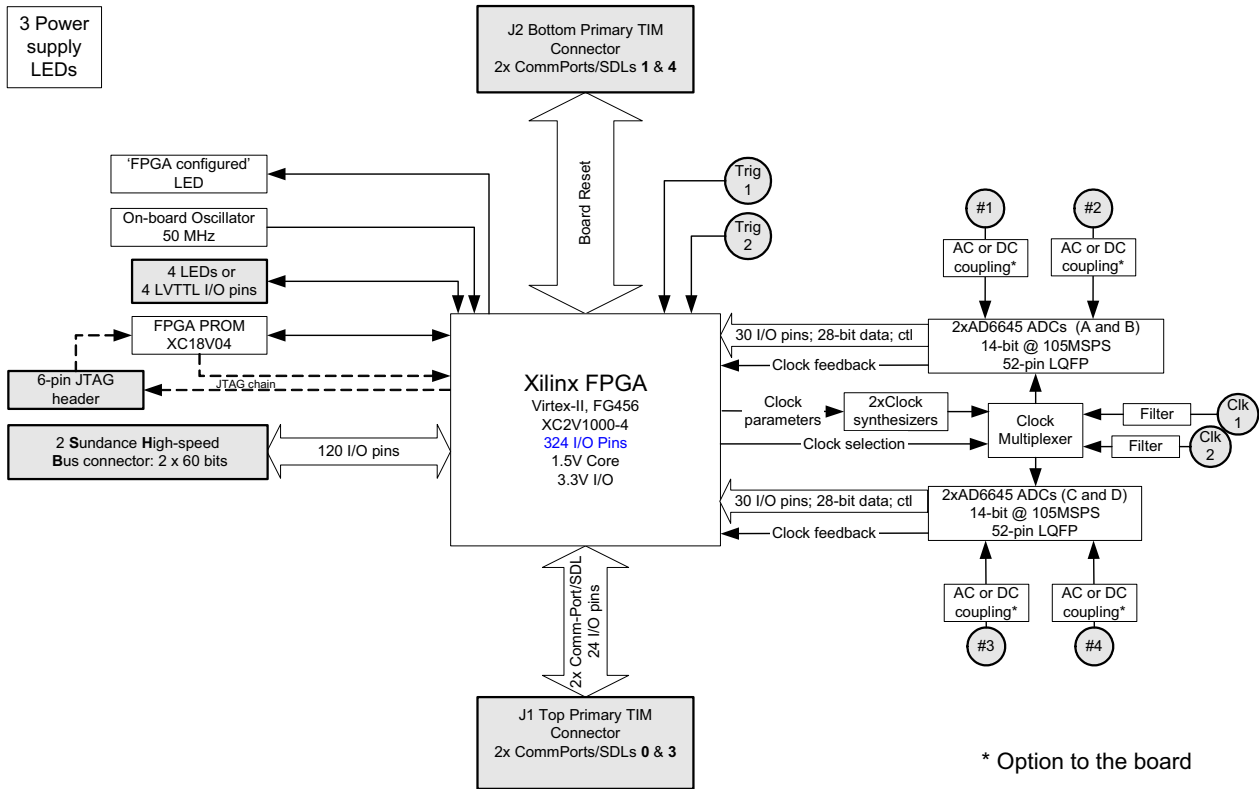


**Figure 1 - Block Diagram.**

Connections to the outside world are greyed out.

Main parts of the board are described in the next part of this document.

## Architecture Description.

The module consists of a Xilinx Virtex-II FPGA, four Analog Devices (14-bit monolithic sampling Analog-to-Digital converters) AD6645.

The AD6645 is a 14-bit monolithic sampling analog-to-digital converter. The chip provides CMOS-compatible digital outputs. It is the Analog Devices' fourth generation of wideband ADCs. The AD6645 maintains outstanding AC performance up to input frequencies of 200 MHz, which makes it suitable for multi-carrier 3G applications. The AD6645 is able to sample from 30 up to 105 MHz. Nevertheless, it is possible to reduce that rate by performing decimation on the data flow.

Parallel busses connect ADCs to the FPGA, which is responsible for transferring samples from the converters. Two on-board frequency synthesizers generate differential encode lines (sampling clocks) to feed the converters; two connectors for two external clocks is also available. Each analogue signal input to the ADCs goes through an extra stage, which can be an opamp (DC coupling) or an RF transformer (AC coupling). The option must be defined when ordering a *SMT364*. ADCs can be coupled together. i.e. they have the same sampling clock or have separate clocks, one external and  one coming from the on-board clock synthesizer.

The Xilinx FPGA Virtex-II is configured via a 6-pin JTAG header or from the on-board Xilinx PROM (XC18V04) at startup. The default configuration mode is from a PROM, which contains the standard modes of operation (as described in this document). An on-board LED indicates that the FPGA is configured. Both devices, FPGA and PROM are in the JTAG chain.

Four Communication links (ComPorts) following the Texas Instrument C4x standard are connected to the FPGA and will be used to receive control words or for other purpose. They can achieve transfers at up to 20Mbytes/s.

Two full *SHB* connectors (60-pin) are accessible from the FPGA. Both are output only and carry samples from ADCs. There are two ADC data-flows per SHB connector). Please refer to the SHB specifications for more details about ways connectors can be configured. Both SHB can be implemented as either two 16-bit interfaces or a single 32-bit interface. In the case of a 32-bit interface, both ADCs must receive the same sampling clock signal.

Four LEDs are driven by the FPGA. Four LVTTL I/Os for general purpose are also available. No clamping diodes to 3.3 Volts and ground are available on the board to avoid damaging pads on the FPGA. It is therefore to the customer to make sure the signals connected to these I/Os are LVTTL and don't show any overshoots.

External Clock, trigger and analogue input signals are all single-ended. External connections to the board are all 50-Ohm terminated. External triggers have clamping diodes to 3.3V and to Ground to avoid damaging the FPGA they are connected to.

A global reset signal is mapped to the FPGA from the top TIM connector to reset the FPGA and reload the FPGA

### Virtex FPGA.

What the FPGA does.

The *SMT364* is populated with a Xilinx Virtex FPGA (XC2V1000-4FG456). This device controls major functions on the module, like CommPorts and SHB communications, data flows from the converters and clock management.

This FPGA needs being configured after power-up and after a module reset. This operation is possible thanks to the on-board Xilinx PROM. This operation can be done automatically when jumper J1 (Figure 8 - Connector Location.) is fitted. If it is not fitted, no configuration is loaded into the FPGA and allows therefore the user to program the FPGA via JTAG with no possible conflict.

Four control registers are implemented into this FPGA to set up converters, their data format, clock synthesizers, CommPort and SHB. Some more details are given in the next parts of this document.

The FPGA is serially programmed using the dedicated pins. The PROM is originally programmed with a default bit stream, which implements all features mentioned in this document.

Ressource occupied.

The default firmware, as it comes with the board, uses FPGA resources, such as Ram Blocks, Flip-flop, Slices, I/O pads. The following table gathers all of them:

|  | Number used | Out of | Percentage of utilisation |
|---|---|---|---|
| **Number of External IOBs** | 170 | 324 | 52% |
| **Number of RAMB16s** | 0 | 40 | 0% |
| **Number of SLICEs** | 753 | 5120 | 14% |
| **Number of GCLKs** | 5 | 16 | 31% |
| **Number of DCMs** | 0 | 8 | 0% |
| **Number of External DIFFMs** | 0 | 162 | 0% |
| **Number of External DIFFSs** | 0 | 162 | 0% |

**Figure 2 - FPGA utilisation.**

Most of the resources are not used by the default firmware, which allows the user to implement some extra processing such as digital filters.

### ADCs.

The *SMT364* is populated with four [AD6645s](#). For more details about these converters (inner characteristics), please refer to the manufacturer (Analog Devices) datasheets.

Data and control lines of the converters are all connected to the FPGA.

### Clock management.

The *SMT364* has two identical on-board low-jitter clock synthesizers, one per pair of ADCs. Both have a **S**erial **P**ort **I**nterface. The FPGA is responsible for setting them to the correct values loaded into a control register. A wide range of frequencies can be set this way. The SPIs are write-only, i.e. they can't be read back.

Clock multiplexers are also available on the board to route the appropriate clock signal (from external or on-board source) to the converters. It is usual to have both ADCs fed with the same sampling clock but it is possible to have an ADC receiving the external clock and the second one receiving the on-board clock. In this particular case, two 16-bit interfaces are necessary to transfer samples to an external TIM.

### Sundance High-speed Bus - SHB.

The *SMT364* provides 2 full SHB (**S**undance **H**igh-speed **B**us) connectors, labelled SHBA (J2) and SHBB (J3) – see Figure 8 - Connector Location.)

SHBA and SHBB are set as transmitter only to transfer data coming from the Analogue-to-Digital Converters to an external SHB module, for instance *SMT365*, *SMT365E* or *SMT374*. Transfers at up to 100 MHz are supported on these two SHB connectors.

The FPGA routes the data lines coming from ADCA and ADCB to SHBA and from ADCC and ADCD to SHBB. The board offers to possibility to output data in either two's complement or binary format. It is also possible to output a 16-bit counter on each SHB half for system testing purpose – It then becomes easier to detect any missing data. The board can also be enabled to add channels with each other ADCA+ADCB and/or ADCC+ADCD and/or ADCA+ADCB+ADCC+ADCD in binary format only.

On each data path, decimators can be set to trim samples out. Decimators are independent. If both decimators of a pair of channel (channels A and B or Channels C and D) are set with the same values and if the sampling clocks (Channel A and Channel B or Channel C and Channel D) are the same, data streams of a same SHB connector can be considered as synchronised and therefore the two 16-bit data streams can be considered as a single 32-bit data stream.

It is possible to control (start/stop) the data flow by the way of an external trigger, for which the active level (high or low) can be set in a control register. It is recommended

to have external trigger signal synchronised to the sampling clock. This external trigger also goes thought 7 latch stages.

### Communication Ports (ComPorts).

The *SMT364* provides 4 physical ComPorts: 0, 1, 3 and 4. The default bit stream provided implements ComPort 4 (Input at reset) to load control registers. A physical connection to a ComPort 0, 1 or 2 (Output at reset) is therefore necessary, to an *SMT365* for instance. Please report to the part dealing with ComPorts (Communication Ports (ComPorts).) in this document for more details.

### External triggering.

Two external trigger connectors (J6 and J12 – see Figure 8 - Connector Location.) are available on the board to trigger converters from an external source. The selection is made via a control register, where channel selection can also be set. There is one trigger per pair of ADC channels.

Triggering consists in enabling or stopping the converters. This is available and accurate as long as the triggering signals are synchronised on the sampling clock. Triggering signals can be set as active high or low in via the control register.

Each trigger input is clamped to 3.3 and Ground to avoid damaging the FPGA I/Os. This is achieved by using single diodes ([BAV99](#)). These diodes can support as maximum, 200mA of forward current and 70 Volts of reverse voltage. It is to the customer to consider this when building a system using an *SMT364*.

### LEDs.

Seven LEDs (Figure 8 - Connector Location.) are available on the board. Four (denoted 0, 1, 2, and 3 on the PCB – top left) of them, green, are driven by the FPGA. In the default bitstream, they indicate what follows:

0 -> Flashing under the ADCA sampling clock (it can be useful to check that the LED is flashing when using an external sampling clock signal),

1 -> Flashing under the ADCB sampling clock,

2 -> Flashing under the ADCB sampling clock,

3 -> Flashing under the ADCB sampling clock.

Two green LEDs, located at the bottom left and right of the board indicate the status of the power supplies. Both should be on when the board is under power.

A red LED located on the top right of the board indicated when the FPGA is not programme. In normal operation, i.e. J1 fitted (Figure 8 - Connector Location.), it flashes once at power-up and after a module reset.

Just after a reset (TIM or FPGA Global Reset), the LEDs display the Firmware version.

### TTL I/Os.

Four TTL I/Os (J4 – see Figure 8 - Connector Location.) are connected directly to the FPGA. They support LVTTL signals. It is recommended to make sure the lines connected to these pins are LVTTL compatible in order not to damage the FPGA pads, as lines are not clamped.

## Sundance Standards.

### Communication Ports (ComPorts).

According to the board you can get up to six 8-bit, data-parallel, inter-processor links that follow Texas Instruments' TMS320C4x Communication Port standard. Additional information on the standard is available in the TMS320C4x User's Guide chapter 12: *Communication ports and the Texas Instrument Module Specification*.

The standard gives a TIM six links numbered from 0 to 5. Each link can be a transmitter or a receiver, and will switch automatically between these states depending on the way you use it. Writing to a receiver or reading from a transmitter will cause a hardware negotiation (token exchange) that will reverse the state of both ends of the link.

Following a processor reset, the first three links (0, 1, and 2) initialise as transmitters and the remainder (3, 4, and 5) initialise as receivers. When you wire TIMs together you *must* make sure that you only ever connect links initialising as transmitters to links initialising as receivers; never connect two transmitters or two receivers. For example, connecting link 0 of one TIM to link 4 of another is safe; connecting link 0 of one TIM to link 2 of another could damage the hardware.

## Always connect ComPort 0, 1 or 2 to ComPort 3, 4 or 5.

On most carrier board the physical connection between ComPorts is made with FMS cables (Ref. SMT3xx-FMS). You must be careful when connecting the cables the make sure that one end is inserted in the opposite sense to the other. One end must have the *blue* backing facing out and the other must have the *silver* backing facing out.

The SMT310Q (SMT320) motherboard communicates with the host PC using ComPort 3 of the site 1 TIM. You should not make any other connections to this ComPort.

ComPorts (Communication ports) links follow Texas Instrument C4x standard. They are 8-bit parallel inter-processor ports of the 'C4x processors.

**The ComPorts drive at 3.3v signal levels.**

The FPGA can implement up to two FIFO buffered ComPort interfaces fully compliant with the TIM standard. They are guaranteed for a transfer rate of 20MB/s.

The FIFOs are useful to maintain a maximum bandwidth and to enable parallel transfers.

Therefore, as an example, each CommPort can be associated with two 15x32-bit unidirectional FIFOs implemented into the FPGA; one for input and one for output. An additional one-word buffer makes them appear as 16x32-bit FIFOs.
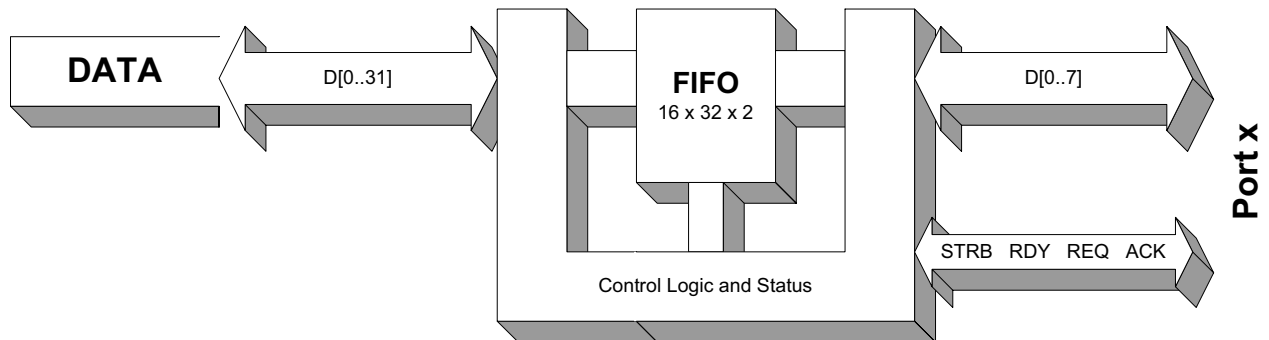


**Figure 3 - CommPort interface data path.**

**S*undance* H*igh-speed* B*us - SHB.***

Both [SHB](#) buses are identical and 60-bit wide.

*SHBs* are parallel communication links for synchronous transmissions. Each *SHB* can be divided into two independent 8-bit buses. Each 8-bit bus includes a clock and three control signals: write enable, request and acknowledge. An *SHB* bus can also be divided into two 16-bit buses and one 8-bit bus.

Here is the architecture of the *SHB* interface implemented into the FPGA:
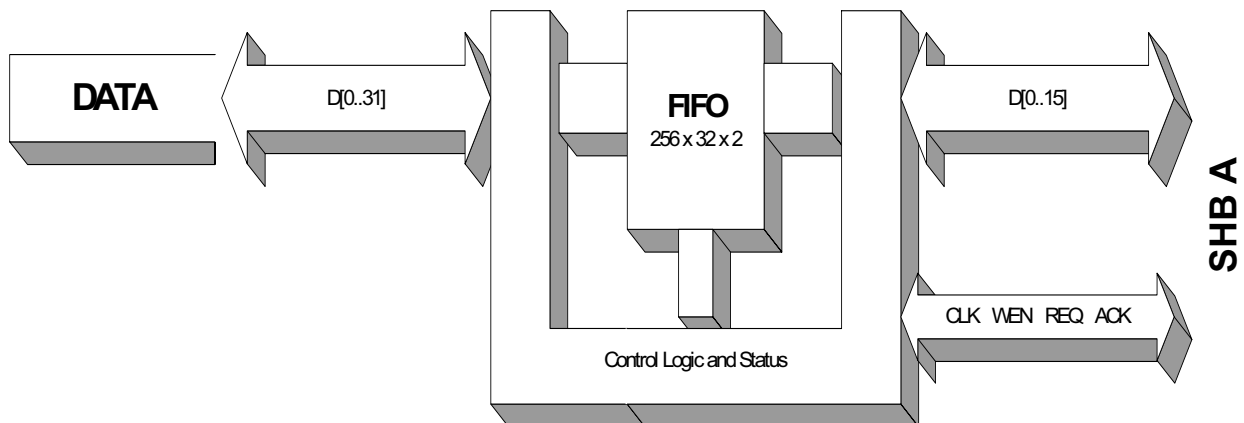


**Figure 4 - SHB interface structure.**

*Communication links implemented on the SMT364.*

The *SMT364* provides 4 ComPort links. They are given the numbers 0, 1, 3 and 4. The default firmware provided with the board implements ComPort4 as a control

register communication port, which means that every control register word has to be sent to ComPort4 on the *SMT364* to be received.

The board also connects two full *SHB* connectors (60 bits) to the FPGA. The FPGA implements two 16-bit (or one 32-bit) unidirectional (transmitter only) interfaces per *SHB* connector to send out samples coming from ADCs.

### *For more details about ComPorts and SHB.*

The following link will give you more information: External_Interface_User_manual.pdf

## ADC Performance.

| Description | Specification |
|---|---|
| **Analogue inputs** | |
| Maximum voltage | 1.1 Volts peak-to-peak (AC coupling).<br>2.2 Volts peak-to-peak (DC coupling – Gain 1).<br>(Specify ADC coupling when placing an order) |
| Impedance | 50 $\Omega$. |
| Bandwidth | - No anti-aliasing filter on the board. It is to the user to set one up if required.<br>- Input transformers (AC option): 2-775 MHz.<br>- Input opamps (DC option): 0-320 MHz<br>- A-to-D converters: 0-250 MHz. |
| **External Clock** | |
| Minimum voltage | - DC-coupled input. Requires a External clock signal centered around 0V.<br>- 0.2 Volt peak-to-peak minimum.<br>- Maximum voltage: 3.3 Volts<br>- Minimum voltage: -3.3 Volts |
| Impedance | 50 $\Omega$. |
| Frequency range | 30-105 MHz – low jitter. |
| **External Trigger** | |
| Frequency Range | 0-52.5 MHz. |
| Signal format | LVTTL (3.3 Volts) format – connected to 3.3V FPGA – Clamp diodes to 3.3V and Ground. |
| **Characteristics** | |
| Resolution | 14 bits. |
| Output format | Binary or 16-bit extended two's complement. |
| Maximum sampling frequency | 105 MHz. |
| SFDR | Up to 81dB. |
| SNR | Up to 63dB. |

**Figure 5 - ADC Performance.**

The following graphs gives the average FFT of sixteen 16K-FFTs processed after capturing data from Channel B – The on-board sampling frequency set to 105 MHz – A 21MHz sine signal is fed to the board. The test has been performed without any input filter (which explains the second peak due to harmonics) at all and with a 35dBc harmonic performance signal generator.
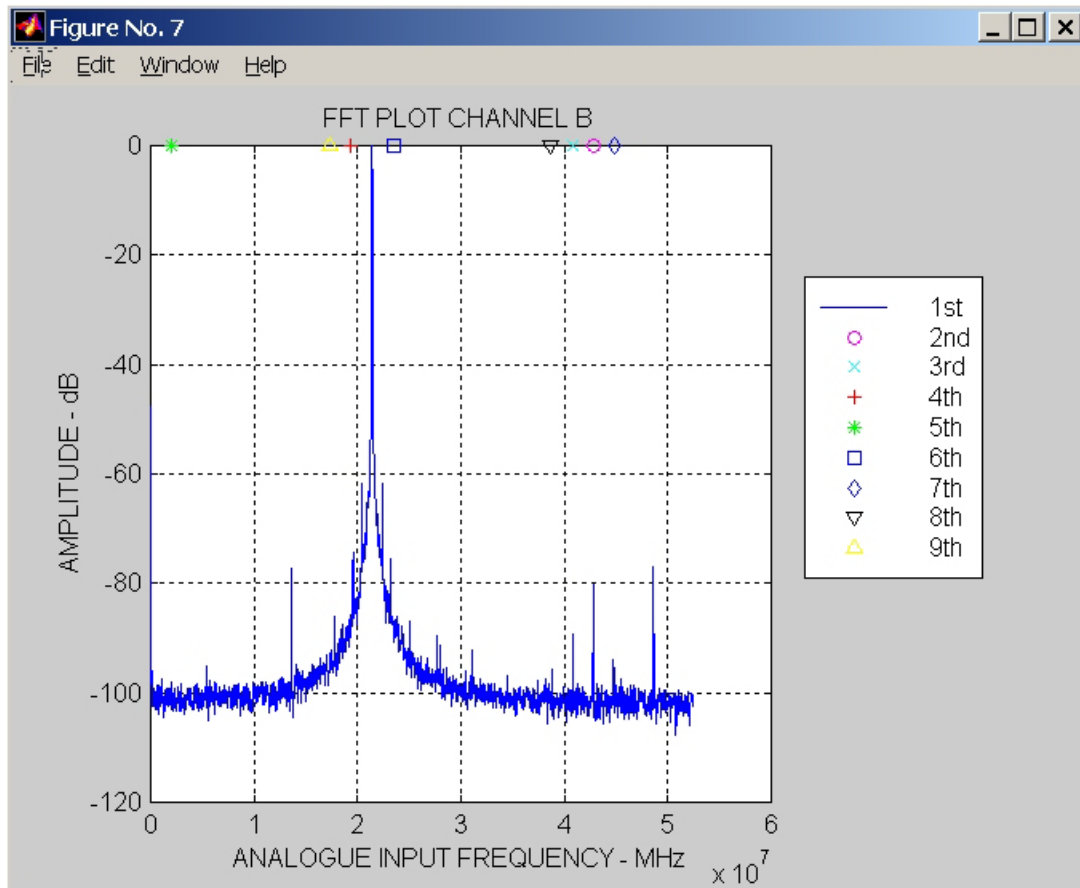


**Figure 6 - FFT ADC Channel - On-board clock.**

Similar results are obtained when using an external clock. It is recommended to use a low-jitter clock and a filter on the ADC inputs. They indeed have a large input bandwidth and therefore allow a high level of harmonics in.

The *SMT6600* package, provided with the *SMT364* contains a documentation dealing with performance. It shows some captures and FFT graphs at different frequencies.

## SHB pinout.

| Pin | | | Signal | Pin | | | Signal | Pin | | | Signal |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | | CLK0 | 21 | | | D19 | 41 | | | D39 |
| 2 | | | D0 | 22 | | | D20/ WEN1 | 42 | | | D40 |
| 3 | | | D1 | 23 | | | D21/ REQ1 | 43 | | | D41 |
| 4 | | | D2 | 24 | | | D22/ ACK1 | 44 | | | D42 |
| 5 | | | D3 | 25 | | | D23/ CLK2 | 45 | | | D43 |
| 6 | | | D4 | 26 | | | D24 | 46 | | | D44/ WEN3 |
| 7 | | | D5 | 27 | | | D25 | 47 | | | D45 REQ23 |
| 8 | | | D6 | 28 | | | D26 | 48 | | | D46/ ACQ3 |
| 9 | | | D7 | 29 | | | D27 | 49 | | | D47/ CLK3 |
| 10 | | | D8/ WEN0 | 30 | | | D28 | 50 | | | D48 |
| 11 | | | D9/ REQ0 | 31 | | | D29 | 51 | | | D49 |
| 12 | | | D10/ ACK0 | 32 | | | D30 | 52 | | | D50 |
| 13 | | | D11/CLK1 | 33 | | | D31 | 53 | | | D51 |
| 14 | | | D12 | 34 | | | D32/WEN2 | 54 | | | D52 |
| 15 | | | D13 | 35 | | | D33/REQ2 | 55 | | | D53 |
| 16 | | | D14 | 36 | | | D34/ ACK2 | 56 | | | D54 |
| 17 | | | D15 | 37 | | | D35/ CLK3 | 57 | | | D55 |
| 18 | | | D16 | 38 | | | D36 | 58 | | | D56/ WEN4 |
| 19 | | | D17 | 39 | | | D37 | 59 | | | D57/ REQ4 |
| 20 | | | D18 | 40 | | | D38 | 60 | | | D58/ ACK4 |

**Figure 7 - SHB Pinout.**

| | |
|---|---|
| 32-bit Interface | |
| 16-bit interface | |

This standard is implemented using SAMTEC QSTRIP 0.50mm Hi-speed connectors.

To improve electrical performances, a ground plane is embedded in each QSTRIP connector.

For long distances micro-coax ribbon cable is used to connect 2 QSTRIP connectors.

An SHB interface can be 8,16 or 32-bit wide.

The default FPGA firmware implements 2 16-bit interfaces.

## FPGA Pinout.

```
#################################
# Constraint File Virtex II for SMT364
#Author:Philippe ROBERT
#$Date:23.07.2002
#$Version: 1.0 - Original draft
#$Date: 09.09.2002
# $Version: 1.1 - CP1 removed and
Clock synthesizer changed
#$Date: 23.07.2002
#$Version    1.0    generated    with
FloorPlanner
#$Version  1.1  01/04/03  -  pinout
reviewed
# $Version 1.2 28/04/03 - CommPort 1
and 4 added
#    (c)    Sundance    Multiprocessor
Technology   #
#################################
# Start of Constraints extracted by
Floorplanner from the Design
```

**# ADCD**

```
NET "adcd_rdy_gclk" LOC = "AB12"  ;
NET "adcd_rdy" LOC = "AA16"  ;
NET "adcd_ovr" LOC = "V17"  ;
NET "adcd_data<13>" LOC = "AB16" ;
NET "adcd_data<12>" LOC = "W16"  ;
NET "adcd_data<11>" LOC = "Y16"  ;
NET "adcd_data<10>" LOC = "V16"  ;
NET "adcd_data<9>" LOC = "V15"  ;
NET "adcd_data<8>" LOC = "AA17"  ;
NET "adcd_data<7>" LOC = "AB17"  ;
NET "adcd_data<6>" LOC = "AA18"  ;
NET "adcd_data<5>" LOC = "AB18"  ;
NET "adcd_data<4>" LOC = "W17"  ;
NET "adcd_data<3>" LOC = "Y17"  ;
NET "adcd_data<2>" LOC = "W18"  ;
NET "adcd_data<1>" LOC = "Y18"  ;
NET "adcd_data<0>" LOC = "AB19"  ;
```

**# ADCC**

```
NET "adcc_rdy_gclk" LOC = "Y12"  ;
NET "adcc_rdy" LOC = "AA13"  ;
NET "adcc_ovr" LOC = "Y15"  ;
NET "adcc_data<13>" LOC = "AB13"  ;
NET "adcc_data<12>" LOC = "U13"  ;
NET "adcc_data<11>" LOC = "V13"  ;
NET "adcc_data<10>" LOC = "W13"  ;
NET "adcc_data<9>" LOC = "Y13"  ;
NET "adcc_data<8>" LOC = "AA14"  ;
NET "adcc_data<7>" LOC = "AB14"  ;
NET "adcc_data<6>" LOC = "W14"  ;
NET "adcc_data<5>" LOC = "Y14"  ;
NET "adcc_data<4>" LOC = "U14"  ;
NET "adcc_data<3>" LOC = "V14"  ;
NET "adcc_data<2>" LOC = "AA15"  ;
NET "adcc_data<1>" LOC = "AB15"  ;
NET "adcc_data<0>" LOC = "W15"  ;
```

**# ADCB**

NET "adcb_rdy_gclk" LOC = "V11" ;

NET "adcb_rdy" LOC = "AB7" ;

NET "adcb_ovr" LOC = "V9" ;

NET "adcb_data<13>" LOC = "AA7" ;

NET "adcb_data<12>" LOC = "U9" ;

NET "adcb_data<11>" LOC = "V8" ;

NET "adcb_data<10>" LOC = "Y8" ;

NET "adcb_data<9>" LOC = "W8" ;

NET "adcb_data<8>" LOC = "AB8" ;

NET "adcb_data<7>" LOC = "AA8" ;

NET "adcb_data<6>" LOC = "Y9" ;

NET "adcb_data<5>" LOC = "W9" ;

NET "adcb_data<4>" LOC = "AB9" ;

NET "adcb_data<3>" LOC = "AA9" ;

NET "adcb_data<2>" LOC = "Y10" ;

NET "adcb_data<1>" LOC = "W10" ;

NET "adcb_data<0>" LOC = "V10" ;

# ADCA

NET "adca_rdy_gclk" LOC = "Y11" ;

NET "adca_rdy" LOC = "AB4" ;

NET "adca_ovr" LOC = "W7" ;

NET "adca_data<13>" LOC = "AA4" ;

NET "adca_data<12>" LOC = "Y4" ;

NET "adca_data<11>" LOC = "AA3" ;

NET "adca_data<10>" LOC = "Y5" ;

NET "adca_data<9>" LOC = "W5" ;

NET "adca_data<8>" LOC = "V7" ;

NET "adca_data<7>" LOC = "V6" ;

NET "adca_data<6>" LOC = "AB5" ;

NET "adca_data<5>" LOC = "AA5" ;

NET "adca_data<4>" LOC = "Y6" ;

NET "adca_data<3>" LOC = "W6" ;

NET "adca_data<2>" LOC = "AB6" ;

NET "adca_data<1>" LOC = "AA6" ;

NET "adca_data<0>" LOC = "Y7" ;

# CLOCK SYNTHESIZERS

NET "freq_s_load_adc_CD" LOC = "C17" ;

NET "freq_s_load_adc_AB" LOC = "A18" ;

NET "freq_s_data_adc_CD" LOC = "B17" ;

NET "freq_s_data_adc_AB" LOC = "B19" ;

NET "freq_s_clock_adc_CD" LOC = "A17" ;

NET "freq_s_clock_adc_AB" LOC = "A19" ;

NET "freq_np_load_adc_CD" LOC = "D17" ;

NET "freq_np_load_adc_AB" LOC = "B18" ;

NET "freq_master_reset_CD" LOC = "C16" ;

NET "freq_master_reset_AB" LOC = "D16" ;

NET "freq_clk_sel_adc_CD<1>" LOC = "E17" ;

NET "freq_clk_sel_adc_CD<0>" LOC = "E16" ;

NET "freq_clk_sel_adc_AB<1>" LOC = "F18" ;

NET "freq_clk_sel_adc_AB<0>" LOC = "D21" ;

# MISC

NET "ttls<3>" LOC = "A15" ;

NET "ttls<2>" LOC = "C15" ;

NET "ttls<1>" LOC = "B15" ;

NET "ttls<0>" LOC = "D15" ;

NET "pxi_trig4" LOC = "D18" ;

NET "pxi_trig3" LOC = "C21" ;

NET "pxi_trig2" LOC = "C22" ;

NET "pxi_trig1" LOC = "E18" ;

NET "pxi_clk" LOC = "C18" ;

NET "nreset" LOC = "V12" ;

NET "leds<3>" LOC = "F14" ;

NET "leds<2>" LOC = "E15" ;

NET "leds<1>" LOC = "A16" ;

NET "leds<0>" LOC = "B16" ;

NET "iiofs<2>" LOC = "Y21" ;

NET "iiofs<1>" LOC = "AA20" ;

NET "iiofs<0>" LOC = "W20" ;

NET "conf_init" LOC = "AA19" ;

NET "conf_din" LOC = "V18" ;

NET "clock" LOC = "D11" ;

NET "adc_trig_CD" LOC = "T21" ;

NET "adc_trig_AB" LOC = "T2" ;

# COMMPORT 4

NET "cp4_stb" LOC = "A7" ;

NET "cp4_req" LOC = "B7" ;

NET "cp4_rdy" LOC = "D7" ;

NET "cp4_data<7>" LOC = "D8" ;

NET "cp4_data<6>" LOC = "C8" ;

NET "cp4_data<5>" LOC = "B8" ;

NET "cp4_data<4>" LOC = "A8" ;

NET "cp4_data<3>" LOC = "E9" ;

NET "cp4_data<2>" LOC = "F9" ;

NET "cp4_data<1>" LOC = "D9" ;

NET "cp4_data<0>" LOC = "C9" ;

NET "cp4_ack" LOC = "C7" ;

# COMMPORT 3

NET "cp3_stb" LOC = "V19" ;

NET "cp3_req" LOC = "V22" ;

NET "cp3_rdy" LOC = "V20" ;

NET "cp3_data<7>" LOC = "T20" ;

NET "cp3_data<6>" LOC = "T19" ;

NET "cp3_data<5>" LOC = "U22" ;

NET "cp3_data<4>" LOC = "U21" ;

NET "cp3_data<3>" LOC = "U20" ;

NET "cp3_data<2>" LOC = "U19" ;

NET "cp3_data<1>" LOC = "T18" ;

NET "cp3_data<0>" LOC = "U18" ;

NET "cp3_ack" LOC = "V21" ;

# COMMPORT 1

NET "cp1_stb" LOC = "C12" ;

NET "cp1_req" LOC = "B13" ;

NET "cp1_rdy" LOC = "B12" ;

NET "cp1_data<7>" LOC = "C13" ;

NET "cp1_data<6>" LOC = "D13" ;

NET "cp1_data<5>" LOC = "E13" ;

NET "cp1_data<4>" LOC = "E14" ;

NET "cp1_data<3>" LOC = "A14" ;

NET "cp1_data<2>" LOC = "B14" ;

NET "cp1_data<1>" LOC = "C14" ;

NET "cp1_data<0>" LOC = "D14" ;

NET "cp1_ack" LOC = "A13" ;

# COMMPORT 0

NET "cp0_stb" LOC = "T3" ;

NET "cp0_req" LOC = "T5" ;

NET "cp0_rdy" LOC = "T4" ;

NET "cp0_data<7>" LOC = "U1" ;

NET "cp0_data<6>" LOC = "U2" ;

NET "cp0_data<5>" LOC = "V1" ;

NET "cp0_data<4>" LOC = "V2" ;

NET "cp0_data<3>" LOC = "U3" ;

NET "cp0_data<2>" LOC = "U4" ;

NET "cp0_data<1>" LOC = "W1"  ;

NET "cp0_data<0>" LOC = "W2"  ;

NET "cp0_ack" LOC = "R5"  ;

# SHBA

NET "shba_clk1" LOC = "D12"  ;

NET "shba_clk0" LOC = "E12"  ;

NET "shba<59>" LOC = "T1"  ;

NET "shba<58>" LOC = "R4"  ;

NET "shba<57>" LOC = "R3"  ;

NET "shba<56>" LOC = "R2"  ;

NET "shba<55>" LOC = "R1"  ;

NET "shba<54>" LOC = "P6"  ;

NET "shba<53>" LOC = "P5"  ;

NET "shba<52>" LOC = "P4"  ;

NET "shba<51>" LOC = "P3"  ;

NET "shba<50>" LOC = "P2"  ;

NET "shba<49>" LOC = "P1"  ;

NET "shba<48>" LOC = "N6"  ;

NET "shba<47>" LOC = "N5"  ;

NET "shba<46>" LOC = "N4"  ;

NET "shba<45>" LOC = "N3"  ;

NET "shba<44>" LOC = "N2"  ;

NET "shba<43>" LOC = "N1"  ;

NET "shba<42>" LOC = "M6"  ;

NET "shba<41>" LOC = "M5"  ;

NET "shba<40>" LOC = "M4"  ;

NET "shba<39>" LOC = "M3"  ;

NET "shba<38>" LOC = "M2"  ;

NET "shba<37>" LOC = "M1"  ;

NET "shba<36>" LOC = "L2"  ;

NET "shba<35>" LOC = "L3"  ;

NET "shba<34>" LOC = "L4"  ;

NET "shba<33>" LOC = "L5"  ;

NET "shba<32>" LOC = "K1"  ;

NET "shba<31>" LOC = "K2"  ;

NET "shba<30>" LOC = "K3"  ;

NET "shba<29>" LOC = "K4"  ;

NET "shba<28>" LOC = "L6"  ;

NET "shba<27>" LOC = "K6"  ;

NET "shba<26>" LOC = "K5"  ;

NET "shba<25>" LOC = "J5"  ;

NET "shba<24>" LOC = "J1"  ;

NET "shba<23>" LOC = "J2"  ;

NET "shba<22>" LOC = "J3"  ;

NET "shba<21>" LOC = "J4"  ;

NET "shba<20>" LOC = "H1"  ;

NET "shba<19>" LOC = "H2"  ;

NET "shba<18>" LOC = "H3"  ;

NET "shba<17>" LOC = "H4"  ;

NET "shba<16>" LOC = "J6"  ;

NET "shba<15>" LOC = "H5"  ;

NET "shba<14>" LOC = "G1"  ;

NET "shba<13>" LOC = "G2"  ;

NET "shba<12>" LOC = "G3"  ;

NET "shba<11>" LOC = "G4"  ;

NET "shba<10>" LOC = "F1"  ;

NET "shba<9>" LOC = "F2"  ;

NET "shba<8>" LOC = "F3"  ;

NET "shba<7>" LOC = "F4"  ;

NET "shba<6>" LOC = "G5"  ;

NET "shba<5>" LOC = "F5"  ;

NET "shba<4>" LOC = "E1"  ;

NET "shba<3>" LOC = "E2"  ;

NET "shba<2>" LOC = "E3"  ;

NET "shba<1>" LOC = "E4"  ;

NET "shba<0>" LOC = "D1"  ;

# SHBB

NET "shbb_clk1" LOC = "F13" ;

NET "shbb_clk0" LOC = "B11" ;

NET "shbb<59>" LOC = "T22" ;

NET "shbb<58>" LOC = "P17" ;

NET "shbb<57>" LOC = "R18" ;

NET "shbb<56>" LOC = "R19" ;

NET "shbb<55>" LOC = "R20" ;

NET "shbb<54>" LOC = "R21" ;

NET "shbb<53>" LOC = "R22" ;

NET "shbb<52>" LOC = "P19" ;

NET "shbb<51>" LOC = "P20" ;

NET "shbb<50>" LOC = "P21" ;

NET "shbb<49>" LOC = "P22" ;

NET "shbb<48>" LOC = "P18" ;

NET "shbb<47>" LOC = "N18" ;

NET "shbb<46>" LOC = "N19" ;

NET "shbb<45>" LOC = "N20" ;

NET "shbb<44>" LOC = "N21" ;

NET "shbb<43>" LOC = "N22" ;

NET "shbb<42>" LOC = "N17" ;

NET "shbb<41>" LOC = "M17" ;

NET "shbb<40>" LOC = "M18" ;

NET "shbb<39>" LOC = "M19" ;

NET "shbb<38>" LOC = "M20" ;

NET "shbb<37>" LOC = "M21" ;

NET "shbb<36>" LOC = "L22" ;

NET "shbb<35>" LOC = "L21" ;

NET "shbb<34>" LOC = "L20" ;

NET "shbb<33>" LOC = "L19" ;

NET "shbb<32>" LOC = "L18" ;

NET "shbb<31>" LOC = "L17" ;

NET "shbb<30>" LOC = "K22" ;

NET "shbb<29>" LOC = "K21" ;

NET "shbb<28>" LOC = "K20" ;

NET "shbb<27>" LOC = "K19" ;

NET "shbb<26>" LOC = "K18" ;

NET "shbb<25>" LOC = "K17" ;

NET "shbb<24>" LOC = "J22" ;

NET "shbb<23>" LOC = "J21" ;

NET "shbb<22>" LOC = "J20" ;

NET "shbb<21>" LOC = "J19" ;

NET "shbb<20>" LOC = "J18" ;

NET "shbb<19>" LOC = "J17" ;

NET "shbb<18>" LOC = "H22" ;

NET "shbb<17>" LOC = "H21" ;

NET "shbb<16>" LOC = "H20" ;

NET "shbb<15>" LOC = "H19" ;

NET "shbb<14>" LOC = "G22" ;

NET "shbb<13>" LOC = "G21" ;

NET "shbb<12>" LOC = "G20" ;

NET "shbb<11>" LOC = "G19" ;

NET "shbb<10>" LOC = "H18" ;

NET "shbb<9>" LOC = "G18" ;

NET "shbb<8>" LOC = "F22" ;

NET "shbb<7>" LOC = "F21" ;

NET "shbb<6>" LOC = "F20" ;

NET "shbb<5>" LOC = "F19" ;

NET "shbb<4>" LOC = "E22" ;

NET "shbb<3>" LOC = "E21" ;

NET "shbb<2>" LOC = "E20" ;

NET "shbb<1>" LOC = "E19" ;

NET "shbb<0>" LOC = "D22" ;

## At power-up and on reset.

At power-up, the FPGA is not configured and is waiting for a bit stream to be loaded.

By fitting Jumper J1 (Figure 8 - Connector Location.), it will allow the bit stream stored into the PROM to be loaded into the FPGA at power-up and after every TIM reset.

If J1 is not fitted, nothing happens. This condition is useful when needing to configure the FPGA via JTAG.

Also at power-up and on a carrier board reset signal, the *SMT364* expects receiving a dummy ComPort word (any value) and sends one back containing the Firmware version number. It is a way of checking that the firmware is latest and that the board is responding and ready to work. The format of that ComPort word is as follow:

> ***0xFF364Fxy***, which means FPGA firmware version **x**.**y**
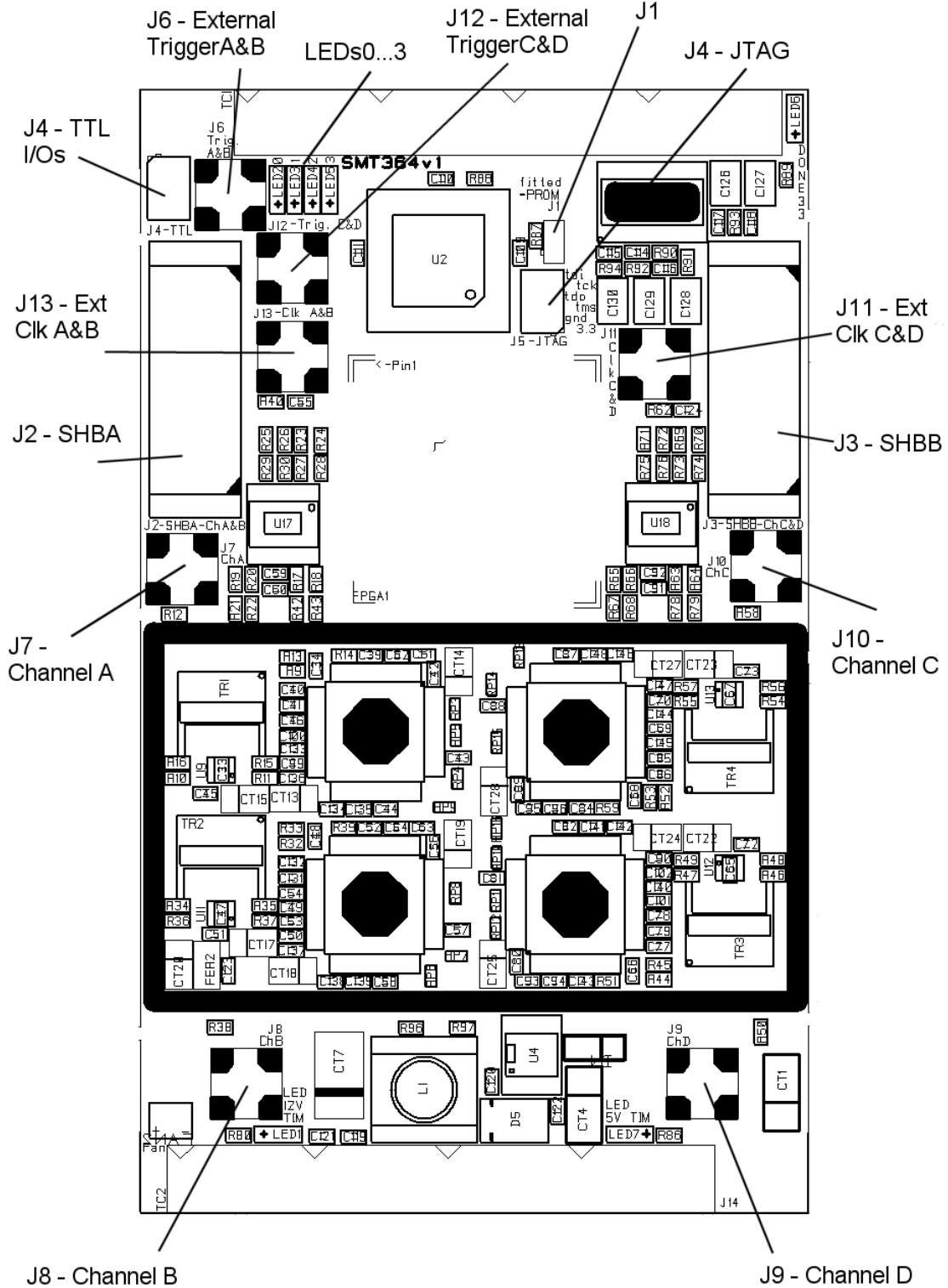
# Connector position.



**Figure 8 - Connector Location.**

The diagram below gives the position and the meaning of the connectors that the customer is likely to use.

## Operating conditions.

### Safety

The module presents no hazard to the user.

### EMC

The module is designed to operate within an enclosed host system that provides adequate EMC shielding. Operation within the EU EMC guidelines is only guaranteed when the module is installed within an appropriate host system.

The module is protected from damage by fast voltage transients introduced along output cables from outside the host system.

Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.

### General Requirements

The module must be fixed to a TIM40-compliant carrier board.

The *SMT364* module is in a range of modules that must be supplied with a 3.3v power source. In addition to the 5v supply specified in the TIM specification, these new generation modules require an additional 3.3v supply to be presented on the two diagonally opposite TIM mounting holes. The lack of this 3.3v power supply should not damage the module, although it will obviously be inoperable; prolonged operation under these circumstances is not recommended.

The *SMT364* is compatible with all Sundance TIM carrier boards. It is a 5v tolerant module, and as such, it may be used in mixed systems with older TIM modules, carrier boards and I/O modules. It is anyway recommended to use the *SMT364* connected to an SHB TIM module such as *SMT365* or *SMT365E* or *SMT374* in order to get better transfer performance.

The external ambient temperature must remain between 0˚C and 40˚C, and the relative humidity must not exceed 95% (non-condensing).

### Power Consumption

The power consumption of this TIM is dependent on the operating conditions in terms of core activity and I/O activity. The maximum power consumption is 10.95W, which is 700mA under 12Volts, 180mA under 5Volts and 500mA under 3.3Volts.

# Register settings.

## *Register 0x0 – Clock management.*

| Bit number | Description |
|---|---|
| Bit 31 | 0 |
| Bit 30 | 0 |
| Bit 29 | 0 |
| Bit 28 | 0 |
| Bit 27 | Clock Selection Channel D ('0'=Internal; '1'=External) |
| Bit 26 | Clock Selection Channel C ('0'=Internal; '1'=External) |
| Bit 25 | Clock Selection Channel B ('0'=Internal; '1'=External) |
| Bit 24 | Clock Selection Channel A ('0'=Internal; '1'=External) |
| Bit 23 | Clock synthesizer – N (divider) Bit2 – ADC-CD |
| Bit 22 | Clock synthesizer – N (divider) Bit1 – ADC-CD |
| Bit 21 | Clock synthesizer – N (divider) Bit0 – ADC-CD |
| Bit 20 | Clock synthesizer - M Bit8 – ADC-CD |
| Bit 19 | Clock synthesizer – M Bit7 – ADC-CD |
| Bit 18 | Clock synthesizer - M Bit6 – ADC-CD |
| Bit 17 | Clock synthesizer - M Bit5 – ADC-CD |
| Bit 16 | Clock synthesizer - M Bit4 – ADC-CD |
| Bit 15 | Clock synthesizer - M Bit3 – ADC-CD |
| Bit 14 | Clock synthesizer - M Bit2 – ADC-CD |
| Bit 13 | Clock synthesizer - M Bit1 – ADC-CD |
| Bit 12 | Clock synthesizer - M Bit0 – ADC-CD |
| Bit 11 | Clock synthesizer – N (divider) Bit2 - ADC-AB |
| Bit 10 | Clock synthesizer – N (divider) Bit1 - ADC-AB |
| Bit 9 | Clock synthesizer – N (divider) Bit0 - ADC-AB |
| Bit 8 | Clock synthesizer - M Bit8 – ADC-AB |
| Bit 7 | Clock synthesizer - M Bit7 – ADC-AB |
| Bit 6 | Clock synthesizer - M Bit6 – ADC-AB |
| Bit 5 | Clock synthesizer - M Bit5 – ADC-AB |
| Bit 4 | Clock synthesizer - M Bit4 – ADC-AB |
| Bit 3 | Clock synthesizer - M Bit3 – ADC-AB |
| Bit 2 | Clock synthesizer - M Bit2 – ADC-AB |
| Bit 1 | Clock synthesizer - M Bit1 – ADC-AB |
| Bit 0 | Clock synthesizer - M Bit0 – ADC-AB |

$F_{Synthesized}$ = (M/N) MHz - With 500 < M < 250 (binary encoding) and N can take one of the following values: 1 ("000"), 1.5 ("001"), 2 ("010"), 3 ("011"), 4 ("100"), 6 ("101"), 8

("110") or 12 ("111"). See ICS8430-01 datasheet for more information performance, jitter, etc.

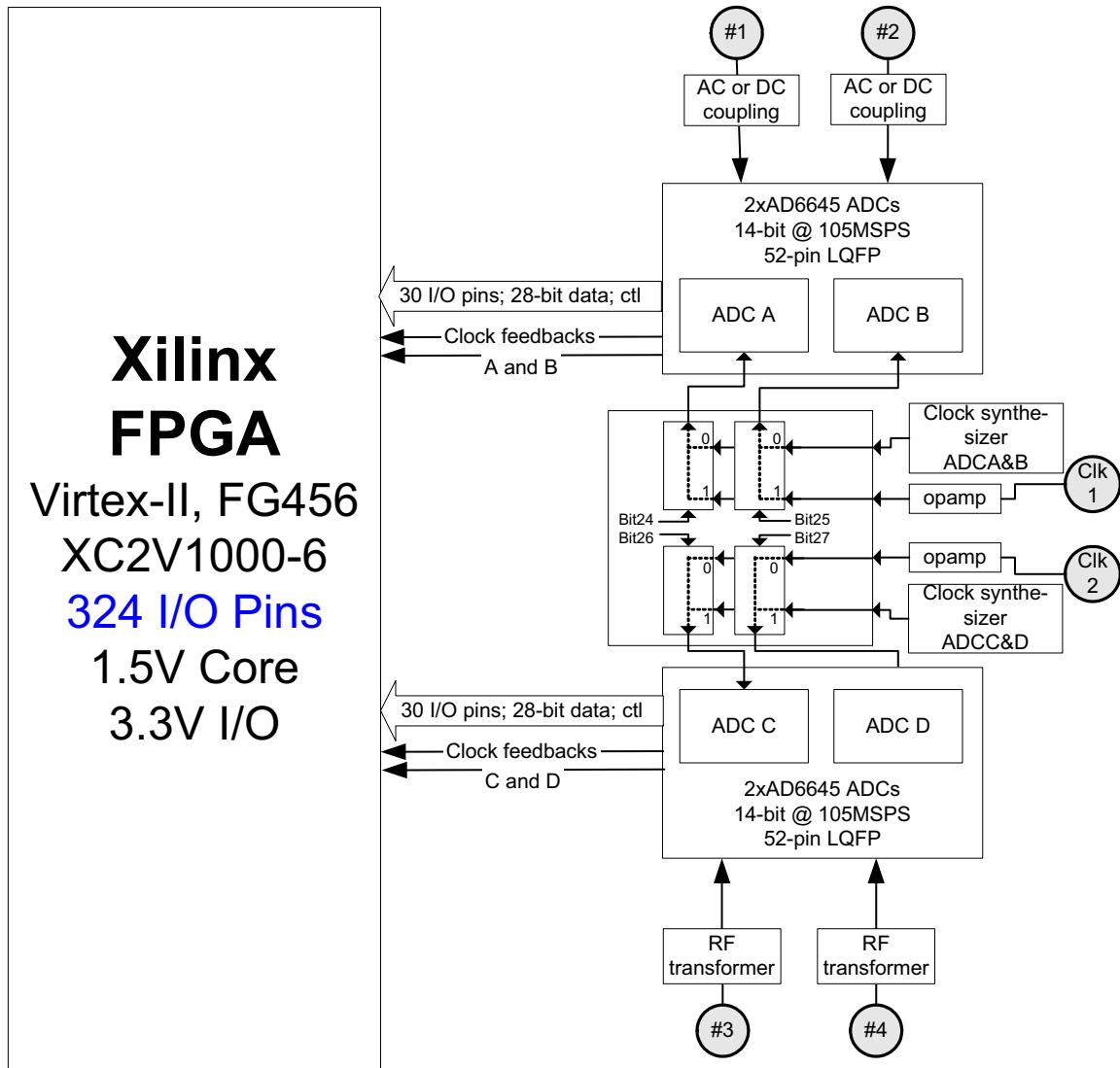The following diagram shows how clock signals can be routed on the PCB.



**Figure 9 - Clock Routing.**

The skew between ADC clock signals is negligible, which means that samples coming from both converters can be considered as synchronised when Bit26 and Bit27 are the same.

### *Register 0x1 –Channel data routing – Triggers.*

| Bit number | Description |
| --- | --- |
| Bit 31 | 0 |
| Bit 30 | 0 |
| Bit 29 | 0 |
| Bit 28 | 1 |
| Bit 27 | |
| Bit 26 | |
| Bit 25 | |
| Bit 24 | |
| Bit 23 | |
| Bit 22 | |
| Bit 21 | |
| Bit 20 | |
| Bit 17-19 | |
| Bit 16 | |
| Bit 15 | |
| Bit 14 | Route D |
| Bit 13 | Route C – Bit 1 |
| Bit 12 | Route C – Bit 0 |
| Bit 11 | Route B – Bit 1 |
| Bit 10 | Route B – Bit 0 |
| Bit 9 | |
| Bit 8 | Route A |
| Bit 7 | |
| Bit 6 | |
| Bit 5 | Channel C and D - Trigger Level ('0'=Active low; '1'=Active high) |
| Bit 4 | Channel C and D - Trigger Enable ('0'=External Trigger Disabled; '1'=Enabled) |
| Bit 3 | |
| Bit 2 | |
| Bit 1 | Channel A and B - Trigger Level ('0'=Active low; '1'=Active high) |
| Bit 0 | Channel A and B - Trigger Enable ('0'=External Trigger Disabled; '1'=Enabled) |

There is one external Trigger signal per pair of ADCs. Channels A and B are coupled together. So are Channels C and D. Each trigger signal can be active high or low.

Data routes can also be configured vie Register 0x1. The following diagram shows all the possibilities (Data go through a pipeline and can be added with each other):
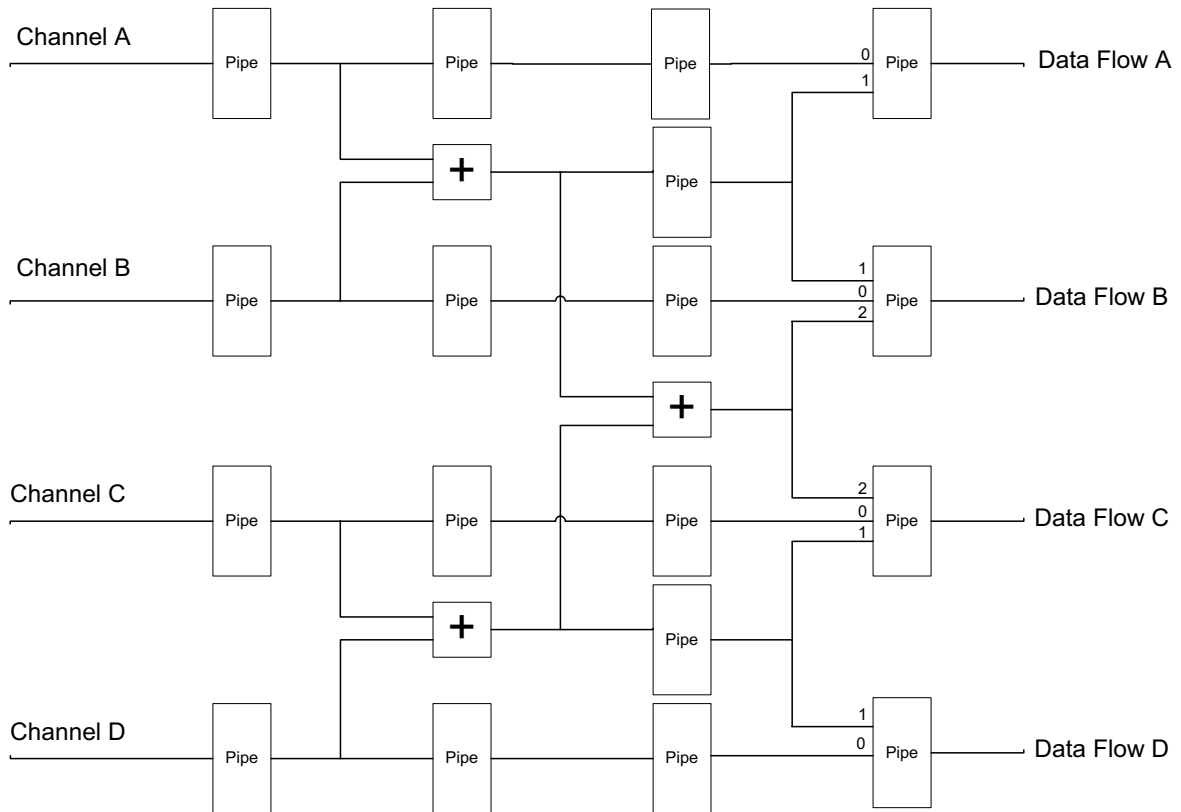
**Figure 10 - Data routing.**

*Register 0x2 –ADCC and ADCD Selection Modes and Decimation factors.*

| Bit number | Description |
|:---:|:---:|
| Bit 31 | 0 |
| Bit 30 | 0 |
| Bit 29 | 1 |
| Bit 28 | 0 |
| Bit 24-27 | |
| Bit 23 | |
| Bit 22 | |
| Bit 21 | Channel D Mode Selection – Bit 1. |
| Bit 20 | Channel D Mode Selection – Bit 0. |
| Bit 19 | Decimation Factor Channel D – Bit 7 |
| Bit 18 | Decimation Factor Channel D – Bit 6 |
| Bit 17 | Decimation Factor Channel D – Bit 5 |
| Bit 16 | Decimation Factor Channel D – Bit 4 |
| Bit 15 | Decimation Factor Channel D – Bit 3 |
| Bit 14 | Decimation Factor Channel D – Bit 2 |
| Bit 13 | Decimation Factor Channel D – Bit 1 |
| Bit 12 | Decimation Factor Channel D – Bit 0 |
| Bit 11 | |
| Bit 10 | |
| Bit 9 | Channel C Mode Selection – Bit 1. |
| Bit 8 | Channel C Mode Selection – Bit 0. |
| Bit 7 | Decimation Factor Channel C – Bit 7 |
| Bit 6 | Decimation Factor Channel C – Bit 6 |
| Bit 5 | Decimation Factor Channel C – Bit 5 |
| Bit 4 | Decimation Factor Channel C – Bit 4 |
| Bit 3 | Decimation Factor Channel C – Bit 3 |
| Bit 2 | Decimation Factor Channel C – Bit 2 |
| Bit 1 | Decimation Factor Channel C – Bit 1 |
| Bit 0 | Decimation Factor Channel C – Bit 0 |

A <u>Decimation Factor</u> of 0 (default value) does not have any effect on the data flow. When it is set to 1, one sample out of two is trimmed out. When it is set to 2, one out of three is trimmed out and so on. The maximum value is 31.

Channel selection:

- "00"=Channel disabled,

- "01"=16-bit counter on clock ADCA,

- "10"=Channel A two's complement encoding, i.e. samples go straight through as ADCs output samples in two's complement 14-bit format. 14-bit samples coming from the ADC are extended to 16-bit on SHBA – Bit13 is copied onto Bits14 and 15.

- "11"=Channel A binary encoding. Binary conversion consists in inverting the MSB of each sample. This operation introduces a DC offset of half the full scale, which can be removed by subtracting 8192 (decimal) of each sample.

*Register 0x3 –ADCA and ADCB Selection Modes and Decimation factors.*

| Bit number | Description |
|---|---|
| Bit 31 | 0 |
| Bit 30 | 0 |
| Bit 29 | 1 |
| Bit 28 | 1 |
| Bit 24-27 | |
| Bit 23 | |
| Bit 22 | |
| Bit 21 | Channel B Mode Selection – Bit 1. |
| Bit 20 | Channel B Mode Selection – Bit 0. |
| Bit 19 | Decimation Factor Channel B – Bit 7 |
| Bit 18 | Decimation Factor Channel B – Bit 6 |
| Bit 17 | Decimation Factor Channel B – Bit 5 |
| Bit 16 | Decimation Factor Channel B – Bit 4 |
| Bit 15 | Decimation Factor Channel B – Bit 3 |
| Bit 14 | Decimation Factor Channel B – Bit 2 |
| Bit 13 | Decimation Factor Channel B – Bit 1 |
| Bit 12 | Decimation Factor Channel B – Bit 0 |
| Bit 11 | |
| Bit 10 | |
| Bit 9 | Channel A Mode Selection – Bit 1. |
| Bit 8 | Channel A Mode Selection – Bit 0. |
| Bit 7 | Decimation Factor Channel A – Bit 7 |
| Bit 6 | Decimation Factor Channel A – Bit 6 |
| Bit 5 | Decimation Factor Channel A – Bit 5 |
| Bit 4 | Decimation Factor Channel A – Bit 4 |
| Bit 3 | Decimation Factor Channel A – Bit 3 |
| Bit 2 | Decimation Factor Channel A – Bit 2 |
| Bit 1 | Decimation Factor Channel A – Bit 1 |
| Bit 0 | Decimation Factor Channel A – Bit 0 |

A <u>Decimation Factor</u> of 0 (default value) does not have any effect on the data flow. When it is set to 1, one sample out of two is trimmed out. When it is set to 2, one out of three is trimmed out and so on. The maximum value is 31.

Channel selection:

- "00"=Channel disabled,

- "01"=16-bit counter on clock ADCA,

- "10"=Channel A two's complement encoding, i.e. samples go straight through as ADCs output samples in two's complement 14-bit format. 14-bit samples coming from the ADC are extended to 16-bit on SHBA – Bit13 is copied onto Bits14 and 15.

- "11"=Channel A binary encoding. Binary conversion consists in inverting the MSB of each sample. This operation introduces a DC offset of half the full scale, which can be removed by subtracting 8192 (decimal) of each sample.

### *Register 0xD – FPGA Global Reset.*

| Bit number | Description |
|---|---|
| Bit 31 | 1 |
| Bit 30 | 1 |
| Bit 29 | 0 |
| Bit 28 | 1 |
| Bit  27-0 | Not Used. |

By sending this control word, the FPGA gets reset. Every single register in the FPGA is reset. The FPGA transmit that command to the:

- Clock synthesizers, which keep the internal register values but does not output any signal,

- Clock multiplexers, which take there default state (external clocks routed to ADCs)

- The interface implemented in the FPGA, including CommPort interface. It is note recommended to proceed to an FPGA global reset while communications are happening. It might stick the other end into an unknown state.


After a Reset command, the SMT364 expects receiving a dummy ComPort word (any value) and sends one back containing the Firmware version number. It is a way of checking that the firmware is latest and that the board is responding and ready to work. The format of that ComPort word is as follow:

0xFF364Fxy, which means FPGA firmware version x.y

### *Register 0xF – Serial Interfaces load.*

| Bit number | Description |
|---|---|
| Bit 31 | 1 |
| Bit 30 | 1 |
| Bit 29 | 1 |
| Bit 28 | 1 |
| Bit 27-0 | Not Used. |

The clock synthesizers have all a **S**erial **P**ort **I**nterface. By sending this control word, the FPGA serialises Register 0x0 and sends it to both clock synthesizers.

## *SMT364* **package.**

The *SMT364* comes with an install package (*SMT6600*) that contain examples and a C header file.

When ordered with either an *SMT365* or *SMT365E* or *SMT374*, it comes with a Pegasus application and a 3L application.