Unit / Module Name:	Quad 125-MSPS ADC Module
Unit / Module Number:	SMT384
Used On:	SMT368 and other SLB base modules
Document Issue:	1.5
Date:	13/02/2006

CONFIDENTIAL

Approvals		Date
Managing Director		
Software Manager		
Design Engineer		

Certificate Number FM 55022

Revision History

	Changes Made	Issue	Initials
08/10/05	**Original Document.**	**1.0**	**PSR**
09/10/05	**SLB pinout corrections added**	**1.1**	**PSR**
02/12/05	**Typo corrections added**	**1.2**	**PSR**
13/02/06	**Layout added and input levels corrected.**	**1.3**	**PSR**
23/02/06	**Input stage (DC option) opamp gain added, rewording, AD9510 as default clock distribution chip.**	**1.4**	**PSR**
28/02/06	**Details added to ADC DC input stage**	**1.5**	**PSR**

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1 Introduction

1.1 Overview

The *SMT384* is a single width expansion TIM that plugs onto the SLB base module SMT368 (Virtex-4 FPGA or other SLB base module) and incorporates 4 Texas Instrument Analog-to-Digital Converters (ADS5500) and a comprehensive clock circuitry based on an AD9510 (Analog Devices) chip that allows synchronisation among the converters and cascading modules for multiple receiver systems as well as the use of an external reference clock. It provides a multi-channel acquisition solution.

ADCs are 14-bit and can sample at up to 125 MHz. All converters are 3.3-Volt. As a standard, the ADCs are all AC-coupled (RF Transformers), but can also be optionally DC-coupled (TI opamp THS4509).

The Xilinx FPGA on the base module is responsible for handling data or control commands coming from the TI converters, **C**omports (TIM-40 standard), **S**undance **H**igh-speed **B**us (SHB). These interfaces are compatible with a wide range of Sundance's modules.

Converter configuration, sampling and transferring modes are set via internal control registers stored inside the FPGA and accessible via Comport.

1.2 Module features

The main features of the *SMT384* are listed below:

- Quad 14-bit 125MSPS ADC (ADS5500),

- On-board low-jitter clock generation (AD9510),

- One external clocks, two external triggers and one reference clock via MMCX connector,

- One SLB connector to link *SMT384* and the base SLB module,

- Synchronisation signals,

- All Analogue inputs to be connected to 50-Ohm sources/loads.

- Temperature sensors.

1.3 Possible applications

The *SMT384* can be used for the following application (this non-exhaustive list should be taken as an example):

- High Intermediate-Frequency (IF) sampling architecture,

- Cellular base station such as CDMA and TDMA,

- Baseband I&Q systems,

- Wireless communication systems,

- Communication instrumentation,

- ...

1.4 Related Documents

ADS5500 Datasheet – Texas Instrument:

http://focus.ti.com/docs/prod/folders/print/ads5500.html

AD9510 Datasheet – Analog Devices:

http://www.analog.com/en/prod/0,2877,AD9510,00.html

Sundance **H**igh-speed **B**us (*SHB*) specifications – Sundance.

ftp://ftp2.sundance.com/Pub/documentation/pdf-files/SHB_Technical_Specification.pdf

Sundance **L**VDS **B**us (SLB) specifications – Sundance.

http://www.sundance.com/docs/SLB%20-%20Technical%20Specifications.pdf

TIM specifications.

ftp://ftp2.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf

MMCX Connectors – Hubert Suhner.

MMCX Connectors

Surface Mount MMCX connector

Sundance Multiprocessor Technology Ltd.

SMT368

2 Functional Description

In this part, we will see the general block diagram and some comments on some the *SMT384* entities.

2.1 Block Diagram

The following diagram describes the architecture of the *SMT384*, coupled – as an example – with an *SMT368* to show how mezzanine and base modules are connected together:
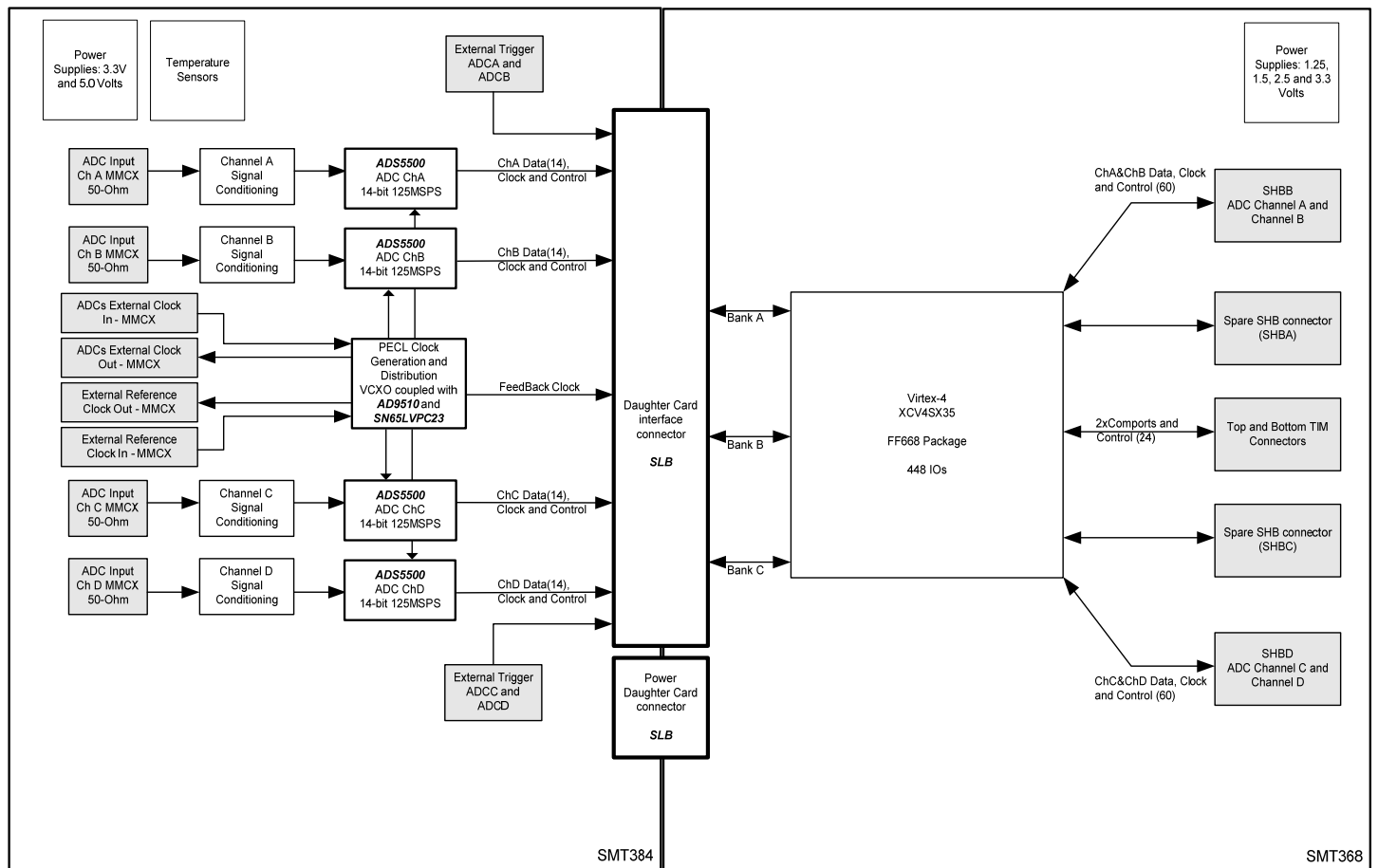
Figure 1 - Block Diagram.

2.2 Module Description

The module is built around four TI ADS5500 14-bit sampling analog-to-digital.

ADCs: Analog data enters the module via four MMCX connectors, one for each channel. Both signals are then conditioned (AC coupling as standard via RF transformers; DC optional via Texas Instrument amplifier THS4509) before being digitized. ADCs get their own sampling clock, which can be either on-board generated or from an external reference or an external clock, common to all ADCs (MMCX connector). Digital samples travel to the FPGA on the base module via the inter-module connector (*SLB* – **S**undance **L**VDS **B**us, used in this case as 'single-ended').

Clock generator and distribution: All samplings clocks are generated by the same chip. It allows having them all synchronized to a single reference clock. The on-board clock uses the VCXO locked on an on-board 10MHz reference. The reference also can be external, in that case the VCXO is still used. In the case of an external clock, the VCXO is no longer used as the AD9510 then acts as a clock multiplexer. In all cases, all sampling clocks are synchronized to the same clock source.

Multi-module Synchronization: *SMT384s* can be cascaded and still be synchronized as either the external reference or the external clock can be passed the next module in the chain. The external reference goes through a 0-delay buffer and is then output. Please note that symchronisation is in frequency and not in phase.

Inter-module Connector: it is made of a power (33 pins) and data connectors (120 pins). It is called **S**undance **L**VDS **B**us. Please refer to the SLB specifications for more details. In the case of the *SMT384*, the SLB is used as 'single-ended'.

A global reset signal is mapped to the FPGA from the bottom TIM connector.

External Clock signals, used to generate Sampling clocks. There is one external clock, common to all four ADCs. When used, the AD9510 is used as a clock multiplexer. Also available, an external reference clock that can be passed to an other *SMT384* (cascaded modules) module with '0-delay'.

External Trigger: passed directly to the base module. There are two, one for each pair of ADCs (Channel A & B and Channel C & D).

Temperature Sensor: available for constant monitoring.

2.3   ADC Channels.

2.3.1   ADC Main Characteristics.

The main characteristics of the *SMT384* ADCs are gathered into the following table.

Analogue Inputs	
Input voltage range	**AC coupled option**. 2.4 Vp-p (11.5 dbm – 50 Ohm) Full scale - AC coupled via RF transformer. **DC coupled option**. 1.15 Vp-p (Gain amplifier 6dB) centered around 0. DC coupled via amplifier. Gain can be adjusted to a required input amplitude centered around 0. Minimm gain 6dBs, which should allow input swing +/-0.575V as full scale.
Impedance	ADC single-ended inputs are to be connected to a 50Ω source. Source impedance matching implemented between RF transformers and ADC.
Bandwidth	ADC bandwidth: 750 MHz.
External Reference Input	
Input Voltage Level	0.5 – 3.3 Volts peak-to-peak (AC-coupled)
Input Impedance	50-Ohm (Termination implemented at the connector)

Frequency Range	0 – 100 MHz.
External Reference Output	
Output Voltage Level	1.6 Volts peak-to-peak (AC-coupled)
Output Impedance	50-Ohm (Termination implemented at the connector)
External Sampling Clock Input	
Input Voltage Level	0.5 – 3.3 Volts peak-to-peak (AC-coupled)
Input Format	Single-ended or differential on option (3.3V LVPECL).
Frequency range	10-125 MHz
External Trigger Inputs	
Input Voltage Level	1.5-3.3 Volts peak-to-peak.
Format	DC-coupled and Single-ended (Termination implemented at the connector). Differential on option (3.3 V PECL).
Impedance	50-Ohm.
Frequency range	62.5 MHz maximum
ADCs **Output**	
Output Data Width	14-Bits
Data Format	2's Complement or offset binary (Changeable via control register)
SFDR	82dBs maximum (manufacturer)
SNR	70dBs maximum (manufacturer)
Minimum Sampling Clock	10 MHz (ADC DLL off)
Maximum Sampling Frequency	125 MHz (ADC DLL on)

Figure 2 - Main features.

2.3.2   ADC Input Stage.

Each ADC Analogue input is AC-coupled via and RF transformer. Both sides of the transformers are balanced so the input is 50-Ohm single-ended.
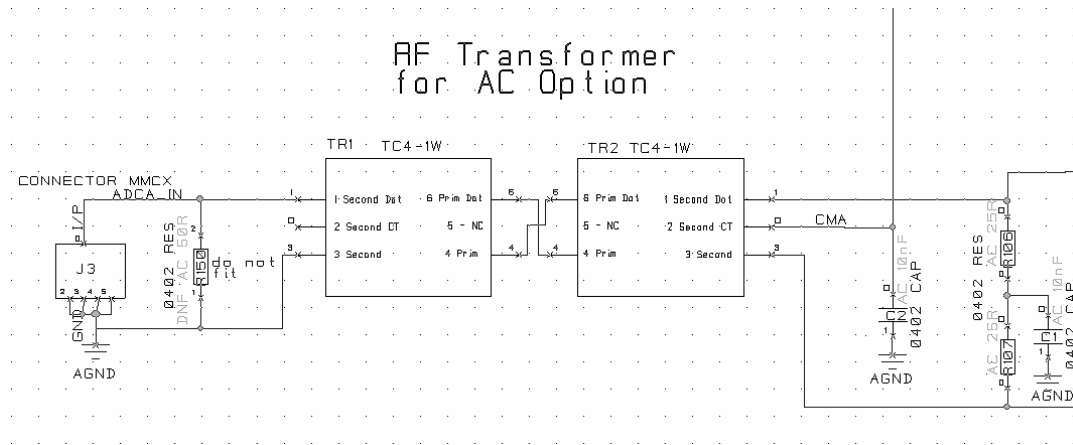
Figure 3 - ADC Input Stage (AC-coupling).

2.4 Clock Structure

There is one integrated clock generator on the module (AD9510 – Analog Devices). The user can either use this clock (on-board) or provide the module with an external clock (input via MMCX connector).
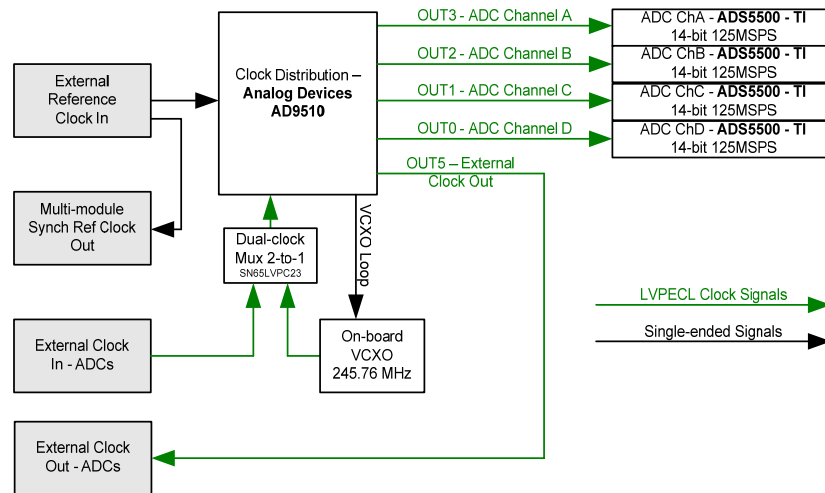
Figure 4 - Clock Structure.

ADCs can all receive the same clock or the integer multiple of it (x2, x3, ...x32), the maximum being 125MHz for each ADC. This clock can be coming from the on-board VCXO or from an external source.

An extra connector outputs the reference clock for multiple-module systems.

Below is shown how the external clock is fed to the system. By default it is single-ended and AC-coupled before being converted into LVPECL format. The option of having a differential external clock is still possible on the hardware by the way of fitting or not some of the components.
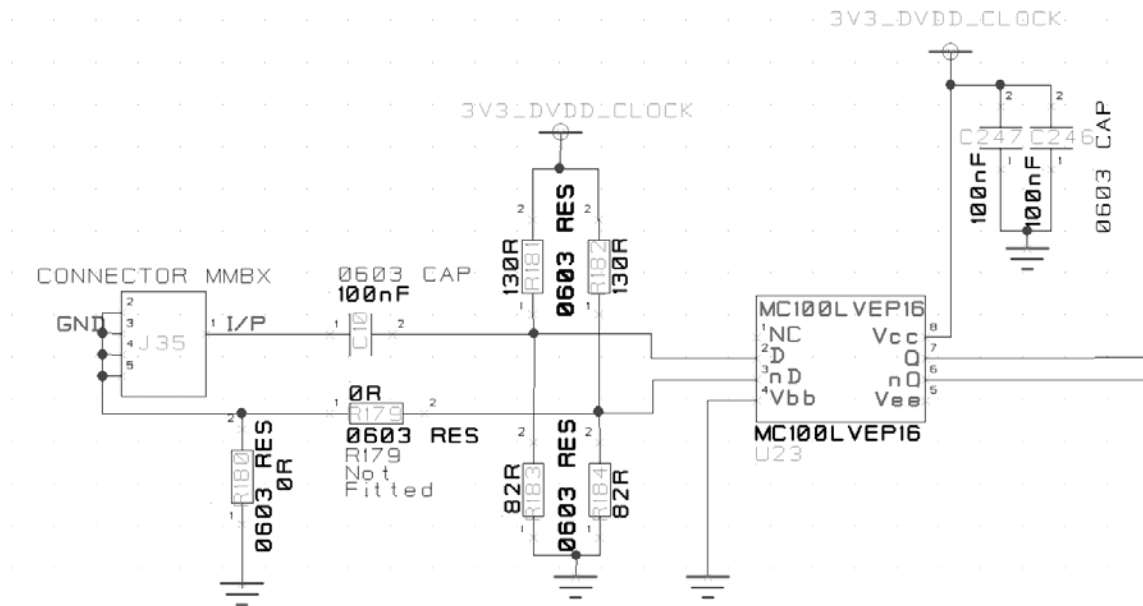
Figure 5 - External Clock.

2.5 Power Supply and Reset Structure

The *SMT384* gets two power sources from the base module: 3.3 and 5 Volts. Linear regulators are used to provide a clean and stable voltage supply to the analog converters. The DC-coupling option uses also -12 Volts.

2.6 Green LEDs.

There are some LEDs on the Daughter Module. Three are dedicated for the power supplies (3.3Volt, 5V ADC Channel A and ADC Channel B). Green LEDs being ON meaning that the supply is under power.

2.7 Mezzanine module Interface

The daughter module interface is made up of two connectors (data and power). The first one is a 0.5mm-pitch differential Samtec connector. This connector is for transferring data such as ADC samples to the FPGA on the main module. The second one is a 1mm-pitch Samtec header type connector. This connector is for providing power to the daughter-card.

Sundance defines these two connectors as the **S**undance **L**VDS **B**us (*SLB*). It has originally been made for data transfers using LVDS format but can also be used with single-ended lines, which is the case for the *SMT384*. To know more about the SLB, please refer to the SLB specifications.

The figure underneath illustrates this configuration. The bottom view of the daughter card is shown on the right. This view must the mirrored to understand how it connects to the main module.

Data connectors
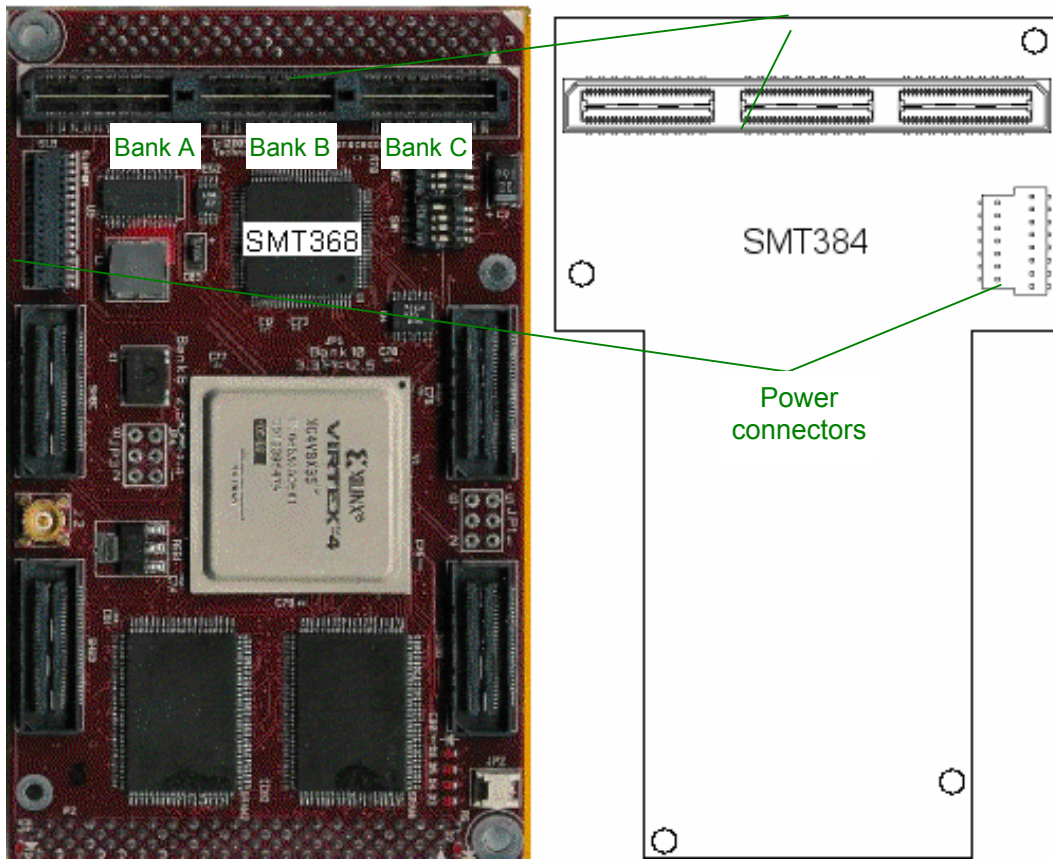
Figure 6 – Mezzanine module Connector Interface (SLB data and power connectors).

The female differential connector is located on the base module. The Samtec Part Number for this connector is QTH-060-01-F-D-DP-A.

The female power connector is located on the base module. The Samtec Part Number for this connector is BKS-133-03-F-V-A

The male differential connector is located on the mezzanine card. The Samtec Part Number for this connector is QSH-060-01-F-D-DP-A

The male power connector is located on the mezzanine card. The Samtec Part Number for this connector is BKT-133-03-F-V-A

The mated height between the main module and the daughter card is 5 mm.

Some JTAG Lines are also mapped onto this connector to be used in case the Daughter module would have a TI Processor. They would allow debugging and programming via JTAG.

The following table shows the pin assignment on the power connector:
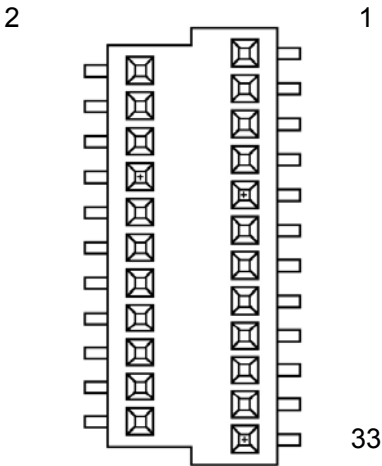
Pin Number	Pin Name	Description of Signal
1	D+3V3	Digital 3.3 Volts
2	DGND	Digital Ground
3	D+3V3	Digital 3.3 Volts
4	DGND	Digital Ground
5	D+3V3	Digital 3.3 Volts
6	DGND	Digital Ground
7	D+3V3	Digital 3.3 Volts
8	DGND	Digital Ground
9	D+5V0	Digital 5.0 Volts
10	DGND	Digital Ground
11	D+5V0	Digital 5.0 Volts
12	DGND	Digital Ground
13	D+5V0	Digital 5.0 Volts
14	DGND	Digital Ground
15	D+5V0	Digital 5.0 Volts
16	DGND	Digital Ground
17	D+12V0	Digital +12.0 Volts – not used on the *SMT384*
18	DGND	Digital Ground
19	D+12V0	Digital +12.0 Volts – not used on the *SMT384*
20	DGND	Digital Ground
21	D-12V0	Digital –12.0 Volts – used on the *SMT384* only for DC option.
22	DGND	Digital Ground
23	D-12V0	Digital –12.0 Volts –used on the *SM384* only for DC option.
24	DGND	Digital Ground
25	DGND	Digital Ground
26	EMU0	Emulation Control 0 – not used on *SMT384*
27	EMU1	Emulation Control 1 – not used on *SMT384*
28	TMS	JTAG Mode Control – not used on *SMT384*
29	nTRST	JTAG Reset – not used on SMT384

30	TCK	JTAG Test Clock – not used on *SMT384*
31	TDI	JTAG Test Input – not used on *SMT384*
32	TDO	JTAG Test Output – not used on *SMT384*
33	DGND	Digital Ground

Figure 7 – Mezzanine Module Interface Power Connector and Pinout.

The following few pages describes the signals on the data connector between the main module and the daughter card. Bank A on the connector is used for the ADC Channels A and B. Bank C is used for the ADC channels C and D. Bank B is used for system clock and trigger signals, ADCs/Clock control signal.

Bank A   Bank B   Bank C

1 3 5 7   41 43   81 83
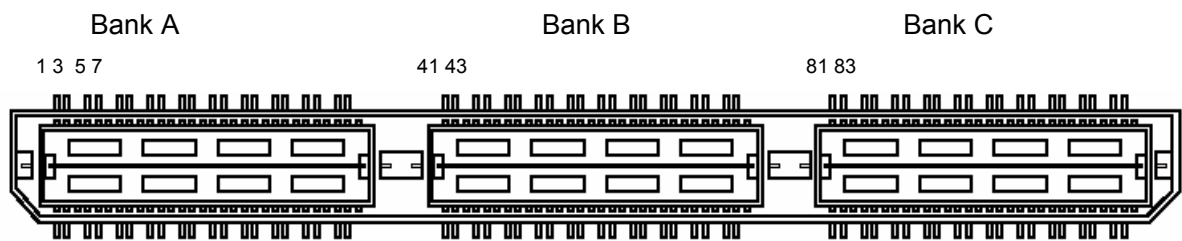
2 4 6 8

Bank A (ADC A and B)

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
1	DOAI0p	Data Out 0, Channel A.	2	DOBI0p	Data Out 1, Channel A.
3	DOAI0n	Data Out 2, Channel A.	4	DOBI0n	Data Out 3, Channel A.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
5	DOAI1p	Data Out 4, Channel A.	6	DOBI1p	Data Out 5, Channel A.
7	DOAI1n	Data Out 6, Channel A.	8	DOBI1n	Data Out 7, Channel A.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
9	DOAI2p	Data Out 8, Channel A.	10	DOBI2p	Data Out 9, Channel A.
11	DOAI2n	Data Out 10, Channel A.	12	DOBI2n	Data Out 11, Channel A.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
13	DOAI3p	Data Out 12, Channel A.	14	DOBI3p	Data Out 13, Channel A.
15	DOAI3n	Over Range, Channel A.	16	DOBI3n	Data Out 0, Channel B.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
17	DOAI4p	Data Out 1, Channel B.	18	DOBI4p	Data Out 2, Channel B.
19	DOAI4n	Data Out 3, Channel B.	20	DOBI4n	Data Out 4, Channel B.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
21	DOAI5p	Data Out 5, Channel B.	22	DOBI5p	Data Out 6, Channel B.
23	DOAI5n	Data Out 7, Channel B.	24	DOBI5n	Data Out 8, Channel B.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
25	DOAI6p	Data Out 9, Channel B.	26	DOBI6p	Data Out 10, Channel B.
27	DOAI6n	Data Out 11, Channel B.	28	DOBI6n	Data Out 12, Channel B.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
29	DOAI7p	Data Out 13, Channel B.	30	DOBI7p	Over Range, Channel B.
31	DOAI7n	Led ADC A and B.	32	DOBI7n	Status Lock AD9510
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
33	ClkOIp	Data Clock Out, Channel A.	34	DOIRIp	Status Ref AD9510
35	ClkOIn	Data Clock Out, Channel B.	36	DOIRIn	Status VCXO AD9510
Dir	Reserved.		Dir	Reserved.	
37	Reserved.	Reserved.	38	Reserved	ADC A and B External Trigger, P.
39	Reserved.	Reserved.	40	Reserved	ADC A and B External Trigger, N.

Figure 8 – Daughter Module Interface: Data Signals Connector and Pinout (Bank A).

Bank A   Bank B   Bank C
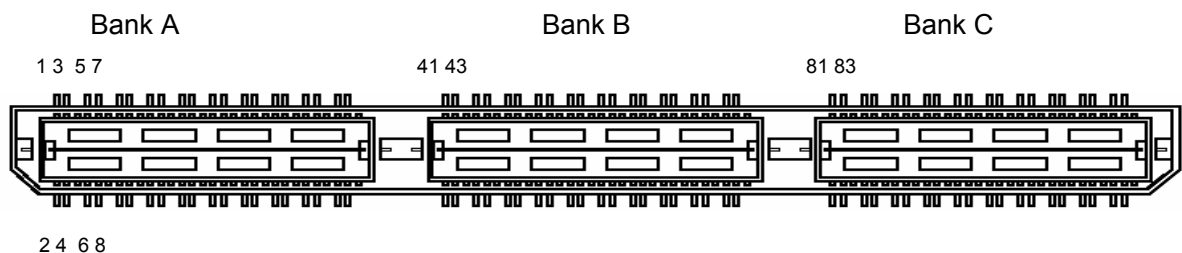
Bank B

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Type	**Clock and Trigger System Signals**		**Type**	**Clock and Trigger System Signals**	
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
41	SMBClk	Temperature Sensor Clock.	42	SMBData	Temperature Sensor Data.
43	SMBnAlert	Temperature Sensor Alert.	44	SerialNo	Reserved
Dir	Daughter Card to Main Module		Dir	Reserved	
45	AdcVDacI	Reserved	46	AdcVDacQ	Reserved
47	AdcVRes	Reserved	48	AdcReset	AD9510 Function
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
49	D3v3Enable	Reserved	50	D2v5Enable	Reserved
51	AdcMode	ADCA Serial Clock.	52	AdcClock	ADCA Serial Data.
Type	**ADC Specific Signals**		**Type**	**ADC Specific Signals**	
Dir	Main Module to Daughter Card		Dir	Reserved	
53	AdcLoad	ADCA Serial Enable.	54	AdcData	ADCB Serial Clock.
55	AdcCal	ADCB Serial Data.	56	AdjClkCntr0	ADCB Serial Enable.
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
57	AdjClkCntr1	ADC A and B Format (binary, 2's).	58	AdjClkCntr2	ADC A and B Reset.
59	AdjClkCntr3	ADC A and B Output Enable.	60	PllCntr0	AD9510 serial Enable.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
61	PllCntr1	AD9510 serial Clock.	62	PllCntr2	AD9510 serial Data.
63	PllCntr3	AD9510 Clock Selection.	64	AdcAClkSel	ADCC Serial Clock.
Type	**Module Control Signals**		**Type**	**Module Control Signals**	
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
65	AdcBClkSel	ADCC Serial Data.	66	IntClkDivEn	ADCC Serial Enable.
67	IntClkDivnReset	ADCD Serial Clock.	68	IntExtClkDivEn	ADCD Serial Data.
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
69	IntExtClkDivnReset	ADCD Serial Enable.	70	FpgaVRef	Reserved
71	FpgaTck	Reserved	72	FpgaTms	Reserved
Dir	Daughter Card to Main Module		Dir	Reserved	
73	FpgaTdi	Reserved	74	FpgaTdo	Reserved
75	MspVRef	Reserved	76	MspTck	Reserved
Dir	Daughter Card to Main Module		Dir	Reserved	
77	MspTms	Reserved	78	MspTdi	Reserved.
79	Msptdo	Reserved	80	MspnTrst	Reserved

Figure 9 – Daughter Module Interface: Data Signals Connector and Pinout (Bank B).

Bank A   Bank B   Bank C
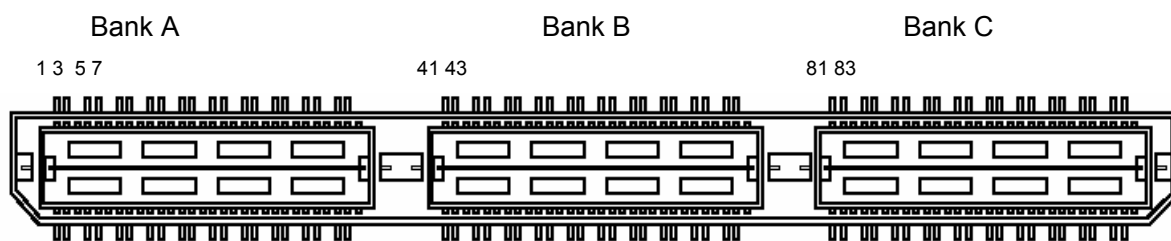
Bank C (ADC C and D)

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
81	DOAQ0p	Data Out 0, Channel C.	82	DOBQ0p	Data Out 1, Channel C.
83	DOAQ0n	Data Out 2, Channel C.	84	DOBQ0n	Data Out 3, Channel C.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
85	DOAQ1p	Data Out 4, Channel C.	86	DOBQ1p	Data Out 5, Channel C.
87	DOAQ1n	Data Out 6, Channel C.	88	DOBQ1n	Data Out 7, Channel C.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
89	DOAQ2p	Data Out 8, Channel C.	90	DOBQ2p	Data Out 9, Channel C.
91	DOAQ2n	Data Out 10, Channel C.	92	DOBQ2n	Data Out 11, Channel C.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
93	DOAQ3p	Data Out 12, Channel C.	94	DOBQ3p	Data Out 13, Channel C.
95	DOAQ3n	Over Range, Channel C.	96	DOBQ3n	Data Out 0, Channel D.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
97	DOAQ4p	Data Out 1, Channel D.	98	DOBQ4p	Data Out 2, Channel D.
99	DOAQ4n	Data Out 3, Channel D.	100	DOBQ4n	Data Out 4, Channel D.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
101	DOAQ5p	Data Out 5, Channel D.	102	DOBQ5p	Data Out 6, Channel D.
103	DOAQ5n	Data Out 7, Channel D.	104	DOBQ5n	Data Out 8, Channel D.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
105	DOAQ6p	Data Out 9, Channel D.	106	DOBQ6p	Data Out 10, Channel D.
107	DOAQ6n	Data Out 11, Channel D.	108	DOBQ6n	Data Out 12, Channel D.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
109	DOAQ7p	Data Out 13, Channel D.	110	DOBQ7p	Over Range, Channel D.
111	DOAQ7n	Led ADC C and D.	112	DOBQ7n	ADC C and D Format (binary, 2's).
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
113	ClkOIp	Data Clock Out, Channel C.	114	DOIRIp	ADC C and D Reset.
115	ClkOIn	Data Clock Out, Channel D.	116	DOIRIn	ADC A and B Output Enable.
Dir	Reserved.		Dir	Reserved.	
117	Reserved.	Reserved.	118	Reserved	ADC C and D External Trigger, P.
119	Reserved.	Reserved.	120	Reserved	ADC C and D External Trigger, N.

Figure 10 – Daughter Module Interface: Data Signals Connector and Pinout (Bank C).

3   Control Register Settings

The Control Registers control the complete functionality of the *SMT384*. They are setup via the Comport0 or 3. The settings of the ADC, triggers, clocks and the configuration of the SHB interfaces and the internal FPGA data path settings can be configured via the Control Registers.

3.1   Control Packet Structure

The data passed on to the *SMT384* over the Comports must conform to a certain packet structure. Only valid packets will be accepted and only after acceptance of a packet will the appropriate settings be implemented. Each packet will start with a certain sequence indicating the start of the packet (0xFF). The address to write the data payload into will follow next. After the address the data will follow. This structure is illustrated in the following figure:

Byte	Byte Content							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'
1	Address 7	Address 6	Address 5	Address 4	Address 3	Address 2	Address 1	Address 0
3	Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
4	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0

Figure 11 – Setup Packet Structure.

3.2   Reading and Writing Registers

Control packets are sent to the *SMT384* over Comport 0 or 3. This is a bi-directional interface. The format of a 'Read Packet' is the same as that of a write packet.

1) Write Packet

Byte 0	Fixed Sequence
Byte 1	Read/Write Address
Byte 3	Read/Write Data
Byte 4	Read/Write Data

Host

ComPort 0 or 3

SMT384
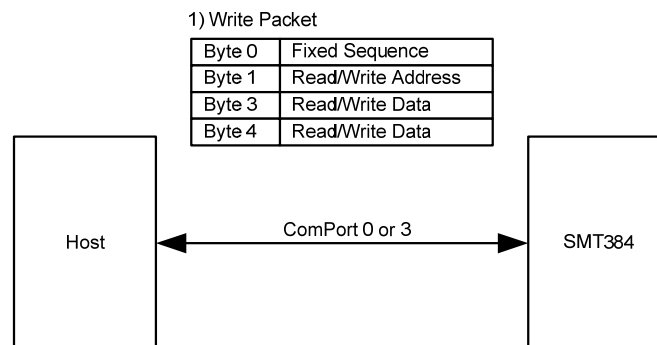
Figure 12 – Control Register Read Sequence.

3.3 Memory Map

The write packets must contain the address where the data must be written to and the read packets must contain the address where the required data must be read. The following figure shows the memory map for the writable and readable Control Registers on the *SMT384:*

Address	Writable Registers	Readable Registers
0x00	Reset Register.	Reserved.
0x01	Test Register.	Reserved.
0x02	ADCA Register 0.	Read-back ADCA Register 0.
0x03	ADCA Register 1.	Read-back ADCA Register 1.
0x04	ADCA Register 2.	Read-back ADCA Register 2.
0x05	ADCB Register 0.	Read-back ADCB Register 0.
0x06	ADCB Register 1.	Read-back ADCB Register 1.
0x07	ADCB Register 2.	Read-back ADCB Register 2.
0x08	ADCC Register 0.	Read-back ADCC Register 0.
0x09	ADCC Register 1.	Read-back ADCC Register 1.
0x0A	ADCC Register 2.	Read-back ADCC Register 2.
0x0B	ADCD Register 0.	Read-back ADCD Register 3.
0x0C	ADCD Register 1.	Read-back ADCD Register 4.
0x0D	ADCD Register 2.	Read-back ADCD Register 5.
0x0E		
0x0F		
0x18	Reserved	Main Module Temperature
0x19	Reserved	Main Module FPGA Temperature
0x1A	Reserved	Mezzanine Module Temperature
0x1B	Reserved	Mezzanine Module Converter Temperature
0x1C	Misc Register (Trigger, Clock Selection, etc…).	Read- Misc Register.
0x1D	Update and Read-back command Register	Firmware Version and Status bits.
0x30	AD9510 Register 0x0.	Read-back AD9510 Register 0.
0x31	AD9510 Register 0x1.	Read-back AD9510 Register 1.
0x32	AD9510 Register 0x2.	Read-back AD9510 Register 2.
0x33	AD9510 Register 0x3.	Read-back AD9510 Register 3.
0x34	AD9510 Register 0x4.	Read-back AD9510 Register 4.
0x35	AD9510 Register 0x5.	Read-back AD9510 Register 5.
0x36	AD9510 Register 0x6.	Read-back AD9510 Register 6.
0x37	AD9510 Register 0x7.	Read-back AD9510 Register 7.
0x38	AD9510 Register 0x8.	Read-back AD9510 Register 8.
0x39	AD9510 Register 0x9.	Read-back AD9510 Register 9.
0x3A	AD9510 Register 0xA.	Read-back AD9510 Register A.
0x3B	AD9510 Register 0xB.	Read-back AD9510 Register B.
0x3C	AD9510 Register 0xC.	Read-back AD9510 Register C.
0x3D	AD9510 Register 0xD.	Read-back AD9510 Register D.
0x3E	AD9510 Register 0xE.	Read-back AD9510 Register E.
0x3F	AD9510 Register 0xF.	Read-back AD9510 Register F.

0x40	AD9510 Register 0x10.	Read-back AD9510 Register 10.
0x41	AD9510 Register 0x11.	Read-back AD9510 Register 11.
0x42	AD9510 Register 0x12.	Read-back AD9510 Register 12.
0x43	AD9510 Register 0x13.	Read-back AD9510 Register 13.
0x44	AD9510 Register 0x14.	Read-back AD9510 Register 14.
0x45	AD9510 Register 0x15.	Read-back AD9510 Register 15.
0x46	AD9510 Register 0x16.	Read-back AD9510 Register 16.
0x47	AD9510 Register 0x17.	Read-back AD9510 Register 17.
0x48	AD9510 Register 0x18.	Read-back AD9510 Register 18.
0x49	AD9510 Register 0x19.	Read-back AD9510 Register 19.

Figure 13 – Register Memory Map.

3.4   Register Descriptions

3.4.1   Reset Register – 0x0.

	Reset Register – 0x0							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved	SHB Reset	Reserved	Reserved	Reserved	AD9510 Reset	ADC C&D Reset	ADC A&B Reset
Default	'0'	'0'	'0'	'0'	'0'	'1'	'1'	'1'

	Reset Register – 0x0	
Setting	**Bit 0**	**Description**
0	0	Normal Operation.
1	1	Resets both ADC devices as well as their corresponding Serial Interfaces.
Setting	**Bit 1**	**Description**
0	0	Normal Operation.
1	1	Resets both ADC devices as well as their corresponding Serial Interfaces.
Setting	**Bit 2**	**Description**
0	0	Normal Operation.
1	1	Resets Clock device as well as its Serial Interfaces.
Setting	**Bit 6**	**Description**
0	0	Normal Operation.
1	1	Resets SHB (ADC) interface – including SHB FIFO.

Note: The Reset bits don't get cleared automatically, so a device can remain reset while not used to reduce the global power consumption.

3.4.2 Test Register – 0x1.

Any 16-bit value written in this register can be read-back to check that the Comport used works properly.

	Test Register – 0x1							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0								
1								

3.4.3 ADCA Register 0 – 0x2.

For more details, refer to ADS5500 datasheet.

	ADCA Register 0 – 0x2							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved							
Default	'0000000'							
0	Reserved						PLL	Reserved
Default	'000000'						'0'	'0'

	ADCA Register 0 – 0x2	
Setting	**Bit 1**	**Description**
0	0	PLL ON – for sampling frequencies between 60 and 125 MHz
1	1	PLL OFF – for sampling frequencies between 10 and 80 MHz

3.4.4 ADCA Register 1 – 0x3.

For more details, refer to ADS5500 datasheet.

	ADCA Register 1 – 0x3							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved					TP1	TP0	Reserved
Default	'000000'					'0'	'0'	'0'
0	Reserved							
Default	'00000000'							

	ADCA Register 1 – 0x3		
Setting	**TP1**	**TP0**	**Description**
0	0	0	Normal Mode of Operation
1	0	1	All outputs are zeroes
2	1	0	All outputs are ones
3	1	1	Continuous stream of '10'

3.4.5 ADCA Register 2 – 0x4.

For more details, refer to ADS5500 datasheet.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	ADCA Register 2 – 0x4							
1	Reserved				PDN	Reserved		
Default	'0000'				'0'	'000'		
0	Reserved							
Default	'00000000'							

	ADCA Register 2 – 0x4		
Setting	PDN	Description	
0	0	Normal Mode of Operation	
1	1	Device in Power Down Mode	

3.4.6 ADCB Register 0 – 0x5.

For more details, refer to ADS5500 datasheet.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	ADCB Register 0 – 0x5							
1	Reserved						1	Reserved
Default	'0000000'						Default	'0000000'
0	Reserved						PLL	Reserved
Default	'000000'						'0'	'0'

	ADCB Register 0 – 0x5		
Setting	Bit 1	Description	
0	0	PLL OFF – for sampling frequencies between 10 and 80 MHz	
1	1	PLL ON – for sampling frequencies between 60 and 125 MHz	

3.4.7 ADCB Register 1 – 0x6.

For more details, refer to ADS5500 datasheet.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	ADCB Register 1 – 0x6							
1	Reserved					TP1	TP0	Reserved
Default	'000000'					'0'	'0'	'0'
0	Reserved							
Default	'00000000'							

	ADCB Register 1 – 0x6		
Setting	TP1	TP0	Description
0	0	0	Normal Mode of Operation
1	0	1	All outputs are zeroes
2	1	0	All outputs are ones
3	1	1	Continuous stream of '10'

3.4.8 ADCB Register 2 – 0x7.

For more details, refer to ADS5500 datasheet.

	ADCB Register 2 – 0x7							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved				PDN	Reserved		
Default	'0000'				'0'	'000'		
0	Reserved							
Default	'00000000'							

	ADCB Register 2 – 0x7	
Setting	**PDN**	**Description**
0	0	Normal Mode of Operation
1	1	Device in Power Down Mode

3.4.9 ADCC Register 0 – 0x8.

For more details, refer to ADS5500 datasheet.

	ADCB Register 0 – 0x8							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved						**1**	Reserved
Default	'0000000'						**Default**	'0000000'
0	Reserved						PLL	Reserved
Default	'000000'						'0'	'0'

	ADCC Register 0 – 0x8	
Setting	**Bit 1**	**Description**
0	0	PLL OFF – for sampling frequencies between 10 and 80 MHz
1	1	PLL ON – for sampling frequencies between 60 and 125 MHz

3.4.10 ADCC Register 1 – 0x9.

For more details, refer to ADS5500 datasheet.

	ADCB Register 1 – 0x9							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved					TP1	TP0	Reserved
Default	'000000'					'0'	'0'	'0'
0	Reserved							
Default	'00000000'							

	ADCC Register 1 – 0x9		
Setting	**TP1**	**TP0**	**Description**
0	0	0	Normal Mode of Operation
1	0	1	All outputs are zeroes
2	1	0	All outputs are ones

3	1	1	Continuous stream of '10'

3.4.11 ADCC Register 2 – 0xA.

For more details, refer to ADS5500 datasheet.

	ADCC Register 2 – 0xA							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved				PDN	Reserved		
Default	'0000'				'0'	'000'		
0	Reserved							
Default	'00000000'							

	ADCC Register 2 – 0xA	
Setting	PDN	Description
0	0	Normal Mode of Operation
1	1	Device in Power Down Mode

3.4.12 ADCD Register 0 – 0xB.

For more details, refer to ADS5500 datasheet.

	ADCD Register 0 – 0xB							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved						**1**	Reserved
Default	'0000000'						**Default**	'0000000'
0	Reserved						PLL	Reserved
Default	'000000'						'0'	'0'

	ADCD Register 0 – 0xB	
Setting	Bit 1	Description
0	0	PLL OFF – for sampling frequencies between 10 and 80 MHz
1	1	PLL ON – for sampling frequencies between 60 and 125 MHz

3.4.13 ADCD Register 1 – 0xC.

For more details, refer to ADS5500 datasheet.

	ADCD Register 1 – 0xC							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved					TP1	TP0	Reserved
Default	'000000'					'0'	'0'	'0'
0	Reserved							
Default	'00000000'							

	ADCD Register 1 – 0xC		
Setting	TP1	TP0	Description
0	0	0	Normal Mode of Operation

1	0	1	All outputs are zeroes
2	1	0	All outputs are ones
3	1	1	Continuous stream of '10'

3.4.14 ADCD Register 2 – 0xD.

For more details, refer to ADS5500 datasheet.

	ADCD Register 2 – 0xD							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved				PDN	Reserved		
Default	'0000'				'0'	'000'		
0	Reserved							
Default	'00000000'							

	ADCD Register 2 – 0xD	
Setting	PDN	Description
0	0	Normal Mode of Operation
1	1	Device in Power Down Mode

3.4.15 Main Module Temperature – 0x18

	Main Module Temperature – 0X18							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Temperature in Degrees Celsius							
Default	'00000000'							

3.4.16 Main Module FPGA Temperature – 0x19

	Main Module FPGA Temperature – 0X19							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Temperature in Degrees Celsius							
Default	'00000000'							

3.4.17 Mezzanine Module Temperature – 0x1A

	Mezzanine Module Temperature – 0X1A							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Temperature in Degrees Celsius							
Default	'00000000'							

3.4.18 Mezzanine Module Converters Temperature – 0x1B

	Mezzanine Module Converters Temperature – 0X1B							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Temperature in Degrees Celsius							
Default	'00000000'							

3.4.19 Miscellaneous Register – 0x1C.

	Miscellaneous Register – 0X1C							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved		ADC C and D Trigger		ADC A and B Trigger		Clock Selection	Reference Selection
Default	'00'		'00'		'00'		'0'	'0'
1	ADC C and D Decimation Factor				ADCA and B Decimation Factor			
Default	'0000'				'0000'			

	Miscellaneous Register – 0x1C	
Setting	**Bit 1**	**Description**
0	0	VCXO selection.
1	1	External Source Selected.
	Miscellaneous Register – 0x1C	
Setting	**Bit 0**	**Description**
0	0	On-Board 10-MHz Reference Clock selected.
1	1	External Reference Selected.

3.4.20 Updates, Read-back and Firmware Version Registers – 0x1D

The Update bit activates the corresponding Serial Interface to pass registers previously written in the FPGA, into the corresponding device (ADCA, ADCB, ADCC, ADCD or CLK devices).

	Update and Read-back commands – 0x1D							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved	Reserved	Reserved	Reserved	CLK Update	Reserved	ADCC&D Update	ADCA&B Update
Default	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
1					Reserved	Reserved		
Default	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

Reading-back this register returns the Firmware version as well as some Status signals coming from theAD9510.

	Firmware Version – 0x1D							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Firmware Version							
Default	'00000000'							
1								AD9510 Status Lock

| Default | '0' | '0' | '0' | '0' | '0' | '0' | '0' | '0' |

3.4.21 AD9510 Register 0 – 0x30.

For more details, refer to AD9510 datasheet.

	AD9510 Register 0 – 0x30							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used							
Default	'00000000'							
0	SDO Inactive	LSB First	Soft Reset	Long Inst.	Not Used			
Default	'0'	'0'	'0'	'1'	'0000'			

3.4.22 AD9510 Register 1 – 0x31.

For more details, refer to AD9510 datasheet.

	AD9510 Register 1 – 0x31							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used							
Default	'00000000'							
0	Not Used							
Default	'00000000'							

3.4.23 AD9510 Register 2 – 0x32.

For more details, refer to AD9510 datasheet.

	AD9510 Register 2 – 0x32							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used			13-bit B Counter (12…8)				
Default	'000'			'00000'				
0	Not Used		6-bit A Counter					
Default	'00'		'000000'					

3.4.24 AD9510 Register 3 – 0x33.

For more details, refer to AD9510 datasheet.

	AD9510 Register 3 – 0x33							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used	LOR Lock_Del		Not Used		LOR Enable	Not Used	
Default	'0'	'00'		'00'		'0'	'00'	
0	13-bit B Counter (7…0)							
Default	'00000000'							

3.4.25 AD9510 Register 4 – 0x34.

For more details, refer to AD9510 datasheet.

	AD9510 Register 4 – 0x34

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used	CP Current			Not Used	Reset R Counter	Reset N Counter	Reset all Counters
Default	'0'	'000'			'0'	'0'	'0'	'0'
0	Not Used	PFD Polarity	PLL Mux Select				CP Mode	
Default	'0'	'0'	'0000'				'00'	

3.4.26 AD9510 Register 5 – 0x35.

For more details, refer to AD9510 datasheet.

	AD9510 Register 5 – 0x35							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used		14-bit R Divider (13…8)					
Default	'00'		'000000'					
0	Not Used	B Bypass	Not Used	Prescaler P			Power Down	
Default	'0'	'0'	'0'	'000'			'01'	

3.4.27 AD9510 Register 6 – 0x36.

For more details, refer to AD9510 datasheet.

	AD9510 Register 0 – 0x30							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used	Digital Lock Det Enable	Digital Lock Det. Window	Not Used			Antibacklash	
Default	'0'	'0'	'0'	'000'			'00'	
0	14-bit R Divider (7…0)							
Default	'00000000'							

3.4.28 AD9510 Register 7 – 0x37.

For more details, refer to AD9510 datasheet.

	AD9510 Register 7 – 0x37							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used		Ramp Capacitor 5			Ramp Current 5		
Default	'0'		'000'			'000'		
0	Not Used							Bypass 5
Default	'0000000'							'1'

3.4.29 AD9510 Register 8 – 0x38.

For more details, refer to AD9510 datasheet.

	AD9510 Register 8 – 0x38							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used							
Default	'00000000'							

0	Not Used		5-bit Fine Delay 5			Must be '0'
Default	'00'		'00000'			'0'

3.4.30 AD9510 Register 9 – 0x39.

For more details, refer to AD9510 datasheet.

	AD9510 Register 9 – 0x39							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used		Ramp Capacitor 6			Ramp Current 6		
Default	'0'		'000'			'000'		
0	Not Used							Bypass 6
Default	'0000000'							'1'

3.4.31 AD9510 Register A – 0x3A.

For more details, refer to AD9510 datasheet.

	AD9510 Register A – 0x3A							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used							
Default	'00000000'							
0	Not Used		5-bit Fine Delay 6					Must be '0'
Default	'00'		'00000'					'0'

3.4.32 AD9510 Register 0 – 0x3B.

For more details, refer to AD9510 datasheet.

	AD9510 Register B – 0x3B							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used				Output Level 1		Power Down 1	
Default	'0000'				'00'		'00'	
0	Not Used				Output Level 0		Power Down 0	
Default	'0000'				'00'		'00'	

3.4.33 AD9510 Register 0 – 0x3C.

For more details, refer to AD9510 datasheet.

	AD9510 Register C – 0x3C							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Not Used				Output Level 3		Power Down 3	
Default	'0000'				'00'		'00'	
0	Not Used				Output Level 2		Power Down 2	
Default	'0000'				'00'		'00'	

3.4.34 AD9510 Register D – 0x3D.

For more details, refer to AD9510 datasheet.

	AD9510 Register D – 0x3D							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Not Used			CMOS Inv 5	Logic Select 5	Output Level 5		Output Power 5
Default	'000'			'0'	'0'	'01'		'0'
0	Not Used			CMOS Inv 4	Logic Select 4	Output Level 4		Output Power 4
Default	'000'			'0'	'0'	'01'		'0'

3.4.35 AD9510 Register E – 0x3E.

For more details, refer to AD9510 datasheet.

	AD9510 Register E – 0x3E							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Not Used			CMOS Inv 7	Logic Select 7	Output Level 7		Output Power 7
Default	'000'			'0'	'0'	'01'		'0'
0	Not Used			CMOS Inv 6	Logic Select 6	Output Level 6		Output Power 6
Default	'000'			'0'	'0'	'01'		'0'

3.4.36 AD9510 Register F – 0x3F.

For more details, refer to AD9510 datasheet.

	AD9510 Register F – 0x3F							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Not Used		CLKs in PD	REF IN PD	Prescaler PD	CLK2 PD	CLK1 PD	Sel CLKIN
Default	'00'		'0'	'0'	'0'	'0'	'0'	'1'
0	Not Used							
Default	'00000000'							

3.4.37 AD9510 Register 10 – 0x40.

For more details, refer to AD9510 datasheet.

	AD9510 Register 10 – 0x40							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Bypass 0	No Synch 0	Force 0	Start H/L 0	Phase Offset 0			
Default	'0'	'0'	'0'	'0'	'0000'			
0	Low Cycles 0				High Cycles 0			
Default	'0000'				'0000'			

3.4.38 AD9510 Register 11 – 0x41.

For more details, refer to AD9510 datasheet.

	AD9510 Register 11 – 0x41							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Bypass 1	No Synch 1	Force 1	Start H/L 1	Phase Offset 1			

	Bit 7	Bit 6	Bit 5	Bit 4				
Default	'0'	'0'	'0'	'0'	'0000'			
0	Low Cycles 1				High Cycles 1			
Default	'0000'				'0000'			

3.4.39 AD9510 Register 12 – 0x42.

For more details, refer to AD9510 datasheet.

	AD9510 Register 12 – 0x42							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Bypass 2	No Synch 2	Force 2	Start H/L 2	Phase Offset 2			
Default	'0'	'0'	'0'	'0'	'0000'			
0	Low Cycles 0				High Cycles 2			
Default	'0000'				'0000'			

3.4.40 AD9510 Register 13 – 0x43.

For more details, refer to AD9510 datasheet.

	AD9510 Register 13 – 0x43							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Bypass 3	No Synch 3	Force 3	Start H/L 3	Phase Offset 3			
Default	'0'	'0'	'0'	'0'	'0000'			
0	Low Cycles 3				High Cycles 3			
Default	'0000'				'0000'			

3.4.41 AD9510 Register 14 – 0x44.

For more details, refer to AD9510 datasheet.

	AD9510 Register 14 – 0x44							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Bypass 4	No Synch 4	Force 4	Start H/L 4	Phase Offset 4			
Default	'0'	'0'	'0'	'0'	'0000'			
0	Low Cycles 4				High Cycles 4			
Default	'0000'				'0000'			

3.4.42 AD9510 Register 15 – 0x45.

For more details, refer to AD9510 datasheet.

	AD9510 Register 15 – 0x45							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Bypass 5	No Synch 5	Force 5	Start H/L 5	Phase Offset 5			
Default	'0'	'0'	'0'	'0'	'0000'			
0	Low Cycles 5				High Cycles 5			
Default	'0000'				'0000'			

3.4.43 AD9510 Register 16 – 0x46.

For more details, refer to AD9510 datasheet.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	AD9510 Register 16 – 0x46							
1	Bypass 6	No Synch 6	Force 6	Start H/L 6	Phase Offset 6			
Default	'0'	'0'	'0'	'0'	'0000'			
0	Low Cycles 6				High Cycles 6			
Default	'0000'				'0000'			

3.4.44 AD9510 Register 17 – 0x47.

For more details, refer to AD9510 datasheet.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	AD9510 Register 17 – 0x47							
1	Bypass 7	No Synch 7	Force 7	Start H/L 7	Phase Offset 7			
Default	'0'	'0'	'0'	'0'	'0000'			
0	Low Cycles 7				High Cycles 7			
Default	'0000'				'0000'			

3.4.45 AD9510 Register 18 – 0x48.

For more details, refer to AD9510 datasheet.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	AD9510 Register 18 – 0x48							
1	Not Used							
Default	'00000000'							
0	Not Used	Set Function pin		PD Synch	PD all Ref	Synch Software	Synch Select	Synch Enable
Default	'0'	'00'		'0'	'0'	'0'	'0'	'0'

3.4.46 AD9510 Register 19 – 0x49.

For more details, refer to AD9510 datasheet.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	AD9510 Register 19 – 0x49							
1	Not Used							Update Registers
Default	'0000000'							'0'
0	Not Used							
Default	'00000000'							

3.4.47 PCB and Firmware Version Registers

The PCB and Firmware Version registers can only be read by the Host. These registers indicate the PCB and Firmware versions of the *SMT384*.

4 PCB Layout

The following figures show the top and bottom view of the main module, the top view of the daughter-card and the module composition viewed from the side.

Figure 14 – Main Module Component Side.

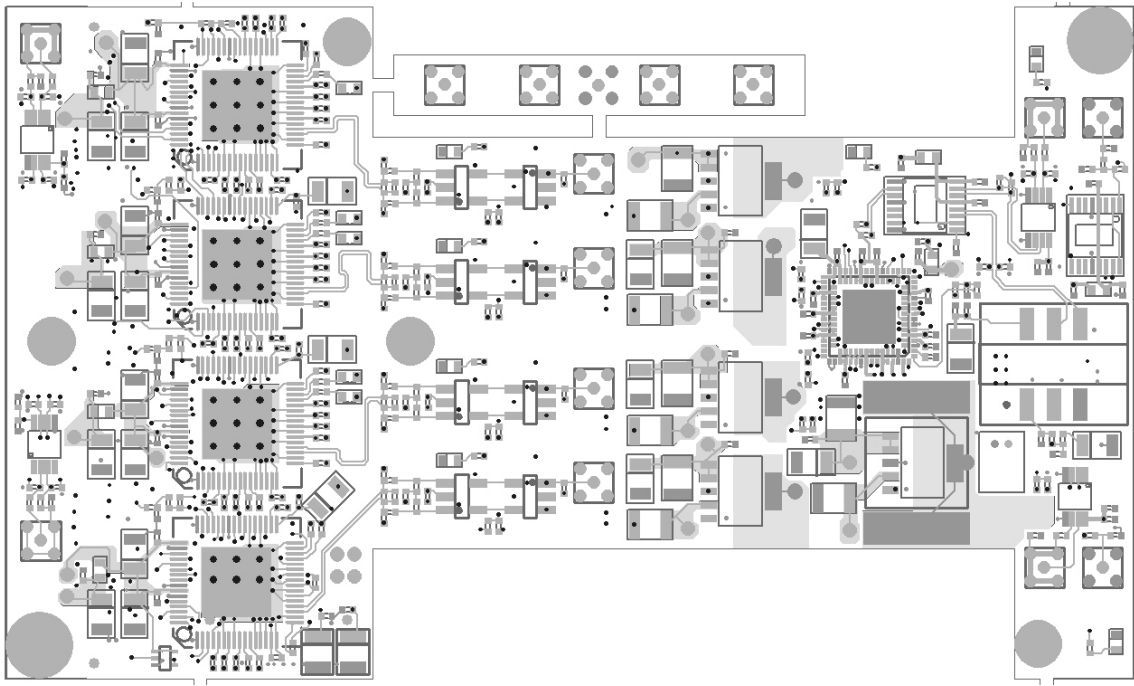**Figure 15 - Main Module (*SMT368*) Solder Side.**
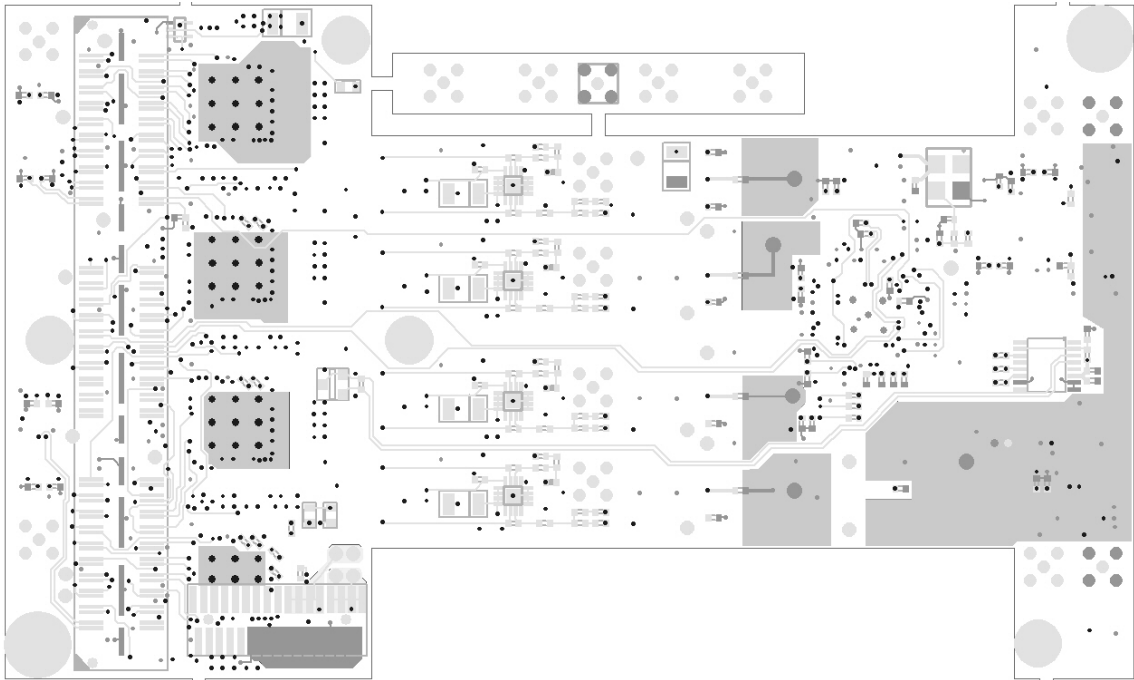
Figure 16 - Daughter Module Component Side.

Figure 17 - Daughter Module Solder Side.