Sundance Multiprocessor Technology Limited **Design Specification**	Form : QCF51 Dated : 20 June 2003 Revision : 6

Unit / Module Name:	Single Channel 10-bit ADC – 2 GSPS
Unit / Module Number:	SMT386
Used On:	SLB Base Modules
Document Issue:	1.2
Date:	07/06/2006

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Revision History

Issue	Changes Made	Date	Initials
1.0	First Release.	07/06/06	PSR
1.1	Block Diagram updated, power dissipation updated.	05/07/06	PSR
1.2	Clock circuitry detailed. Receiver LVDS to LVTTL added on data lines in order to use 1:4 DMUX	28/11/06	PSR

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1 Introduction

1.1 Overview

The SMT386 is single-width SLB Mezzanine Module able to sample a single analog input at 2 GSPS under a resolution of 10 bits. The converter is made by Atmel (AT84AS008B).

The Analog to Digital converter is coupled with a 1:4 Demultiplexer to reduce the speed of the data flow coming out of the ADC, also from Atmel (AT84CS001). LVDS lines are converted into LVTTL.

The Sampling clock is generated by an integrated PLL+VCO chip from Analog Devices (AD9516), able to generate a low-noise 2 GHz clock signal as well as a divided version. It can lock to on-board or an external reference source.

The SMT386 is designed to be paired with one of Sundance SLB Base Modules, such as SMT348.

All SLB Base Modules are FPGA-based, which can control Mezzanines (Clock, ADC settings, etc), process and route data flows.

1.2 Features

The main features of the SMT386 are listed below:

- Single ADC Channel,
- 2GHz maximum sampling frequency,
- 10 bits of data resolution,
- Clock circuitry, including on-board PLL/VCO and connector for external clock,
- SLB Connector (Digital),
- Hubert-Suhner MMCX Connectors (Analog),
- Interface for temperature monitoring.

1.3 Applications

Here is a non exhaustive list of applications that can be based on the SMT386:

- Broadband Direct RF down conversion,
- Wide band satellite receiver,
- High speed instrumentation and system acquisition,
- Radars.

1.4 Related Documents

AT84AS008B Datasheet – Atmel.

http://www.atmel.com/dyn/resources/prod_documents/doc5469.pdf

AT84CS001 Datasheet – Atmel.

http://www.atmel.com/dyn/products/product_card.asp?part_id=3565

AD9516 Datasheet – Analog Devices.

http://www.analog.com/en/prod/0%2C2877%2CAD9516%25252D0%2C00.html

Sundance **L**VDS **B**us (SLB) specifications – Sundance.

http://www.sundance.com/docs/SLB%20-%20Technical%20Specifications.pdf

TIM specifications.

ftp://ftp2.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf

MMCX Connectors – Hubert Suhner.

MMCX Connectors

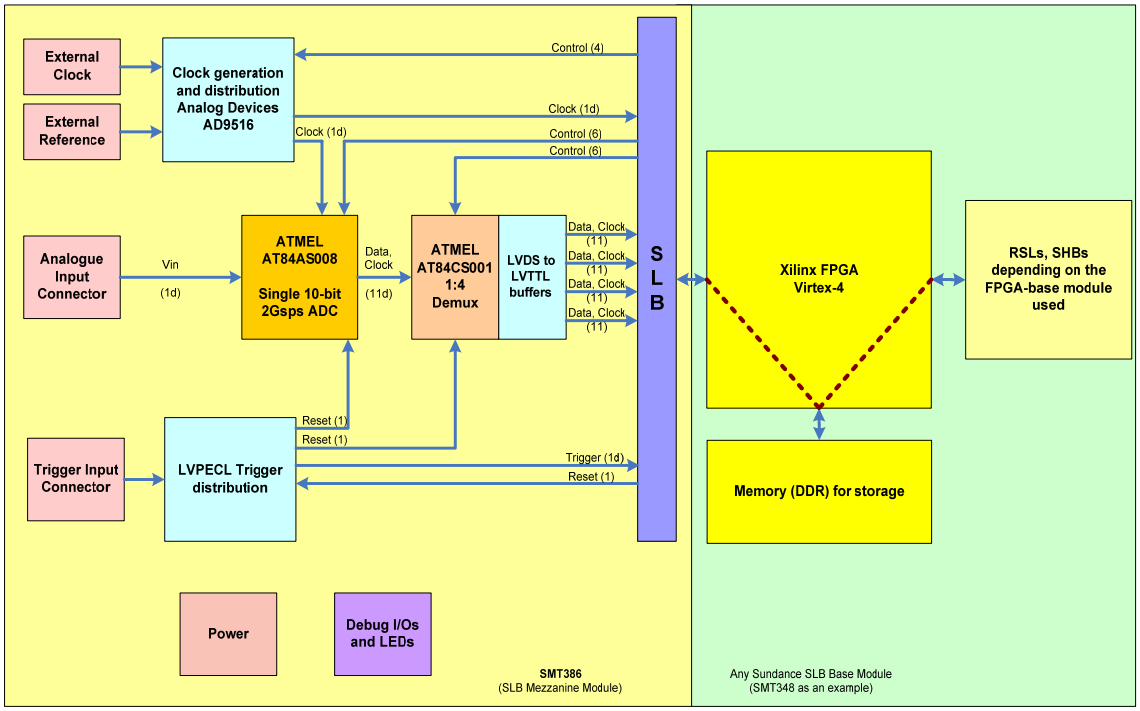
Sundance Multiprocessor Technology Ltd.

SMT348

2 Functional Description

2.1 Block Diagram

Below is shown the block diagram of the SMT386:



Notes: the numbers in brackets denote the amount of FPGA I/O pins required. 'd' stands for differential pairs. 1d thus requires 2 I/Os.

Figure 1 - SMT386 Block Diagram

The Analog signal is fed to the SMT386 via an MMCX connector. The signal is routed to the Atmel ADC converter. As well on MMCX connectors, are an external clock and an external trigger, both are differential signals, LVPECL format.

The data flow is divided into 4 separate flows by an Atmel Dmux part, which outputs are converted into LVTTL levels using a TI part (SN65LVDT386).

All digital functions to either control devices or process data are implemented in the FPGA located on the SLB base module.

2.2 Module Description

2.2.1 Clock Distribution

The clock circuitry is based around the Analogue Device AD9516, which is a PLL coupled with an integrated 2GHz-VCO. The output clock can be divided down via a programmable divider (entire number). It is all configurable by internal register via a Serial Interface. On the SMT386, it will be used in a fixed configuration in order to provide a quality clock signal. At 2GHz, the AD9516 can generate a differential clock signal with RMS jitter lower than 500 femto seconds. The VCO can be locked to an on-board crystal or an external reference. The user can also select an external clock.

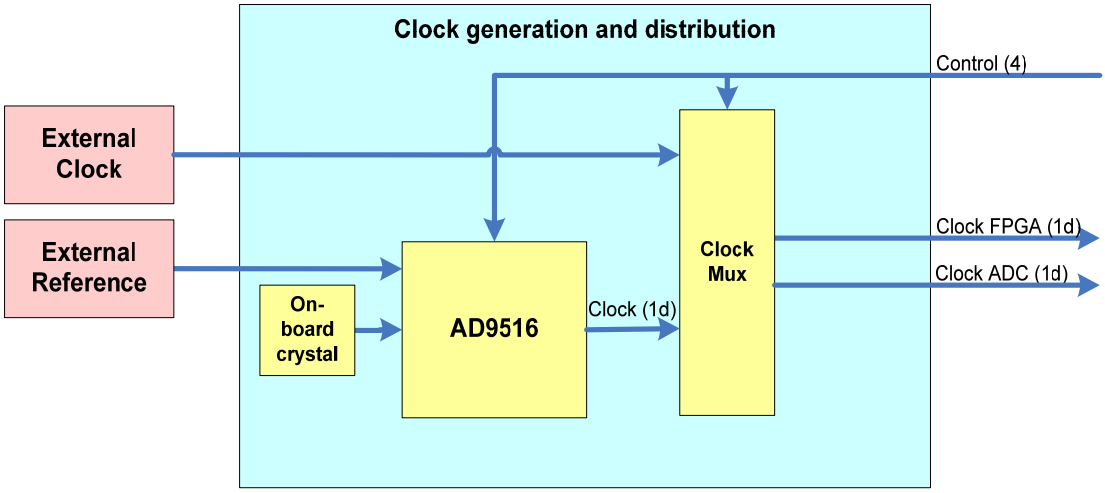


Figure 2 - Clock circuitry.

2.2.2 ADC

The ADC used on the SMT386 is an Atmel 10-bit part, the AT84AS008B, which has a maximum sampling rate of 2.2GSPS. The first version of SMT386 will feature a limited maximum rate to 2GSPS.

The AT84AS008B is given for a input bandwidth of 3.3GHz, a maximum SFDR of -58dBs, a maximum SNR of 52dBs and a maximum ENOB of 8 bits.

2.2.3 De-multiplexer

The De-multiplexer used on the SMT386 is an Atmel part too, the AT84SC001. It allows reducing the data flow rate by a factor of 4. Dual Data Rate is the format used to transfer data from the De-multiplexer to the FPGA on the SLB base module. Its LVDS output format is converted into LVTTL.

2.2.4 Trigger Distribution

The ADC and the De-multiplexer have to be reset simultaneously. The external trigger can be used to start a reset cycle or a command coming from the FPGA, before doing an data acquisition.

2.2.5 Miscellaneous

Some LEDs will be available on the board and driven by the FPGA (SLB base module) in order to provide visual information to the user.

2.2.6 Power requirements

Power supplies will all be coming from linear regulators on order to provide better performance.

AT84AS008B:

Vdvee: -2.2 Volts / 260mA max. Negative Linear Regulator (National LM2991) taken from a -3.3-Volt rail. The power dissipation is estimated at (3.3-2.2)x0.26 = **0.26 Watt**.

Vplusd: +2.5 Volts / 210mA max. Generated by a linear regulator (Texas Instrument - TPS79925) from 3.6-Volt Rail. The estimated power dissipation of the regulator is (3.6-2.5)x0.2 = **0.24 Watt**.

Vcc: +3.3 Volts / 820mA max. Generated by a linear regulator (Texas Instrument - TPS79633) from 3.6-Volt Rail. The estimated power dissipation of the regulator is (3.6-3.3)x0.82 = **0.25 Watt**.

The AT84AS008B is given for a total power dissipation close to 4 Watts.

The thermal resistance given by Atmel for that chip is 4.35ºC/W (Junction to Case). A heat sink is required to bring the case temperature down. A 27mm by 27mm heatsink (height 25mm) of thermal resistance 16.5ºC/W will give a maximum ambient operating temperature of Ta=Tj-4x(16.5+4.35)=41.6ºC. The thermal resistance of the chosen heatsink can drop down to 5.47ºC/W when the module is placed in a forced-air environement (1m/s equivalent to 200lfm), in which case the maximum ambient temperature can reach 85ºC.

The user should be aiming at keeping the junction temperature below 90ºC by either keeping the ambient temperature below 6.6ºC or imposing an air flow, in which case it could reach 50ºC .

AT84CS001:

Vccd: 3.3 Volts / 680mA. A Linear Regulator (Texas Instrument - TPS79633) will be used for this, connected to a 3.6-Volt power rail. The estimated power dissipation of the regulator is (3.6-3.3)x0.68 = **0.20Watt**.

Vplusd: 2.5 Volts / 360mA. A linear regulator (Texas Instrument - TPS79525) will be used again, from the 3.6-Volt power rail. The estimated power dissipation is (3.6-2.5)x0.36 = **0.4 Watt**.

The AT84CS001 is given for a total power dissipation close to 3.3 Watts.

The thermal resistance given by Atmel for that chip (25mm square) is 3.17ºC/W for Junction to Case. A heat sink is required to bring the case temperature down. A 27mm by 27mm heatsink (height 25mm) of thermal resistance 16.5ºC/W will give a maximum ambient operating temperature of Ta=Tj-3.3x(16.5+3.17)=60ºC. The thermal resistance of the chosen heatsink can drop down to 5.47ºC/W when the module is placed in a forced-air environement (1m/s equivalent to 200lfm), in which case the maximum ambient temperature can reach 96ºC.

The user should be aiming at keeping the junction temperature below 90ºC by either keeping the ambient temperature below 25ºC or imposing an air flow, in which case it could reach 61ºC.

AD9516-2:

Vcc : +3.3 Volts / ??mA max

SN65LVDT386:

Vcc : +3.3 Volts / 460mA max per chip. 3 are required to convert all LVDS data lines into LVTTL levels, so that's a total of 1380mA.

2.3 Interface Description

2.3.1 Mechanical Interface

2.3.2 Electrical Interface

3 Verification Procedures

4 Review Procedures

5 Validation Procedures

6 Timing Diagrams

7 Circuit Diagrams

8 PCB Layout Details

8.1 Component Side

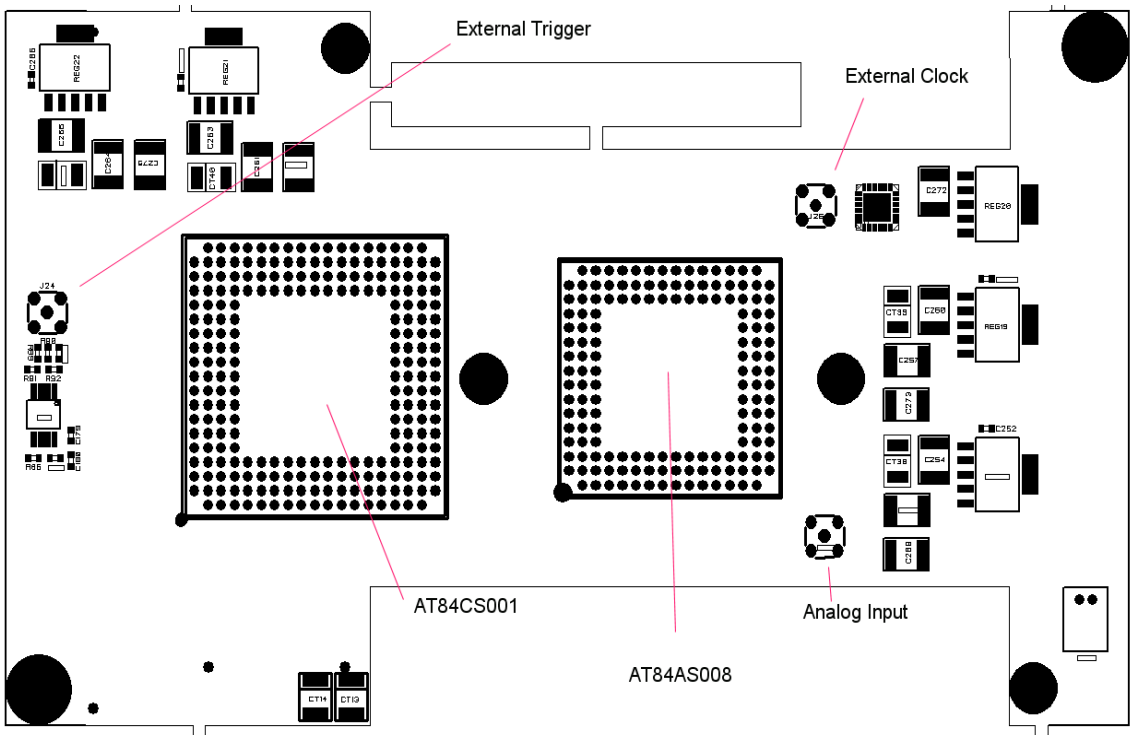


Figure 3 - Top Layout.

8.2 Solder Side

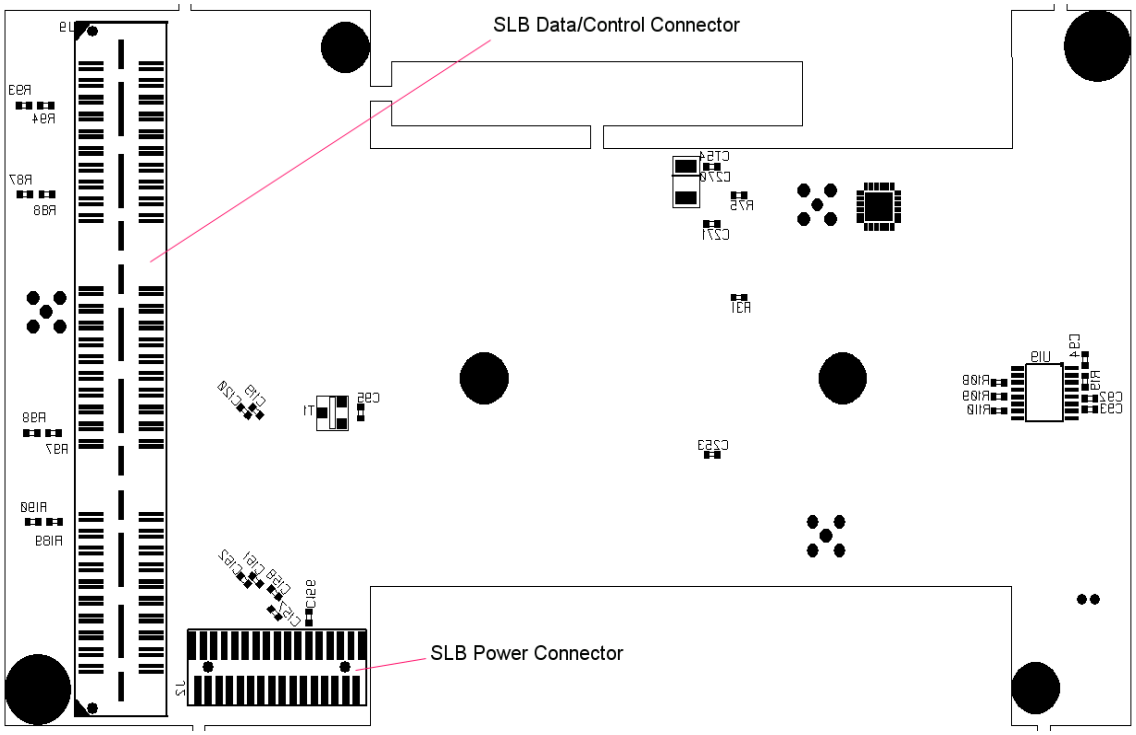


Figure 4 - Bottom Layout.

9 Pinout and Package Requirements

10 Safety

This module presents no hazard to the user.

11 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.