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Unit / Module Number:	SMT390
Used On:	SMT320, SMT310Q, SMT327, SMT300Q
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29/04/02	Main features gathered in a table	2.2	PSR
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31/10/03	Block diagram updated, dimension added, external clock changed	3.1	PSR
13/11/03	Clock Distribution, power connector and expansion connector updated.	3.2	PSR
18/11/03	Diagrams review. Power Generation and Distribution diagram updated. Connections to 4 LEDs added. Board options added. MMBX replaced by MMCX connectors.	3.3	PSR
19/11/03	ComPort numbers corrected. No longer 1 and 4, but 0 and 3. PCB Layout updated.	3.4	PSR

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1 Introduction

1.1 Overview

The *SMT390* is a single width TIM, which converts 2 analogue signals into two 12-bit resolution digital data flows. Analogue to digital conversion is performed by two Analog Devices AD9430s - they are 3.3-Volt 12-bit data CMOS devices that can sample at up to 210 MSPS.

Digital data is output to a Xilinx Virtex-II Pro FPGA (XC2VP20-6 or XC2VP30-6 - FF896, to be specified on order), which controls data transfers via ComPorts or the **S**undance **H**igh-speed **B**us (*SHB*). A copy of the data is also streamed over the **R**ocketIO **S**erial **L**inks on the module (*RSL*). These interfaces are compatible with a wide range of Sundance processor and I/O modules.

The FPGA is configured at power-up via Comport. The configuration process is controlled by a microprocessor MSP430.

Configuration, sampling and transferring modes are set via internal control registers.

1.2 Module features

The main features of the *SMT390* are listed below:

- Dual ADC board,
- On-board low-jitter clock generation,
- 210 Mega Samples Per Second,
- 12-bit resolution,
- Two external clocks and two external triggers via MMCX connector,
- 64 Mbytes (per channel) DDR SDRAM for sample capture,
- Two Standard Sundance ComPorts,
- Two SHB interfaces for easy interconnection to Sundance products,
- Two RSL (**R**ocketIO **S**erial **L**ink) interfaces for fast output transfers,
- All inputs are 50-Ohm terminated,
- On-board MSP430 microprocessor.

1.3 Possible applications

The *SMT390* can be used for the following application (this non-exhaustive list should be taken as an example):

- broadband cable modem head-end systems,
- 3G radio transceivers,
- High-data-rate point-to-point radios,
- Medical imaging systems,
- Spectrum analyzers.

1.4 Related Documents

AD9430 Datasheet - Analog Devices:

http://www.analog.com/productselection/descriptions/AD9430.html

Sundance **H**igh-speed **B**us (*SHB*) specifications – Sundance.

ftp://ftp2.sundance.com/Pub/documentation/pdf-files/SHB_Technical_Specification.pdf

TIM specifications.

ftp://ftp2.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf

Xilinx Virtex-II PRO FPGA.

http://direct.xilinx.com/bvdocs/publications/ds083.pdf

MMCX Connectors – Hubert Suhner.

MMCX Connectors

Surface Mount MMCX connector

2 Functional Description

In this part, we will see the general block diagram and some comments on each of its entities.

2.1 Block Diagram

The following picture shows the block diagram of the *SMT390*.

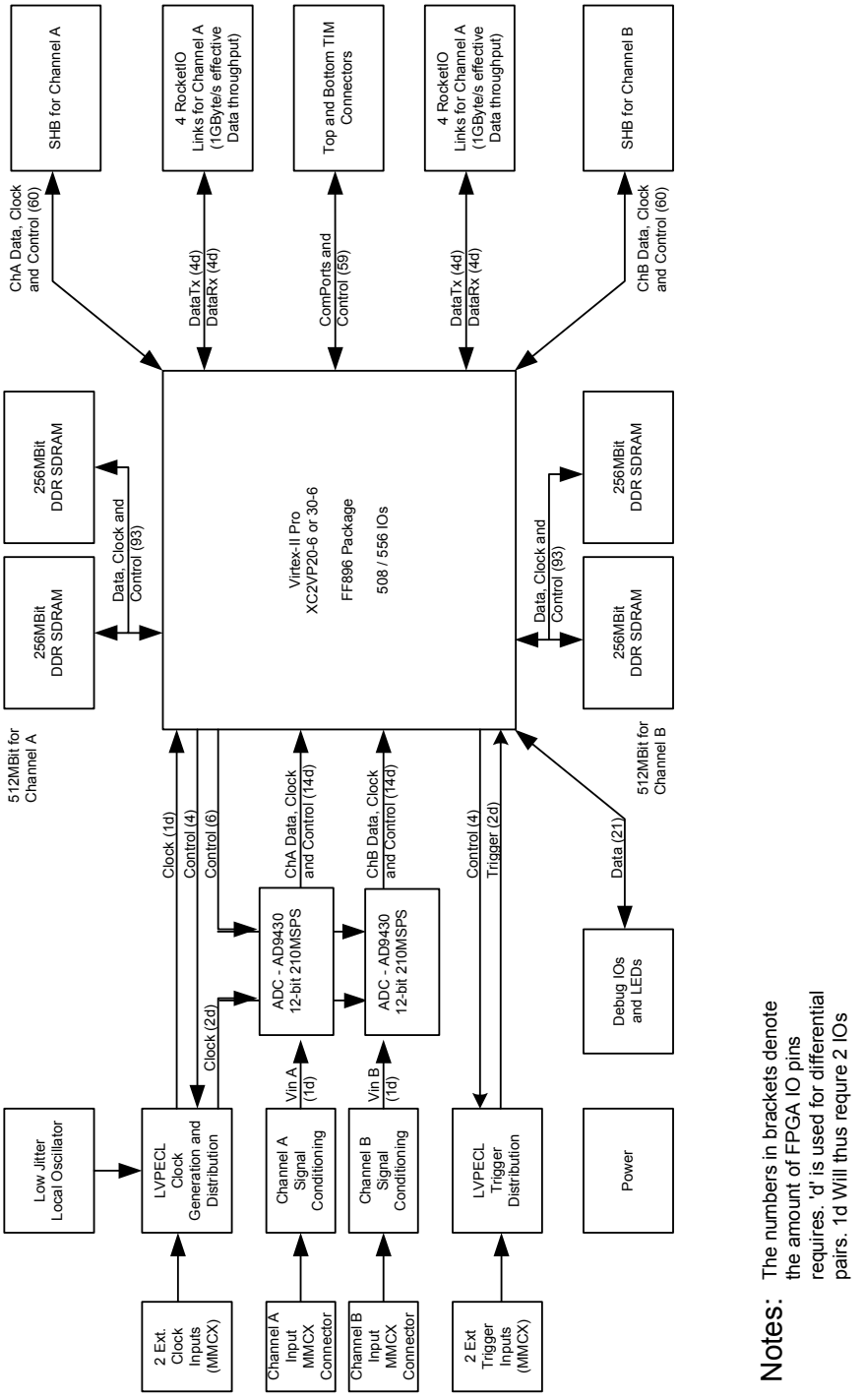


Figure 1 - General block diagram.

2.2 Module Description

The module is built around a Xilinx Virtex-II FPGA and two Analog Devices AD9430 12-bit monolithic sampling analog-to-digital converters.

Analog data enters the module via two MMCX connectors, one for each channel. Both signals are then conditioned (AC coupling) before being digitized. Both ADCs gets their own sampling clock, which can be either on-board generated or from an external source (MMCX connector). ADCs can receive either their own external clock or both the same external clock or both the same on-board clock. Two more MMCX connectors are dedicated for two external trigger signals. External clocks and triggers can be either single-ended or differential (the selection is made on hardware), whereas the analogue input is single-ended only.

ADCs digital outputs are fed into the FPGA. They can be passed directly on both SHB connectors or stored into the on-board DDR SDRAM memory to be transferred afterwards via SHB connectors. ADCs data stream can also be transmitted via RSL connectors.

The design of the *SMT390* is split over two PCBs. The main PCB (main module) contains the FPGA and the digital connector interfaces (TIM, SHB and RSL). The main memory of the *SMT390* is also located on this PCB. The second PCB (daughter card) contains all the analogue circuitry. The clock generation, trigger control, analogue signal conditioning and ADC are located on this PCB.

The FPGA gets control words from a ComPort following the Texas Instrument C4x standard, which can be either ComPort 0 or 3. It then feeds both ADCs with a differential encode signal, from one of the following sources: external (via MMCX connector) or internal (on-board clock generator). Two parallel LVDS buses carry 12-bit samples (2's complement or offset binary format) from both converters to the FPGA, which sends them out through both SHB connectors.

Two full (60-pin) *SHB* connectors are accessible from the FPGA. They are output only to send out digital samples to an other module. Please refer to the *SHB* specifications for more details about ways connectors can be configured.

A global reset signal is mapped to the FPGA from the bottom TIM connector.

2.3 Inputs and outputs main characteristics.

The main characteristics of the *SMT390* are gathered into the following table.

Analogue inputs	
Input voltage range	1.3 p-p – Full scale - AC coupled (scale changeable by half in via control register)
Impedance	50Ω - terminated to ground – single ended
Bandwidth	ADC bandwidth: 700 MHz. Input RF transformer: 800MHz.
External sampling clock inputs	
Format	Single ended or differential (3.3V PECL).
Frequency range	40-210 MHz
External Trigger inputs	
Format	Single ended or differential (3.3 V PECL).

Frequency range	105 MHz maximum
***SMT390* Output**	
Output Data Width	12-Bits
Data Format	2's Compliment or offset binary (Changeable via control register)
SFDR	Up to 80dB
SNR	Up to 65dB
Maximum Sampling Frequency	210 MHz

Figure 2 - Main features.

2.4 Data Stream Description

2.4.1 Block diagram

The data-path for both channels (ADCs) on the module and in the FPGA is identical. The ADCs are driven by its own clock either generated on the module or provided by the user through an MMCX connector. The following diagram shows the data-path inside the FPGA.

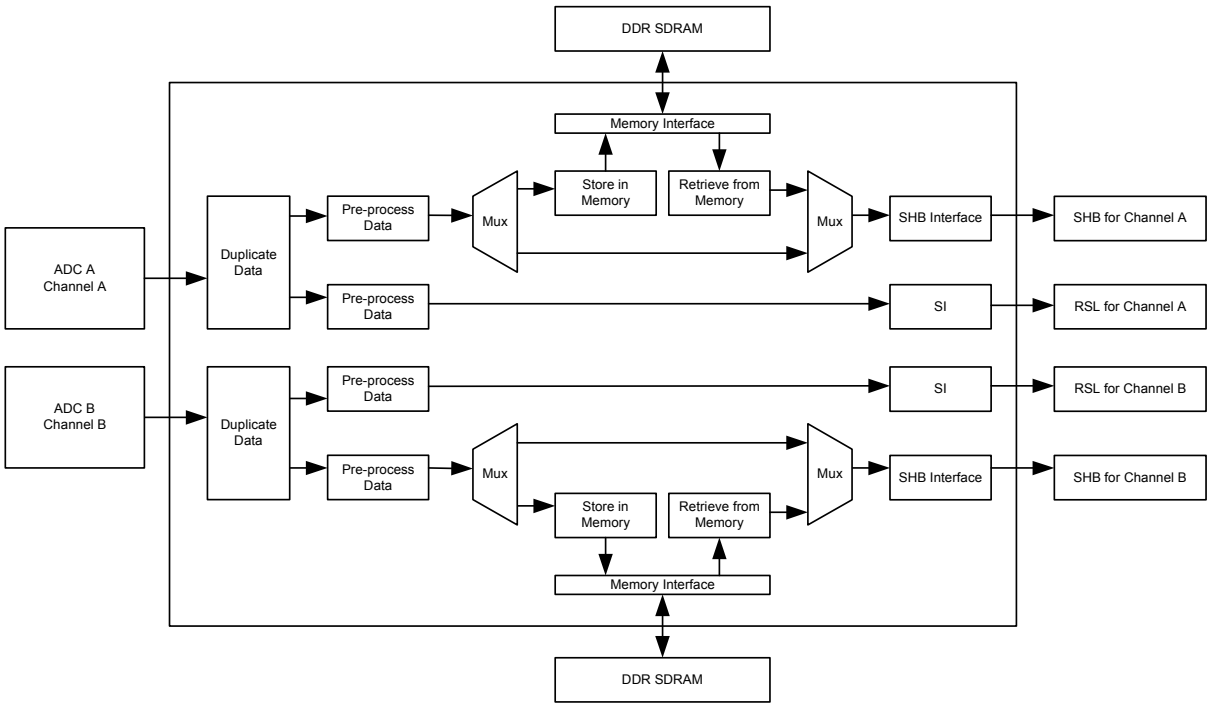


Figure 3 – Internal FPGA Architecture.

The analog data is converted by the ADC converters. A single 12-bit parallel LVDS data-stream is generated by each ADC (i.e. for each channel). This data-stream is duplicated in the FPGA. One stream is transmitted as is over the RSL interface for real-time type applications. The second data-stream can either be transmitted straight over the SHB interface (only if it is decimated by 4 or more) or stored in DDR SDRAM every time a trigger

is received. This data is kept in the memory until a non-real-time type module collects the data over the SHB interface.

2.4.2 Description of Internal FPGA Blocks

Duplicate Data

This block takes the incoming data stream and makes two copies of it. The first copy is used for real-time type applications where the full conversion data-stream is transmitted off the module. The second stream is either for non-real-time type applications where samples are captured and stored in memory or where a decimated data stream is continuously transferred over the SHB interface.

Pre-processing Data

The data pre-processing block performs basic operations on the data-stream. These operations include offset adjustment and decimation if required.

SI

The Serial Interface block takes the parallel input data stream and converts it into a high-speed serial data stream. This data stream is 16b encoded. On the receiving side the clock is recovered out of the serial data stream and the 16b data is decoded to 12b.

Mux

The multiplexer block decides whether a decimated data stream is continuously transmitted over the SHB interface, or whether the raw data stream is stored in memory every time a trigger is received.

Store in Memory

The store in memory block takes the incoming data stream and stores the data into DDR SDRAM. This block will only transfer data into the memory when a valid trigger command is received. The amount of data that must be stored is configurable.

Memory Interface

The memory interface block is the DDR SDRAM controller. This block is responsible to all write and read transactions to and from the DDR SDRAM. Each 12-bit sample is stored into a 16-bit memory location or two samples packed into a 32-bit word.

Retrieve from Memory

The retrieve from memory block retrieves stored data in the DDR SDRAM when it receives a valid read command. The read command specifies the location and amount of data that needs to be retrieved.

SHB Interface

The retrieved data from the 'Retrieve from Memory' block is transmitted over the SHB interface. The SHB interface controls the SHB bus between the *SMT390* and any module connected to the SHB requesting the data.

2.5 Clock Structure

There is an integrated clock generator on the module. The user can either use this clock or provide the module with an external clock (input via MMCX connector). The RSL interface will only function if the module's integrated clock is used.

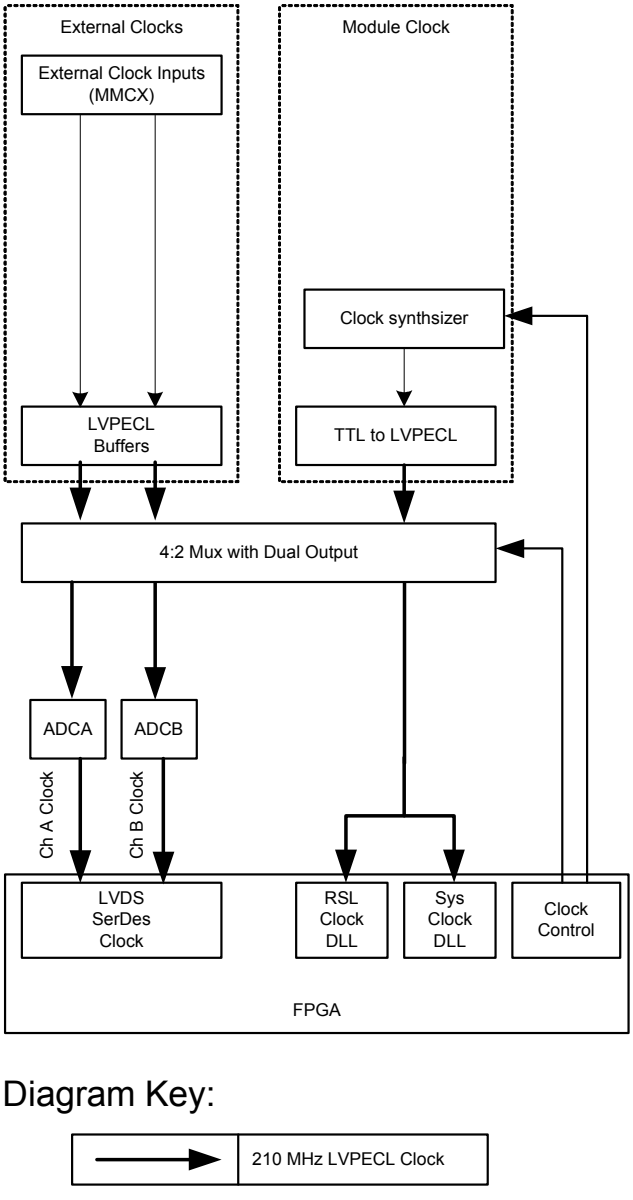


Figure 4 - Clock Structure.

Each ADC can receive as encode signals, the on-board clock or its own external clock or the other channel's clock. It also means that an external clock can encode both ADCs.

2.6 Power Supply and Reset Structure

The *SMT390* conforms to the TIM standard for single width modules. The TIM connectors supply the module with 5.0V. The module also requires an additional 3.3V power supply, which must be provided by the two diagonally opposite mounting holes. This 3.3V is present on all *Sundance* TIM carrier boards. From the 5.0V the FPGA Core Voltage (V_{CCINT} = 1.5V), the FPGA Auxiliary voltage (V_{CCAUX} = 2.5V) is generated. The FPGA IO Voltage (V_{CCO} = 3.3V) is taken straight from the TIM mounting holes. The 3.3V and the 5.0V present on the TIM connector is passed up to the daughter card. The daughter card is responsible for generating its required voltages.

A TI MSP430 low power microprocessor is located on the main module. This microprocessor controls the power sequencing for the main module. High efficiency Vishay DC/DC converters are used to generated the lower voltages.

On the daughter card the Analog Devices ADCs require analog and digital 3.3V. The 3.3V from the main module to daughter card power connector is used for the digital 3.3V. This voltage is filtered to provide the analog 3.3V.

The MSP430 microprocessor also controls the reset sequence for the *SMT390*. There are four possible reset sources for the *SMT390*:

1. A reset is received over the TIM connector
2. After power up an internal Power On Reset in the MSP430 causes a reset
3. Any of the voltages on the board falls outside of it's specified range
4. A reset command is received over either the RSL or the ComPorts interface

The MSP430 distributes the reset to the. The following two diagrams illustrate the power distribution and the reset distribution on the *SMT390*:

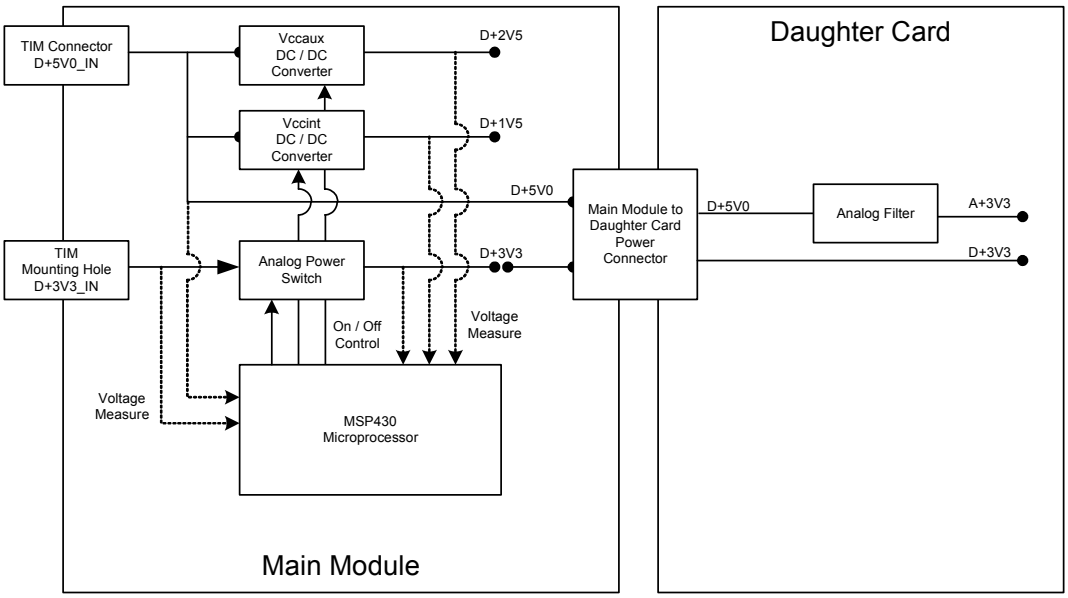


Figure 5 – Power Generation and Distribution.

2.7 MSP430 Functionality

The MSP430 implements analog control functionality that is difficult to implement in the FPGA. The microprocessor

- Controls the power start-up sequence
- Controls the reset structure on the module

2.8 Analog input section

Both analog inputs are AC-coupled (RF transformers).

2.9 ADC Settings

A sub-set of all the features of the AD9430 is implemented on the *SMT390*: S1 for the data format (two's complement or binary) and S5 for the scale.

3 Description of Interfaces

3.1 Memory Interface

Two groups of two 16-bit Samsung DDR SDRAMs form the volatile sample storage space of the module. Each DDR SDRAM is 256 MBits in size. This provides the module with a total of 64Mbytes (or 32 Mega samples) of storage space per channel - each 12-bit sample is stored into at 16-bit data location.

Each channel contains a 32-bit DDR266 controller. This interface is capable of data transfer at 2GBytes / s. It is thus fast enough to write the incoming ADC data stream into memory.

3.2 MSP430 Interface

A 3 Wire SPI interface is implemented between the FPGA and the microprocessor. The FPGA is the master and the microprocessor is the slave. The microprocessor contains a hardware SPI port. This interface is used for issuing a reset command to the microprocessor, and for the FPGA to read the analog test voltages back.

3.3 Serial Number

An SPI silicon serial number device is located on the model. This is used to assign a unique serial number to each module

3.4 Green LEDs.

There is a total of 7 LEDs on the Daughter Module. Three are dedicated for the power supplies (3.3Volt, 5V ADC Channel A and ADC Channel B). Four are driven by the FPGA directly.

3.5 ADC Data Interface

The output of each ADC is a 12-bit LVDS data bus with an LVDS clock. This clock and data bus is connected straight to high-speed LVDS transceivers on the Xilinx Virtex II Pro FPGA.

3.6 Clock synthesizer Interface

A three wire unidirectional control interface is implemented between the FPGA and the on-board clock synthesizer (SY89429V - Micrel).

3.7 TIM Interface

The *SMT390* implements ComPorts 0 and 3. There are no DIP switches on the module and all configuration data is received and transmitted over these two ports. The ComPorts are not used for ADC data transfer. ComPort 0 is implemented as a unidirectional receive interface and only receives data sent to the *SMT390*. ComPort 3 is implemented as a unidirectional transit interface and only transmits data from the *SMT390*.

3.8 RSL Interface

3.8.1 RSL Connector and Pinout Definition

The Rocket Serial Link (RSL) is a serial based communications interconnection standard that is capable of transfer speeds of up to 2.5GBit/s per link. Up to four links can be combined to form a Rocket Serial Link Communications Channel (RSLCC) that is capable of data transfer up to 10GBit/s.

Each RSL is made up of a differential Tx and Rx pair. A single RSL can thus transfer data at 2.5GBit/s in both directions at the same time. Rocket Serial Link interconnections are based on the RocketIO standard used on Xilinx Virtex-II Pro FPGAs. Rocket Serial Links uses Low Voltage Differential Signalling (LVDS).

The *SMT390* uses a subset of the RSL specification. Two RSLs are combined to form a 5GBit/s RSLCC. One RSLCC per ADC channel is implemented on the *SMT390*. The RSLCC is thus capable to transfer the raw data stream of the ADC in real time.

The connector used for the RSL interface is a 0.8mm pitch differential Samtec connector. The part number for this connector is: QSE-014-01-F-D-DP-A. The RSL connector takes the place of the optional 3rd and 4th SHB connector on a TIM module. The following diagram shows the position of the RSL connectors on the *SMT390*:

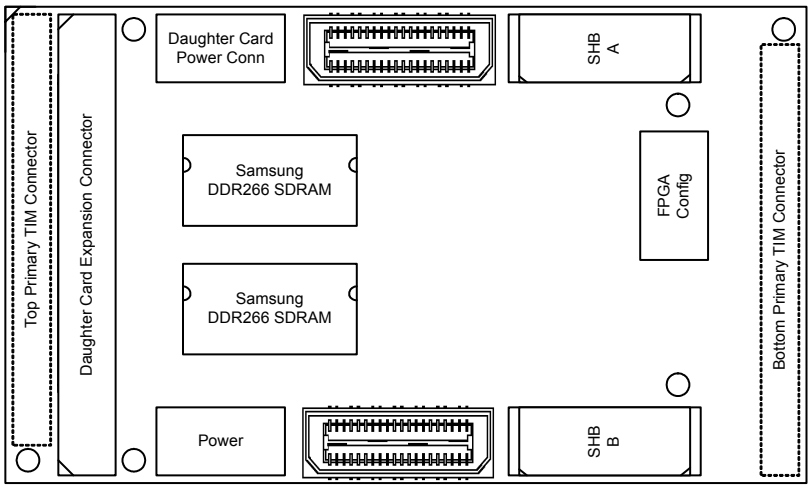
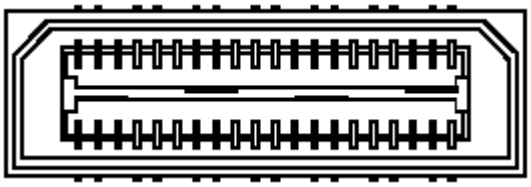


Figure 6 – Rocket Serial Link Interface.

2 4 6 8



1 3 5 7

RSL A

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Dir	Carrier / Other Module to *SMT390*		Dir	*SMT390* to Carrier / Other Module	
1	RxLink0p	Receive Link 0, positive	2	TxLink0p	Transmit Link 0, positive
3	RxLink0n	Receive Link 0, negative	4	TxLink0n	Transmit Link 0, negative
Dir	Carrier / Other Module to *SMT390*		Dir	*SMT390* to Carrier / Other Module	
5	RxLink1p	Receive Link 1, positive	6	TxLink1p	Transmit Link 1, positive
7	RxLink1n	Receive Link 1, negative	8	TxLink1n	Transmit Link 1, negative
Dir	Reserved		Dir	Reserved	
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
Dir	Reserved		Dir	Reserved	
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
Dir	Reserved		Dir	Reserved	
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
Dir	Reserved		Dir	Reserved	
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
Dir	Reserved		Dir	Reserved	
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

Figure 7 – Rocket Serial Link Interface Connector and Pinout (RSL A).

RSL B

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Dir	Carrier / Other Module to *SMT390*		Dir	*SMT390* to Carrier / Other Module	
1	RxLink0p	Receive Link 0, positive	2	TxLink0p	Transmit Link 0, positive
3	RxLink0n	Receive Link 0, negative	4	TxLink0n	Transmit Link 0, negative
Dir	Carrier / Other Module to *SMT390*		Dir	*SMT390* to Carrier / Other Module	
5	RxLink1p	Receive Link 1, positive	6	TxLink1p	Transmit Link 1, positive
7	RxLink1n	Receive Link 1, negative	8	TxLink1n	Transmit Link 1, negative
Dir	Reserved		Dir	Reserved	
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
Dir	Reserved		Dir	Reserved	
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
Dir	Reserved		Dir	Reserved	
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
Dir	Reserved		Dir	Reserved	
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
Dir	Reserved		Dir	Reserved	
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

Figure 8 – Rocket Serial Link Interface Connector and Pinout (RSL B).

3.8.2 RSL Cable Definition

The matching cable for the RSL connector is a Samtec High Speed Data Link Cable (Samtec HFEM Series). The cable may be ordered with different length and mating connector options. The following diagram shows such a typical cable:

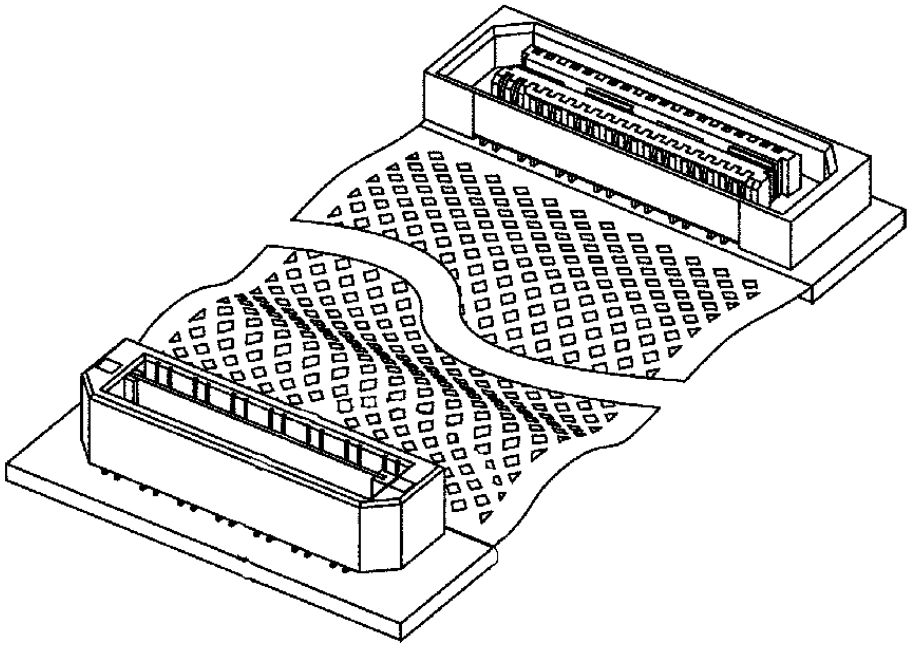


Figure 9 – Samtec HFEM Series Data Cable.

3.9 SHB Interface

The *SMT390* implements a subset of the full SHB implementation. Two configurations are possible

1. SHB A is configured to transmit 32-bit data words (24 bit effectively – 2 ADC samples) for channel A and SHB B is configured to transmit 32-bit data words (24 bit effectively – 2 ADC samples) for channel B. Both SHB interfaces are configured as outputs only. Control and configuration data is received over the ComPorts.
2. SHB A is configured to transmit two 16-bit half-words (effectively twice 12-bit words – 2 ADC samples). The first 16-bits is used for data from channel A and the second 16-bits is used for data from channel B. SHB B is configured in exactly the same way and transmit a copy of the data SHB A transmits.

The first configuration is ideal for higher speed data transfer. The second configuration can be used if (a) just one SHB is available on a module that the *SMT390* interfaces to, or (b) when the data stream must be passed on to two different end points. The two possible configurations are illustrated in the following figure:

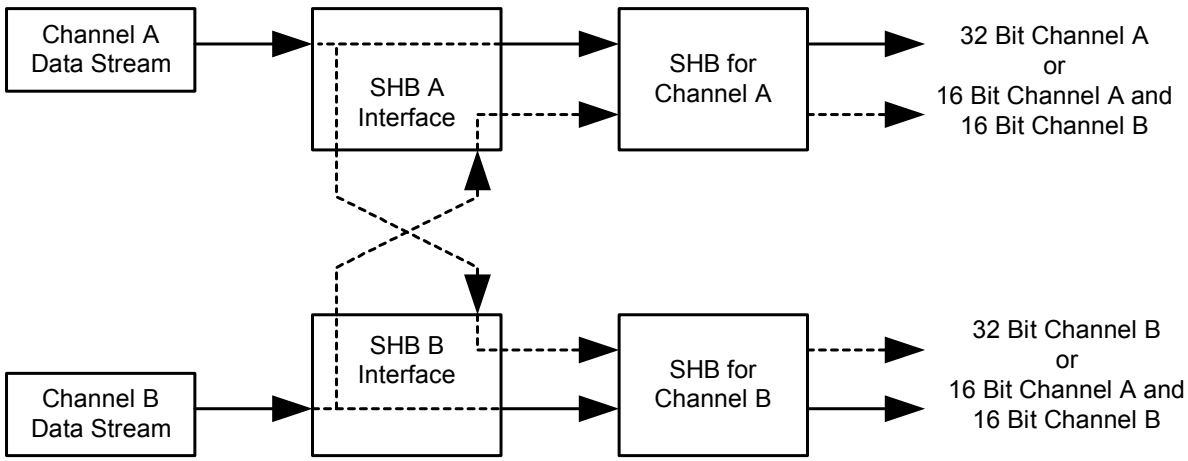


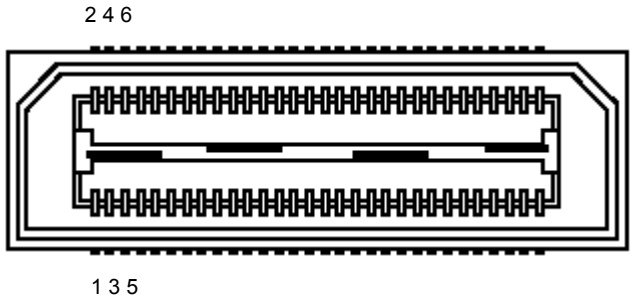
Figure 10 – Possible SHB Configurations.

The SHB interface will transmit data under the following two conditions:

- The SHB data path is set up to transmit decimated data continuously
- Sampled data in the memory is requested (over ComPort 0) and transmitted as a burst transfer over the SHB interface.

The SHB interface cannot be held. The receiving side must thus ensure that there is enough storage space before requesting a sample or that enough bandwidth is available to handle a continuous stream. The SHB clock frequency can be set as either ‘System Clock / 8’ or as ‘System Clock / 16’.

The connector used for the SHB interface is a 0.5mm Samtec QSH Type connector. The full part number for this connector is: QSH-030-01-L-D-A-K.



SHB A and SHB B

Pin No	Pin Name	Direction	Signal Description	Pin No	Pin Name	Direction	Signal Description
1	ChAClk	From 390	Ch A, ½Word Clock	31	Reserved	Reserved	Reserved
2	ChAD0	From 390	Ch A, ½Word Data 0	32	Reserved	Reserved	Reserved
3	ChAD1	From 390	Ch A, ½Word Data 1	33	Reserved	Reserved	Reserved
4	ChAD2	From 390	Ch A, ½Word Data 2	34	Reserved	Reserved	Reserved
5	ChAD3	From 390	Ch A, ½Word Data 3	35	Reserved	Reserved	Reserved
6	ChAD4	From 390	Ch A, ½Word Data 4	36	Reserved	Reserved	Reserved
7	ChAD5	From 390	Ch A, ½Word Data 5	37	ChBClk	From 390	Ch B, ½Word Clock
8	ChAD6	From 390	Ch A, ½Word Data 6	38	ChBD0	From 390	Ch B, ½Word Data 0
9	ChAD7	From 390	Ch A, ½Word Data 7	39	ChBD1	From 390	Ch B, ½Word Data 1
10	ChAD8	From 390	Ch A, ½Word Data 8	40	ChBD2	From 390	Ch B, ½Word Data 2
11	ChAD9	From 390	Ch A, ½Word Data 9	41	ChBD3	From 390	Ch B, ½Word Data 3
12	ChAD10	From 390	Ch A, ½Word Data 10	42	ChBD4	From 390	Ch B, ½Word Data 4
13	ChAD11	From 390	Ch A, ½Word Data 11	43	ChBD5	From 390	Ch B, ½Word Data 5
14	ChAD12	Reserved	Not Implemented	44	ChBD6	From 390	Ch B, ½Word Data 6
15	ChAD13	Reserved	Not Implemented	45	ChBD7	From 390	Ch B, ½Word Data 7
16	ChAD14	Reserved	Not Implemented	46	ChBD8	From 390	Ch B, ½Word Data 8
17	ChAD15	Reserved	Not Implemented	47	ChBD9	From 390	Ch B, ½Word Data 9
18	ChAUser0	Reserved	Not Implemented	48	ChBD10	From 390	Ch B, ½Word Data 10
19	ChAUser1	Reserved	Not Implemented	49	ChBD11	From 390	Ch B, ½Word Data 11
20	ChAUser2	Reserved	Not Implemented	50	ChBD12	Reserved	Not Implemented
21	ChAUser3	Reserved	Not Implemented	51	ChBD13	Reserved	Not Implemented
22	ChAWen	From 390	Ch A, Write Enable	52	ChBD14	Reserved	Not Implemented
23	ChAReq	Reserved	Not Implemented	53	ChBD15	Reserved	Not Implemented
24	ChAAck	Reserved	Not Implemented	54	ChBUser0	Reserved	Not Implemented
25	Reserved	Reserved	Reserved	55	ChBUser1	Reserved	Not Implemented
26	Reserved	Reserved	Reserved	56	ChBUser2	Reserved	Not Implemented
27	Reserved	Reserved	Reserved	57	ChBUser3	Reserved	Not Implemented
28	Reserved	Reserved	Reserved	58	ChBWen	From 390	Ch B, Write Enable
29	Reserved	Reserved	Reserved	59	ChBReq	Reserved	Not Implemented
30	Reserved	Reserved	Reserved	60	ChBAck	Reserved	Not Implemented

Figure 11 –SHB Connector Configuration 2 Pinout.

3.10 Daughter-card Interface

The daughter-card interface is made up of two connectors. The first one is a 0.5mm-pitch differential Samtec connector. This connector is for transferring the ADC LVDS output data to the FPGA on the main module. The second one is a 1mm-pitch Samtec header type connector. This connector is for providing power to the daughter-card.

The figure underneath illustrates this configuration. The bottom view of the daughter card is shown on the right. This view must the mirrored to understand how it connects to the main module.

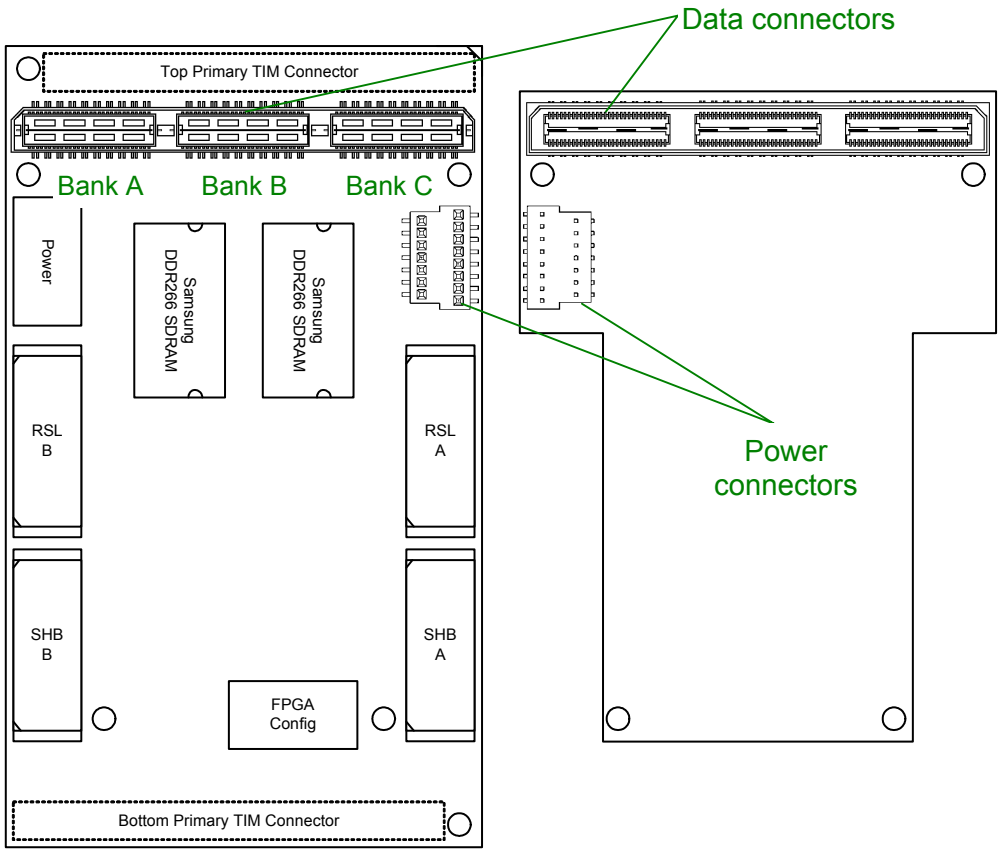


Figure 12 – Daughter Card Connector Interface.

The female differential connector is located on the main module. The Samtec Part Number for this connector is QTH-060-01-F-D-DP-A.

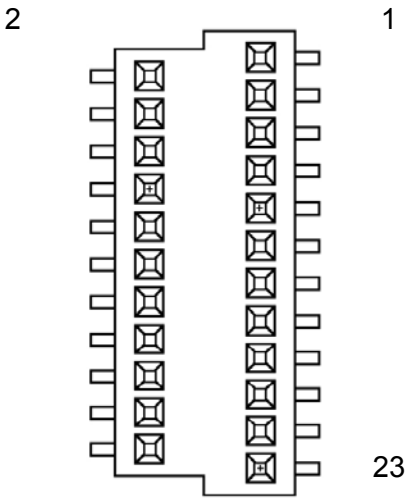
The female power connector is located on the main module. The Samtec Part Number for this connector is BKS-133-03-F-V-A

The male differential connector is located on the daughter card. The Samtec Part Number for this connector is QSH-060-01-F-D-DP-A

The male power connector is located on the daughter card. The Samtec Part Number for this connector is BKT-133-03-F-V-A

The mated height between the main module and the daughter card is 5 mm.

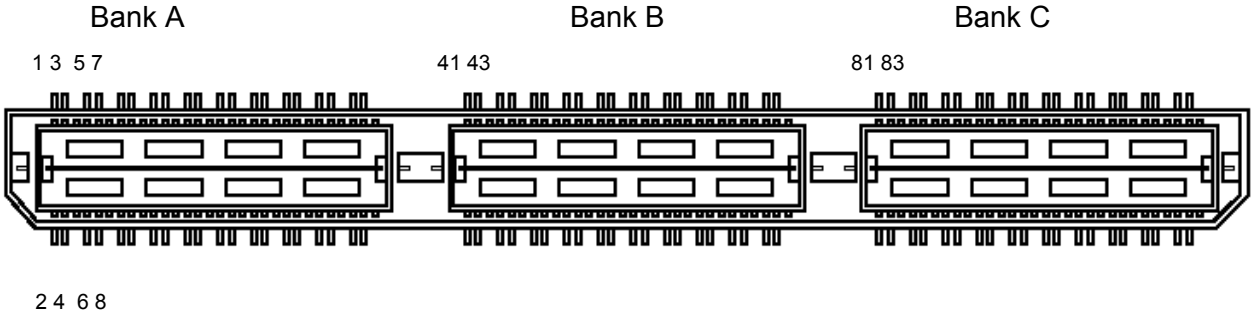
Each pin on the power connector (23 pins in total) can carry 1.5 A. Digital 5V (D+5V0), digital 3V3 (D+3V3) and digital ground (DGND) is provided over this connector. D+3V3 and D+5V0 are assigned four pins each. The daughter card can thus draw a total of 6A of each of these two supplies. The integral ground plane on the differential connector provides additional grounding. The following table shows the pin assignment on the power connector:



Pin Number	Pin Name	Description of Signal
1	D+3V3	Digital 3.3 Volts
2	DGND	Digital Ground
3	D+3V3	Digital 3.3 Volts
4	DGND	Digital Ground
5	D+3V3	Digital 3.3 Volts
6	DGND	Digital Ground
7	D+3V3	Digital 3.3 Volts
8	DGND	Digital Ground
9	D+5V0	Digital 5.0 Volts
10	DGND	Digital Ground
11	D+5V0	Digital 5.0 Volts
12	DGND	Digital Ground
13	D+5V0	Digital 5.0 Volts
14	DGND	Digital Ground
15	D+5V0	Digital 5.0 Volts
16	DGND	Digital Ground
17	D+12V0	Digital +12.0 Volts
18	DGND	Digital Ground
19	D+12V0	Digital +12.0 Volts
20	DGND	Digital Ground
21	D-12V0	Digital –12.0 Volts
22	DGND	Digital Ground
23	D-12V0	Digital –12.0 Volts

Figure 13 – Daughter Card Interface Power Connector and Pinout.

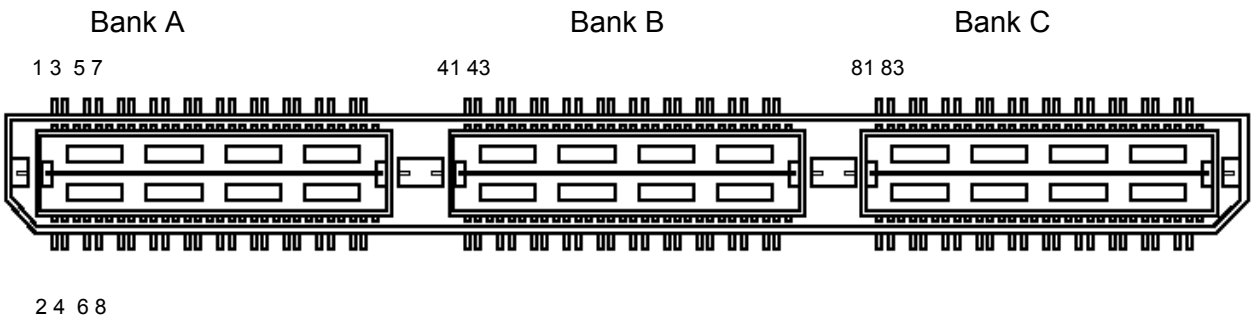
The following few pages describes the signals on the data connector between the main module and the daughter card. Bank A on the connector is used for the ADC I Channel data bus. Bank C is used for the ADC Q channel data bus. Bank B is used for system clock and trigger signals, ADC control signals and general system control signals. The general system control signals include: daughter card sense signal, daughter card ID signals, DC/DC control signals and daughter card reset signal. All reserved signals are connected to the FPGA on the main module for future expansion.



Bank A

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
1	DOAI0p	Data Out 0, Channel A (pos).	2	DOBI0p	Data Out 8, Channel A (pos).
3	DOAI0n	Data Out 0, Channel A (neg).	4	DOBI0n	Data Out 8, Channel A (neg).
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
5	DOAI1p	Data Out 1, Channel A (pos).	6	DOBI1p	Data Out 9, Channel A (pos).
7	DOAI1n	Data Out 1, Channel A (neg).	8	DOBI1n	Data Out 9, Channel A (neg).
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
9	DOAI2p	Data Out 2, Channel A (pos).	10	DOBI2p	Data Out 10, Channel A (pos).
11	DOAI2n	Data Out 2, Channel A (neg).	12	DOBI2n	Data Out 10, Channel A (neg).
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
13	DOAI3p	Data Out 3, Channel A (pos).	14	DOBI3p	Data Out 11, Channel A (pos).
15	DOAI3n	Data Out 3, Channel A (neg).	16	DOBI3n	Data Out 11, Channel A (neg).
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
17	DOAI4p	Data Out 4, Channel A (pos).	18	DOBI4p	Reserved.
19	DOAI4n	Data Out 4, Channel A (neg).	20	DOBI4n	Reserved.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
21	DOAI5p	Data Out 5, Channel A (pos).	22	DOBI5p	Reserved.
23	DOAI5n	Data Out 5, Channel A (neg).	24	DOBI5n	Reserved.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
25	DOAI6p	Data Out 6, Channel A (pos).	26	DOBI6p	Reserved.
27	DOAI6n	Data Out 6, Channel A (neg).	28	DOBI6n	Reserved.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
29	DOAI7p	Data Out 7, Channel A (pos).	30	DOBI7p	Reserved.
31	DOAI7n	Data Out 7, Channel A (neg).	32	DOBI7n	Reserved.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
33	ClkOIp	Output Ready, Channel A (pos).	34	DOIRIp	Out of Range, Channel A (pos).
35	ClkOIn	Output Ready, Channel A (neg).	36	DOIRIn	Out of Range, Channel A (neg).
Dir	Reserved.		Dir	Reserved.	
37	Reserved	Reserved.	38	Reserved	Reserved.
39	Reserved	Reserved.	40	Reserved	Reserved.

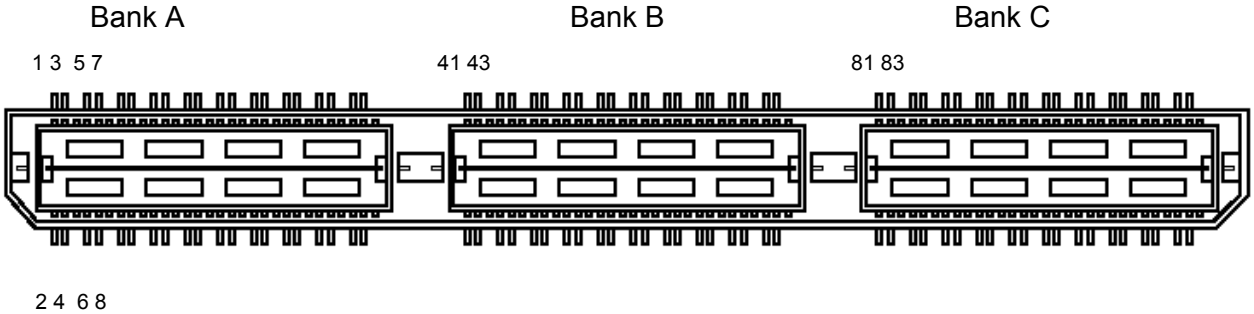
Figure 14 – Daughter Card Interface: Data Signals Connector and Pinout (Bank A).



Bank B

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Type	**Clock and Trigger System Signals**		**Type**	**Clock and Trigger System Signals**	
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
41	SMBClk	Temperature Sensor Clock.	42	SMBData	Temperature Sensor Data.
43	SMBnAlert	Temperature Sensor Alert.	44	SerialNo	Serial Number Data Line.
Dir	Daughter Card to Main Module		Dir	Reserved	
45	AdcVDacI	Reserved	46	AdcVDacQ	Reserved
47	AdcVRes	Reserved	48	AdcReset	Reserved
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
49	D3v3Enable	3.3V Power Enable	50	D2v5Enable	5V Power Enable
51	AdcMode	Data Format (2's/bin), ChA.	52	AdcClock	Half or Full Scale, ChA.
Type	**ADC Specific Signals**		**Type**	**ADC Specific Signals**	
Dir	Main Module to Daughter Card		Dir	Reserved	
53	AdcLoad	Data Format (2's/bin), ChB.	54	AdcData	Half or Full Scale, ChB.
55	AdcCal	Reserved.	56	AdjClkCntr0	Adj. Clock Serial Clock.
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
57	AdjClkCntr1	Adj. Clock Serial Data.	58	AdjClkCntr2	Adj. Clock Serial Load.
59	AdjClkCntr3	Adj. Clock Serial Test.	60	PllCntr0	Led1
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
61	PllCntr1	Led2	62	PllCntr2	Led3
63	PllCntr3	Led4	64	AdcAClkSel	Clock Selection, ChA
Type	**Module Control Signals**		**Type**	**Module Control Signals**	
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
65	AdcBClkSel	Clock Selection, ChB	66	IntClkDivEn	AdcAClkOpp
67	IntClkDivnReset	Reserved.	68	IntExtClkDivEn	AdcBClkOpp
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
69	IntExtClkDivnReset	Reserved.	70	FpgaVRef	JTAG FPGA Vref.
71	FpgaTck	JTAG FPGA tck.	72	FpgaTms	JTAG FPGA tms.
Dir	Daughter Card to Main Module		Dir	Reserved	
73	FpgaTdi	JTAG FPGA tdi.	74	FpgaTdo	JTAG FPGA tdo.
75	MspVRef	JTAG MSP430 Vref	76	MspTck	JTAG MSP430 tck.
Dir	Daughter Card to Main Module		Dir	Reserved	
77	MspTms	JTAG MSP430 tms.	78	MspTdi	JTAG MSP430 tdi.
79	Msptdo	JTAG MSP430 tdo.	80	MspnTrst	JTAG MSP430 reset

Figure 15 – Daughter Card Interface: Data Signals Connector and Pinout (Bank B).



Bank C

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
81	DOAQ0p	Data Out 0, Channel B (pos).	82	DOBQ0p	Data Out 8, Channel B (pos).
83	DOAQ0n	Data Out 0, Channel B (neg).	84	DOBQ0n	Data Out 8, Channel B (neg).
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
85	DOAQ1p	Data Out 1, Channel B (pos).	86	DOBQ1p	Data Out 9, Channel B (pos).
87	DOAQ1n	Data Out 1, Channel B (neg).	88	DOBQ1n	Data Out 9, Channel B (neg).
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
89	DOAQ2p	Data Out 2, Channel B (pos).	90	DOBQ2p	Data Out 10, Channel B (pos).
91	DOAQ2n	Data Out 2, Channel B (neg).	92	DOBQ2n	Data Out 10, Channel B (neg).
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
93	DOAQ3p	Data Out 3, Channel B (pos).	94	DOBQ3p	Data Out 11, Channel B (pos).
95	DOAQ3n	Data Out 3, Channel B (neg).	96	DOBQ3n	Data Out 11, Channel B (neg).
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
97	DOAQ4p	Data Out 4, Channel B (pos).	98	DOBQ4p	Reserved.
99	DOAQ4n	Data Out 4, Channel B (neg).	100	DOBQ4n	Reserved.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
101	DOAQ5p	Data Out 5, Channel B (pos).	102	DOBQ5p	Reserved.
103	DOAQ5n	Data Out 5, Channel B (neg).	104	DOBQ5n	Reserved.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
105	DOAQ6p	Data Out 6, Channel B (pos).	106	DOBQ6p	Reserved.
107	DOAQ6n	Data Out 6, Channel B (neg).	108	DOBQ6n	Reserved.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
109	DOAQ7p	Data Out 7, Channel B (pos).	110	DOBQ7p	Reserved.
111	DOAQ7n	Data Out 7, Channel B (neg).	112	DOBQ7n	Reserved.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
113	ClkOQp	Output Ready, Channel B (pos).	114	DOIRQp	Out of Range, Channel B (pos).
115	ClkOQn	Output Ready, Channel B (neg).	116	DOIRQn	Out of Range, Channel B (neg).
Dir	Reserved.		Dir	Reserved.	
117	Reserved.	Reserved.	118	Reserved.	Reserved.
119	Reserved.	Reserved.	120	Reserved.	Reserved.

Figure 16 – Daughter Card Interface: Data Signals Connector and Pinout (Bank C).

4 Control Register Settings

The Control Registers control the complete functionality of the *SMT390*. They are setup via the ComPort or RSL link. The settings of the ADC, triggers, clocks, the configuration of the SHB and RSL interfaces and the internal FPGA data path settings can be configured via the Control Registers.

4.1 Control Packet Structure

The data passed on to the *SMT390* over the ComPorts must conform to a certain packet structure. Only valid packets will be accepted and only after acceptance of a packet will the appropriate settings be implemented. Each packet will start with a certain sequence indicating the start of the packet (0xFF). The address to write the data payload into will follow next. After the address the data will follow. The packet is ended off with a CRC of the packet (currently not implemented). This structure is illustrated in the following figure:

	Byte Content							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'
1	Address 7	Address 6	Address 5	Address 4	Address 3	Address 2	Address 1	Address 0
3	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
4	Optional CRC – Not Implemented							

Figure 17 – Setup Packet Structure.

4.2 Reading and Writing Registers

Control packets are sent to the *SMT390* over ComPort 0. This is a unidirectional interface and data can only be sent to the *SMT390* over ComPort 0. ComPort 3 is used to read control information back from the *SMT390*. ComPort 3 is thus also a unidirectional interface going from the *SMT390* to the system host. Data is read by issuing a 'Read Request' control packet containing the address to be read over ComPort 0. The *SMT390* will collect the required data and send a 'Read Packet' out over ComPort 3 containing the requested data. The format of a 'Read Packet' is the same as that of a write packet.

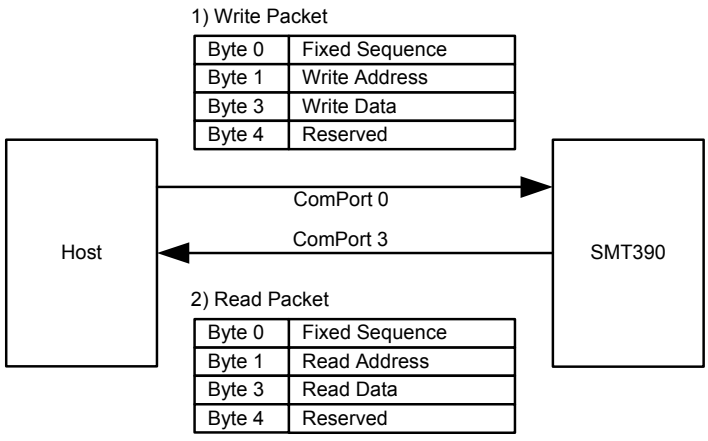


Figure 18 – Control Register Read Sequence.

4.3 Memory Map

The write packets must contain the address where the data must be written to and the read packets must contain the address where the required data must be read. The following figure shows the memory map for the writable and readable Control Registers on the *SMT390*:

Address	Writable Registers	Readable Registers
0x00	Reset Register	Reserved
0x01	Read Register	Reserved
0x03	Clock Control Register	Read-back Clock Control Register
0x04	VCO Voltage Register	Read-back VCO Voltage Register
0x05	Trigger Source Register	Read-back Trigger Source Register
0x06	Trigger Block Size Register	Read-back Trigger Block Size Register
0x07	ADC Setup Register	Read-back ADC Setup Register
0x08	FPGA Data Routing Register	Read-back FPGA Data Routing Register
0x09	SHB Clock Register	Read-back SHB Clock Register
0x0A	Pre-processing Control Register	Read-back Pre-processing Control Register
0x0B	Reserved	Measured Voltage 0
0x0C	Reserved	Measured Voltage 1
0x0D	Reserved	Measured Voltage 2
0x0E	Reserved	Measured Voltage 3
0x0F	Reserved	Measured Voltage 4
0x10	Reserved	Measured Voltage 5
0x11	Reserved	Reserved
0x12	Reserved	Main Module Temperature
0x13	Reserved	Module Serial Number 0 (LSB)
0x14	Reserved	Module Serial Number 1
0x15	Reserved	Module Serial Number 2
0x16	Reserved	Module Serial Number 3
0x17	Reserved	Module Serial Number 4
0x18	Reserved	Module Serial Number 5 (MSB)
0x19	Reserved	PCB Version
0x1A	Reserved	Firmware Version

Figure 19 – Register Memory Map.

4.4 Register Descriptions

4.4.1 The Reset Register

Writing any value into the reset register will reset the *SMT390*.

4.4.2 The Read Register

Writing a value (address) into the Read Register will result in a read at the address written into the read register. The read data will be sent over ComPort 3 in a 'Read Packet' format

4.4.3 The Clock Control Register

The Clock Control Register sets the clock source and clock routing options. The following figure shows the different control bits in the Clock control register:

	Clock Control Register							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved						Clock Source	
Default	'000000'						'00'	

	Clock Source		
Setting	**Bit 1**	**Bit 0**	**Description**
0	0	0	Onboard VCO uses for System, RSL and ADC Clocks
1	0	1	External Clocked used for System and ADC Clocks. RSL Interface disabled
2	1	0	Local Main Board Oscillator used for System and RSL Clock. ADC Disabled (used if daughter card is not present – determined by sense line on the daughter card interface)
3	1	1	Reserved for future use

Figure 20 – Clock Control Register.

4.4.4 Trigger Source Control Register

The Trigger Source Control Register sets the trigger source and trigger routing options. The following figure shows the different control bits in the Trigger control register:

	Clock Control Register							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	SHB Capture Setup		SHB Decimate Setup		RSL Trigger Setup		Trigger Source	
Default	'00'		'00'		'00'		'00'	

Setting	**Bit 1**	**Bit 0**	**Description**
	Trigger Source		
0	0	0	External Trigger
1	0	1	ComPort Command
2	1	0	RSL Command
3	1	1	Reserved for future use
	RSL Trigger Setup		
0	0	0	Start / Stop transmitting when the next trigger is received
1	0	1	Transmit the pre-set amount of samples when a trigger is received
2	1	0	Ignore Triggers and transmit data continuously
3	1	1	Reserved for future use
	SHB Decimate Setup		
0	0	0	External Trigger

1	0	1	Transmit the pre-set amount of samples when a trigger is received
2	1	0	Ignore Triggers and transmit data continuously
3	1	1	Reserved for future use
	SHB Capture Setup		
0	0	0	Capture the pre-set amount of samples when a trigger is received
1	0	1	Reserved for future use
2	1	0	Reserved for future use
3	1	1	Reserved for future use

Figure 21 – Trigger Source Control Register.

4.4.5 Trigger Block Size Control Register

The Trigger Block Size sets the amount of sample blocks to capture and store in DDR SDRAM when a trigger is received. The default block size is 1 Mega Byte of samples (1048576 8-Bit samples). The amount of these blocks that must be stored per trigger can be set between 1 and 32

	Trigger Block Size Control Register							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved			Trigger Block Size				
Default	'000'			'00001'				

	Trigger Block Size	
Setting	**Bit 4 down to Bit 0**	**Block Size**
0	'00000'	1 Mega Byte
1	'00010'	2 Mega Bytes
31	'11111'	32 Mega bytes

Figure 22 – Trigger Block Size Control Register.

4.4.6 ADC Setup Control Register

The ADC Setup Control Register sets the configuration settings of the ADC that is configurable by the user. Refer to section 2.9 for more information on these settings.

	ADC Setup Register							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved				Analog Selection		Decimate Mode	StandBy Mode
Default	'0000'				'00'		'0'	'0'

Setting	**Bit 1**	**Bit 0**	**Description**
	Standby Mode		

0	NA	0	ADC Active
1	NA	1	ADC in standby mode
	Decimation Mode		
0	NA	0	ADC Decimation disabled
1	NA	1	ADC Decimation by 16 enabled
	Analog Selection		
0	0	0	Analog Selection Mode A
1	0	1	Analog Selection Mode B
2	1	0	Analog Selection Mode C
3	1	1	Reserved for future use

Figure 23 – ADC Setup Control Register.

4.4.7 FPGA Data Routing Control Register

The FPGA Data Routing Control Register sets the internal configurable FPGA data paths. On the SHB data path the data can either be decimated and routed straight to the SHB interface or it can be routed to the memory control interface and stored in memory

	FPGA Data Routing Control Register							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved							DataPath
Default	'0000000'							'0'

	FPGA Data Path		
Setting	**Bit 1**	**Bit 0**	**Description**
0	NA	0	Data is decimated and routed straight to the SHB interface
	NA	1	Data is stored in the onboard memory

Figure 24 – Clock Control Register.

4.4.8 SHB Clock Control Register

The SHB Clock Control Register sets the SHB clock transmit frequency.

	SHB Clock Control Register							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved							SHBClock
Default	'0000000'							'0'

	SHB Clock		
Setting	**Bit 1**	**Bit 0**	**Description**
0	NA	0	SHB clock is System Clock / 8
	NA	1	SHB clock is System Clock / 16

Figure 25 – SHB Clock Control Register.

4.4.9 Pre-processing Control Register

The Pre-processing Control Register sets whether or not decimation is implemented on the separate data paths, and if it is what the decimation factor is

	Pre-processing Control Register							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	ShbPath				RslPath			
Default	'0100'				'0000'			

Setting	Bit 3	Bit 2	Bit 1	Bit 0	Description
	RSL Path				
0	0	0	0	0	No Decimation
1	0	0	0	1	Decimate By 2
2	0	0	1	0	Decimate By 4
3	0	0	1	1	Decimate By 8
	0	1	0	0	Decimate By 16
	x	x	x	x	Reserved for future use
	SHB Path				
0	0	0	0	0	No Decimation
1	0	0	0	1	Decimate By 2
2	0	0	1	0	Decimate By 4
3	0	0	1	1	Decimate By 8
	0	1	0	0	Decimate By 16
	x	x	x	x	Reserved for future use

Figure 26 – Pre-processing Control Register.

4.4.10 Measured Voltage Registers

The Measured Voltage register can only be read by the Host. The data is represented as a two digit BCD number.

	Measured Voltage Registers	
Address	**Register Name**	**Register Content**
0x0B	Measured Voltage 0	Main TIM 3.3V
0x0C	Measured Voltage 1	Main TIM 5.0V
0x0D	Measured Voltage 2	Generated 1.5V for FPGA Vccint
0x0E	Measured Voltage 3	Generated 2.5V for FPGA Vccaux
0x0F	Measured Voltage 4	Generated 2.25V for ADC Vccio
0x10	Measured Voltage 5	Reserved for future use

Figure 27 – Measured Voltage Registers.

4.4.11 Main Module Temperature Register

The Main Module Temperature register can only be read by the Host. The data is a 255 bit representation of the module temperature measured at the MSP430. This data must be calibrated to be meaningful.

4.4.12 Module Serial Number Registers

The Module Serial Number registers can only be read by the Host. Six registers form a unique 64 bit silicon serial number.

4.4.13 PCB and Firmware Version Registers

The PCB and Firmware Version registers can only be read by the Host. These registers indicate the PCB and Firmware versions of the SMT390.

5 PCB Layout

The following figures show the top and bottom view of the main module, the top view of the daughter-card and the module composition viewed from the side.

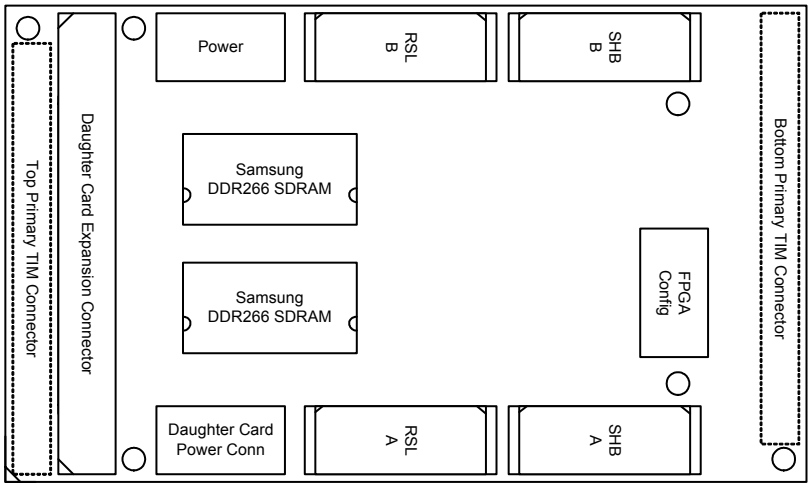


Figure 28 – Module Top View (Main Module).

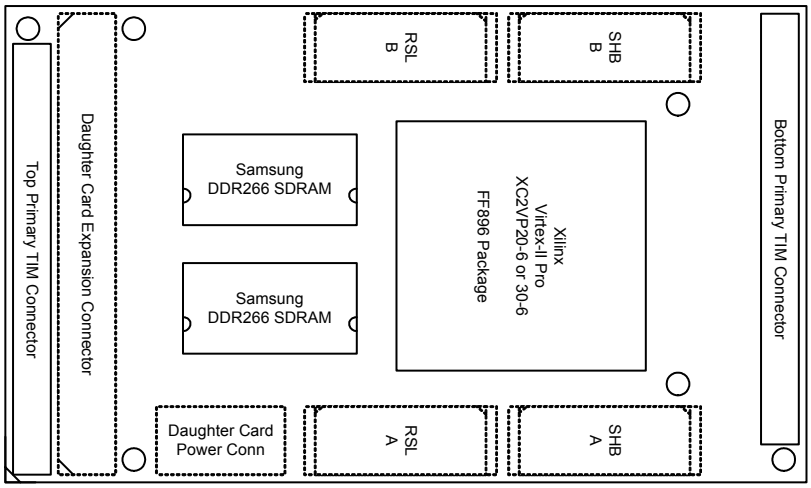


Figure 29 – Module Bottom View (Main Module).

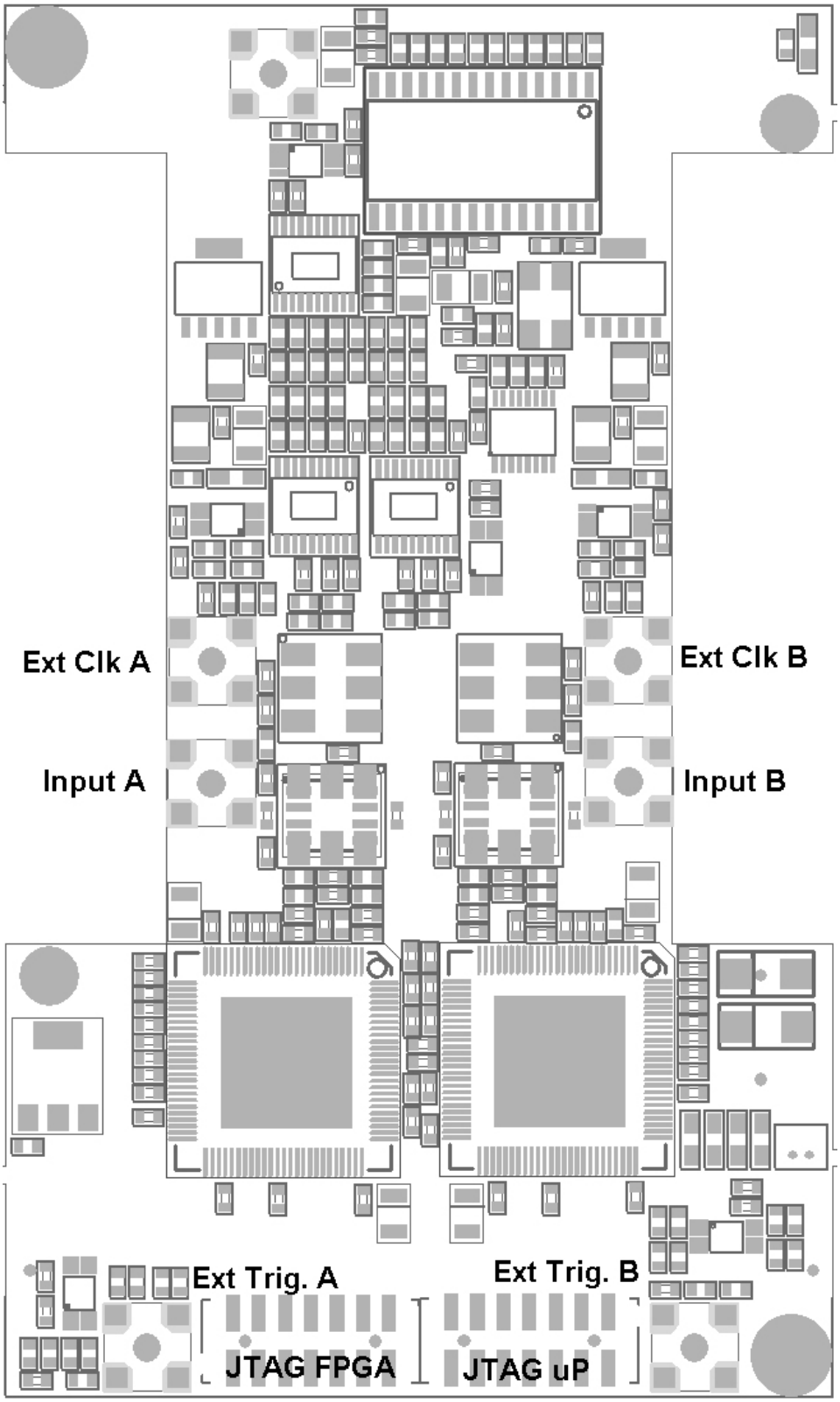
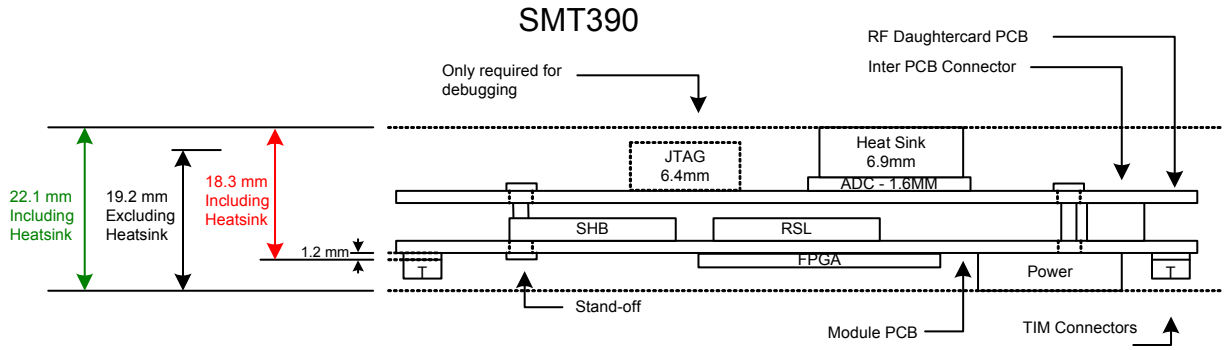


Figure 30 – Top View (Daughter-card).

If the *SMT390* is mated with a PCI carrier two PCI slots will be required for the Module + Carrier combination. If the *SMT390* is mated with a cPCI carrier the Module + Carrier will require two cPCI slots.



In red, extra height when mated on a 310Q
In green, height of the module itself

Figure 31 – Side view of module.

6 Appendix.

The default *SMT390* is supplied with the following options:

- Single-ended External Triggers via MMCX connectors,
- Single-ended External Clocks via MMCX connectors,
- AC-coupled ADC inputs,
- FPGA: Virtex II-Pro VP7-5.

Available option:

- Differential External Triggers via MMCX connectors,
- Differential External Clocks via MMCX connectors,
- MMBX instead of MMCX connectors,
- AC-coupled inputs for low input frequencies (below 30MHz),
- Second input RF transformer on each channel for high input frequencies (above 100MHz),
- FPGA: Virtex II-Pro VP20-5,
- FPGA: Virtex II-Pro VP30-5,
- FPGA: Virtex II-Pro VP30-6.