| | |
|---|---|
| **Unit / Module Name:** | Dual channel 8-bit ADC – 1 GSPS |
| **Unit / Module Number:** | SMT391-VP |
| **Used On:** | SMT338-VP, SMT320, SMT310Q, SMT327, SMT300Q |
| **Document Issue:** | 1.3 |
| **Date:** | 03/09/2004 |

# CONFIDENTIAL

| Approvals | | Date |
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# Revision History

| | Changes Made | Issue | Initials |
|---|---|---|---|
| 24/04/03 | First release | 1.0 | MRV |
| 10/05/03 | Updated data path description, added control register descriptions, general expansion and clarification | 1.1 | MRV |
| 25/05/03 | Updated architecture and specifications after detailed hardware design. | 1.2 | MRV |
| 03/09/04 | Added and modified information on final implementation of design. | 1.3 | MRV |

# List of Abbreviations

| Abbreviation | Explanation |
|---|---|
| ADC | Analog to Digital Converter |
| ATP | Acceptance Test Procedure |
| BCD | Binary Coded Decimal |
| BER | Bit Error Rate |
| BOM | Bill Of Materials |
| CDR | Clock and Data Recovery |
| CPCI | Compact PCI |
| DDR | Double Data Rate |
| DLL | Delay Lock Loop |
| DSP | Digital Signal Processor |
| FPGA | Field Programmable Gate Array |
| GSPS | Giga Sample Per Second |
| LSB | Least Significant Bit |
| LVDS | Low Voltage Differential Signalling |
| LVPECL | Low Voltage Positive ECL |
| MSB | Most Significant Bit |
| NA | Not Applicable |
| PC | Personal Computer |
| PCB | Printed Circuit Board |
| PCI | Peripheral Component Interconnect |
| POR | Power On Reset |
| RSL | Rocket Serial Link |
| RSLCC | Rocket Serial Link Communications Channel |
| SDRAM | Synchronous Dynamic Random Access Memory |
| SHB | Sundance High-speed Bus |
| SI | Serial Interface |
| SMT | Sundance Multiprocessor Technology |
| SPI | Serial Peripheral Interface |
| TBD | To Be Determined |
| TI | Texas Instruments |
| VCO | Voltage Controlled Oscillator |

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## Precautions (Please Read this!).

In order to guarantee that the *SMT391-VP* functions correctly and to protect the module from damage, the following precautions should be taken:

The *SMT391-VP* is a static sensitive product and should be handled accordingly. Always place the module in a static protective bag during storage and transition.

When operated, make sure that the heat generated by the system is extracted e.g. by the use of a fan extractor or an air blower.

SHB and RSL connectors are similar but their use is really different. Do NOT connect an SHB and an RSL connectors together with and SHB cable! This would cause irreversible damages to the modules.

## Naming Conventions.

The SMT391 refers to a dual channel, 8-bit, 1GSPS ADC daughter card.

The SMT338-VP refers to a single width Virtex-II Pro based FPGA module with a Sundance LVDS Bus interface (used for connecting TIM modules to daughter cards)

The SMT391-VP refers to the SMT391 plugged onto the SMT338-VP forming a complete module ADC + FPGA Module.

# 1. Introduction

## 1.1 Overview

The *SMT391-VP* is a single width TIM module. It is capable of sampling two analog inputs at 1 GSPS with a resolution of 8 bits. An Atmel dual channel ADC (AT84AD001) performs the analogue to digital conversion.

Digital data is output to a Xilinx Virtex-II Pro FPGA (XC2VP30-6 - FF896 package), which is controlled via a ComPort link. Data samples from the ADC are first stored in the on-board memory and then transferred onto the **S**undance **H**igh-speed **B**us (*SHB*). This interface is compatible with a wide range of Sundance processor and I/O modules.

A copy of the data will also be streamed over the **R**ocketIO **S**erial **L**inks on the module (*RSL*) in a future version.

The FPGA is configured at power-up over ComPort 3. The configuration process is controlled by a microprocessor (a Texas Instruments MSP430 family microprocessor). Once the FPGA is configured the configuration ComPort is used for setting up control registers in the FPGA to control the functions of the FPGA.

## 1.2 Module Features

The main features of the *SMT391-VP* are listed underneath:

- Dual channel ADC (Ideal for I & Q channel applications)
- 1GHz sampling frequency
- 8 Bit data resolution
- 64 Mbytes (per channel) DDR SDRAM for sample captures
- Custom Clock and Trigger inputs via external connectors
- Two Standard Sundance ComPorts
- Two SHB interfaces for easy interconnection to Sundance products (interfaces for data sample and non-real-time processing)
- RSL interface for data streaming applications
- On-board MSP430 microprocessor

## 1.3 Possible Applications

The SMT391-VP can be used for the following applications (this non-exhaustive list should be taken as an example):

- Broadband cable modem head-end systems
- 3G Radio transceivers
- High-data-rate point-to-point radios
- Medical imaging systems

- Spectrum analyzers

## 1.4 Related Documents

**[1]** **S**undance **H**igh-speed **B**us (*SHB*) specifications – Sundance.
ftp://ftp2.sundance.com/Pub/documentation/pdf-files/SHB_Technical_Specification_v1_0.pdf

**[2]** **R**ocketIO **S**erial **L**inks (*RSL*) specifications – Sundance.
ftp://ftp2.sundance.com/Pub/documentation/pdf-files/RSL_Technical_Specification_v1_0.pdf

**[3]** **TIM** specifications.
ftp://ftp2.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf

**[4]** **S**undance **L**VDS **B**us (*SLB*) specifications – Sundance.
http://www.sundance.com/docs/SLB%20-%20Technical%20Specifications.pdf

**[5]** Virtex-II Pro FPGA datasheet - Xilinx.
http://direct.xilinx.com/bvdocs/publications/ds083.pdf

**[6]** Dual 8-bit ADC datasheet - Atmel.
http://www.atmel.com/dyn/resources/prod_documents/doc2153.pdf

**[7]** ComPort specification – Texas Instruments.
http://focus.ti.com/lit/ug/spru63c.pdf

# 2 Functional Description

## 2.1 Module Overview

The following diagram shows the block diagram of the *SMT391-VP*.

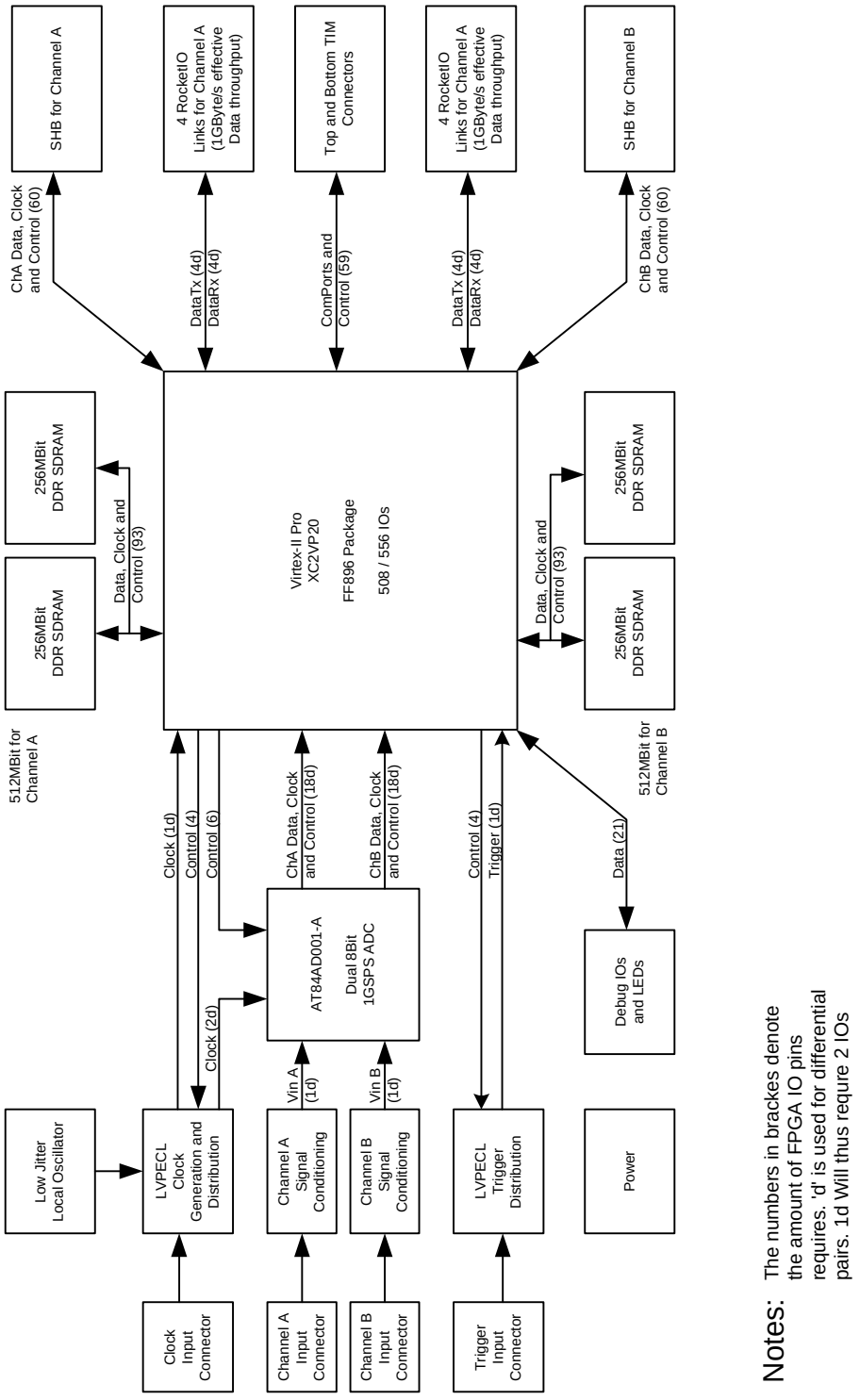



**Figure 1 - Block diagram of the SMT391.**

Analog data enters the module via two MMBX connectors – one for each channel. These two analog data streams are pre-conditioned before it enters the Atmel dual channel ADC converter. In conjunction to the two analog inputs the user can also provide the module with a custom clock and trigger. These two inputs must be LVPECL type signals.

All digital functions on the module are controlled by the Xilinx FPGA. The digital output of the ADC converter is fed into the FPGA. This data is then stored in onboard DDR SDRAM for non real-time processing. The data in the memory is transferred to other modules via the SHB interface. The ADC data stream may also be transmitted over the RSL interface (RSL is not available with the current firmware, but will become available in future firmware versions).

The SMT391 is designed for high-speed I and Q channel type applications. For this reason the two channels are identical and all settings are applicable to both. Operation for both channels are identical and can not be separated. There is only one sample clock for both channels and both channels will respond to the same trigger.

The design of the SMT391 is split over two PCBs. The main PCB (main module – SMT338-VP) contains the FPGA and the digital connector interfaces (TIM, SHB and RSL). The main memory as well as the MSP430 microprocessor is also located on this PCB. The second PCB (daughter card – SMT391) contains all the analog circuitry. The clock generation, trigger control, analog signal conditioning and ADC is located on this PCB. The SMT391-VP refers to the combination of the SMT338-VP and the SMT391.

The depth of the SMT391-VP is 21 mm. If the SMT391-VP is mated with a PCI carrier two PCI slots will be required for the Module + Carrier combination. If the SMT391-VP is mated with a cPCI carrier the Module + Carrier will require two cPCI slots.

The FPGA gets control words over a ComPort interface following the Texas Instruments C4x standard. The ADCs sample data and send the data to the FPGA over two 8-bit LVDS busses per channel (16 bits de-muxed data at half the sample rate) according to the SLB standard. From here the data is stored in the memory when a trigger is received. The data is then sent out over the SHB connectors.

Two full (60-pin) SHB connectors are accessible from the FPGA. Their main function is to send out digital samples to other modules. Please refer to the SHB specification for more details about the way connectors can be configured.

A global reset signal is mapped to the FPGA from the bottom TIM connector via the MSP430 microcontroller.

## 2.2 Communication Ports (ComPorts)

The SMT391-VP provides two ComPorts – ComPort 0 and ComPort 3. Both of these ComPorts are connected to the FPGA on the SMT338-VP. ComPort 3 is also connected to the MSP430 microprocessor. The microprocessor is the master of this ComPort after reset and configures the FPGA with configuration data received over

this link. After configuration the microprocessor releases the ComPort to the FPGA. These ComPorts are driven at 3.3V levels.

## 2.3 Sundance High-Speed Bus (SHB)

Two SHB connectors are used to transmit data coming from the SMT391-VP to the external world. Both SHB busses are identical and 60-bits wide. See the SHB specification for more information.

## 2.4 Main Analog characteristics.

The main analog characteristics of the *SMT391* are listed in the following table:

| | |
|---|---|
| **Analogue inputs** | |
| Input voltage range | 0.5Vp-p |
| Impedance | 50Ω - terminated to ground |
| Analogue Bandwidth | ADC Bandwidth: 1500MHz<br>RF Transformer: 500kHz to 1.5GHz (AC Coupled)<br>RF Transformer: 500kHz to 1.0GHz (DC Coupled) |
| **External sampling clock inputs** | |
| Signal format | LVPECL |
| Frequency range | Up to 1000 MHz |
| **External trigger inputs** | |
| Signal format | LVPECL |
| Frequency range | Up to 250 MHz |
| ***SMT391* Output** | |
| Output Data Width | 8-Bits |
| Data Format | Binary |
| ***ADC Performance @ FS = 1 GSPS, FIN = 500 MHz (from Atmel datasheet)*** | |
| Spurious Free Dynamic Range (SFDR) | -57dBc |
| Signal to Noise and Distortion (SINAD) | 45dB |
| Effective Number Of Bits (ENOB) | 7.1 Bits |
| Total Harmonic Distortion (THD) | -55dB |
| Cross-talk channel I versus channel Q (Cr)<br>FIN = 250 MHz, FS = 1 GHz | < -65dBc |

**Figure 2 - Main features.**

## 2.5 Data Stream Description

The data-path for both channels on the module and in the FPGA is identical. The ADC is driven by a clock either generated on the module (one clock for both channels) or provided by the user through a MMBX connectors (one clock for each channel). The following figure is a diagrammatic representation of the data-path inside the FPGA.

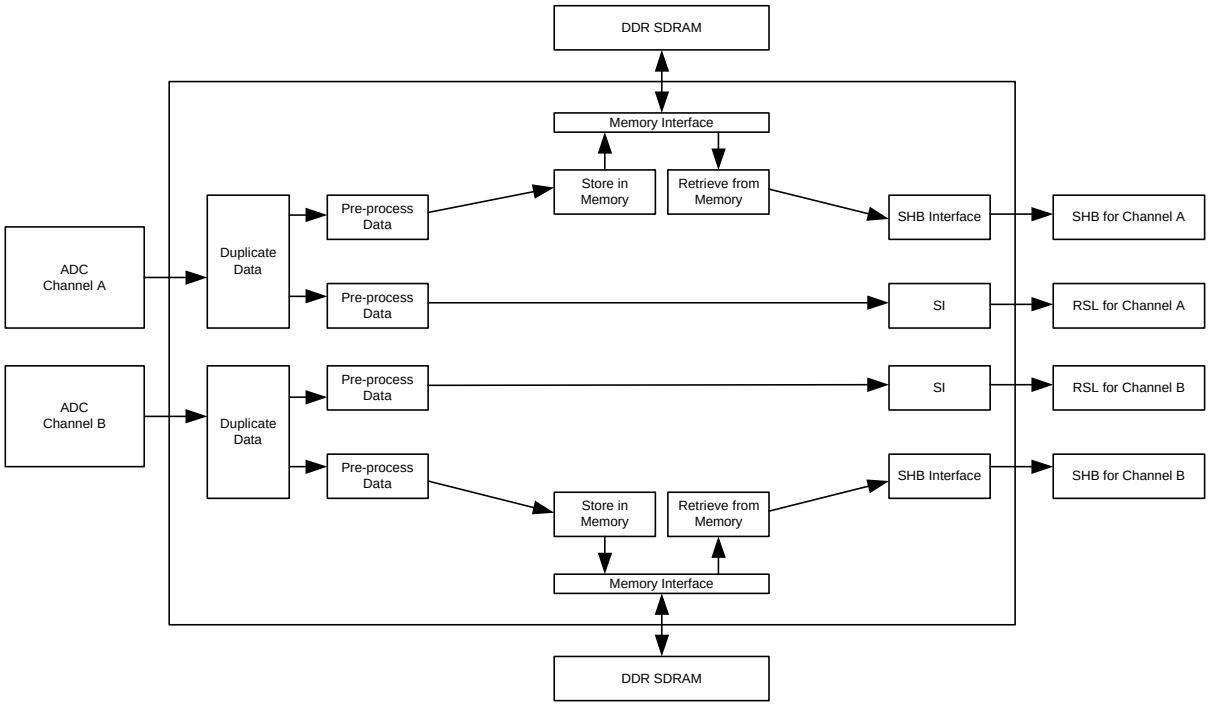



**Figure 3 – Internal FPGA Architecture.**

The analog data is converted by the dual channel ADC converter. A single 16bit parallel LVDS data-stream is generated by the ADC for each channel. This data-stream is duplicated in the FPGA. One stream is transmitted as is over the RSL interface for real-time type applications (not yet supported by current firmware). The second data-stream is stored in DDR SDRAM every time a trigger is received. This data is kept in the memory until a non-real-time type module collects the data over the SHB interface.

### 2.5.1 Description of Internal FPGA Blocks

#### Duplicate Data

This block takes the incoming data stream and makes two copies of it. The first copy is used for real-time type applications where the full conversion data-stream is transmitted off the module. This option is not yet available. The second stream is for non-real-time type applications where samples are captured and stored in memory and then transferred over the SHB interface.

### Pre-processing Data

The data pre-processing block performs basic operations on the data-stream, like decimation (not supported by example firmware, but may be added into firmware design if so required).

### SI

The Serial Interface block takes the parallel input data stream and converts it into a high-speed serial data stream. This data stream is an 8b/10b encoded data stream. On the receiving side the clock is recovered out of the serial data stream and the 10b data is decoded to 8b.

### Store in Memory

The store in memory block takes the incoming data stream and stores the data into DDR SDRAM. This block will only transfer data into the memory when a valid trigger command is received.

### Memory Interface

The memory interface block is the DDR SDRAM controller. This block is responsible to all write and read transactions to and from the DDR SDRAM.

### Retrieve from Memory

The retrieve from memory block retrieves stored data in the DDR SDRAM when it receives a valid read command. The read command specifies the location and amount of data that needs to be retrieved.

### SHB Interface

The retrieved data from the ‘Retrieve from Memory’ block is transmitted over the SHB interface. The SHB interface controls the SHB bus between the SMT391-VP and any module connected to the SHB requesting the data.

In addition to the above interface blocks the FPGA also implements the following functions (not indicated on the diagram):

### Trigger Interface

Handles all triggers. Triggers may be received from the external hardware trigger connectors, or by receiving a trigger command over the ComPort.

### Trigger Interface

Handles all triggers. Triggers may be received from the external hardware trigger connectors (two separate triggers – one for each channel), or by receiving a trigger command over the ComPort (also separate commands for each channel).

### ADC Control Interface

Control interface for writing setup information to the ADC on the SMT391 to configure it for any selected mode of operation. Data is received over the ComPort interface and written out to the clock synthesizer over a serial interface.

### Clock Synthesizer Interface

Control interface for writing setup information to the clock synthesizer on the SMT391 to configure its clock output frequency. Data is received over the ComPort interface and written out to the clock synthesizer over a serial interface.

### PLL Interface

Control interface for writing setup information to the PLL on the SMT391 to configure its two VCO output voltages. Data is received over the ComPort interface and written out to the PLL over a serial interface. The PLL drives two VCO circuits. One VCO + PLL circuit generates the main system clock and is configurable between 600 and 1000 MHz. The side is called the RF side. The other VCO + PLL circuit generates an analog test signal that can be fed back to the ADC input using a one to one RF cable. This side is called the IF side.

### Adc Interface

The ADC interface receives the high speed data stream from the ADC. For each channel it receives a de-multiplex 16-bit data steam at 500 MHz (de-multiplexed because in reality it is an 8-bit 1000 MHz data stream). Data is clocked into the FPGA on an Fs/4 clock on both edges of the clock (Fs/4 output clock is an ADC setup option). From here that data stream is expanded to 64 bits at 125MHz for easier handling inside the FPGA.

### Clock Tree Setup Interface

There are various clock routing configurations available for the SMT391. This interface configures the clock tree.

## 2.6 Clock Structure

There is an integrated clock generator (PLL+VCO clock or Synthesized clock) on the module. The user can either use this clock or provide the module with an external clock (input via MMBX connectors, one for each channel). The RSL interface will only function if the module’s integrated PLL clock is used (RSL is not yet available).

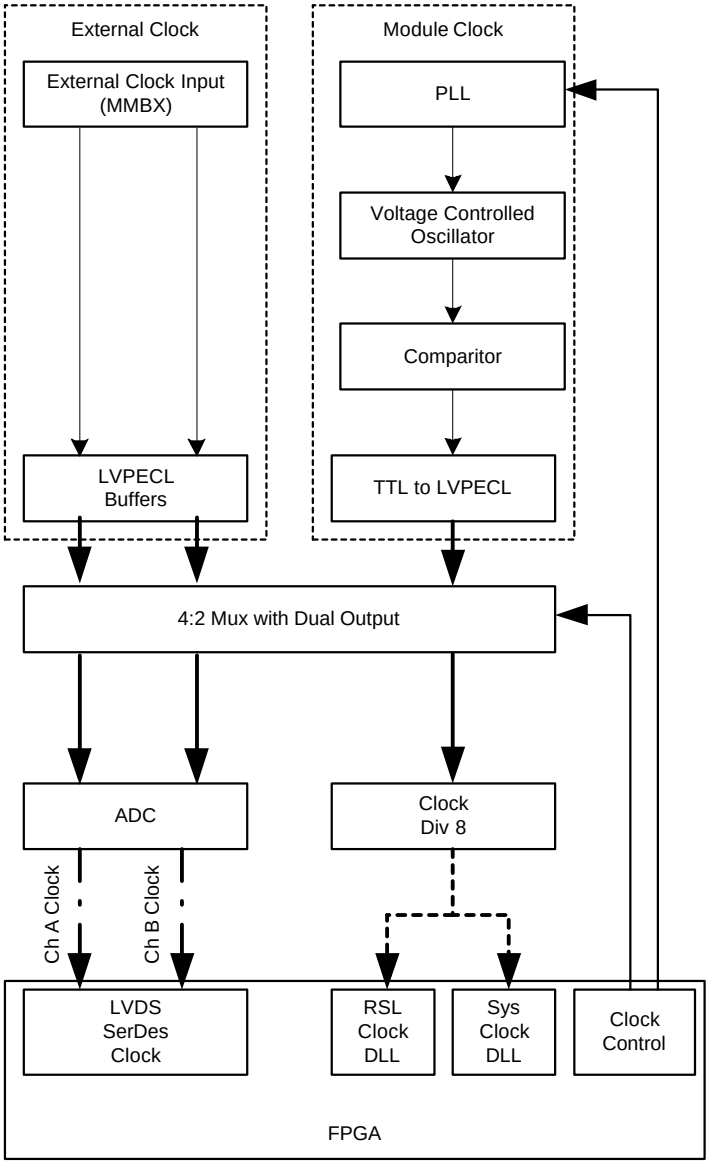



Diagram Key:

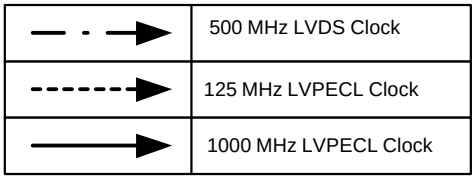



**Figure 4 – Module Clock Structure.**

### 2.6.1 Description of the Clock Tree

The main clock source of the module is a UMC 600MHz to 1000MHz voltage controlled oscillator. The frequency range of the VCO is adjustable with a National PLL. The output of the VCO + PLL combination is passed through a Maxim high

frequency comparator with an LVPECL output to form the main system clock. In addition to this clock there is a clock synthesizer on the module that can generate a 50 to 950 MHz clock. This clock is ideal for testing purposes. Alternatively the user can provide the module with an external LVPECL clock – one input for each channel.

The FPGA controls the LVPECL multiplexers that chooses the final clock (clock synthesizer, PLL+VCO, or external). A copy of this clock is fed to each channel of the ADC. Another copy is divided by 8 (to give a 125MHz LVPECL clock) and fed into the FPGA. (In the current firmware implementation this copy of the clock is not used by the firmware design. The two clocks originating from the ADC is used by the design. This clock can also only be the VCO or the synthesizer clock, not one of the external clocks.)

The ADC clock determines the sampling rate of the ADC. The ADC buffers and divides this clock by two (or four) to provide a 500MHz LVDS clock for each de-multiplexed data channel (or a 250MHz DDR clock depending on the way the ADC is configured). These two clocks are used to clock the ADC data into the FPGA.

When data is transmitted over the RSL links there must be a reference clock on the receiving module that is closely matched in frequency to the transmitting clock. This is important to insure that there will be no data over or under run. Due to this requirement data can only be transmitted over the RSL interface when the on-board VCO clock is used.

All clock circuitry is implemented on the daughter card. The four clocks that enter the FPGA are passed down from the daughter card to the main module. An additional 53MHz oscillator is located on the main module. This oscillator is used as the system clock for the FPGA design.

## 2.7 Trigger Structure

There are two main data-paths (per channel) for data originating from the ADC. The one path transmits all the ADC data as-is over the RSL interface (not yet implemented). The second path captures data samples and stores it in DDR SDRAM memory. This data can then be retrieved at a later stage.

There are two main sources for the trigger. The first is an LVPECL trigger received over the MMBX connector. The second is a trigger command. The trigger command is received over the ComPort interface.

The following trigger settings are possible for the RSL interface (not yet implemented):

- Start transmitting data when a trigger is received. Stop transmitting when the next trigger is received.
- Transmit a pre-determined amount of samples when a trigger is received.
- Ignore all triggers and transmit data continuously.

The following trigger settings are possible for the DDR SDRAM data-path:

- Capture a pre-determined amount of samples when a trigger is received.

Data can be transmitted continuously over the RSL interface. Data can however not be stored continuously in the onboard memory. Data will only be stored when a trigger command is received. This data can then be retrieved at any time over the SHB interface.

The following diagram is a graphical representation of the trigger structure and sources on the SMT391:

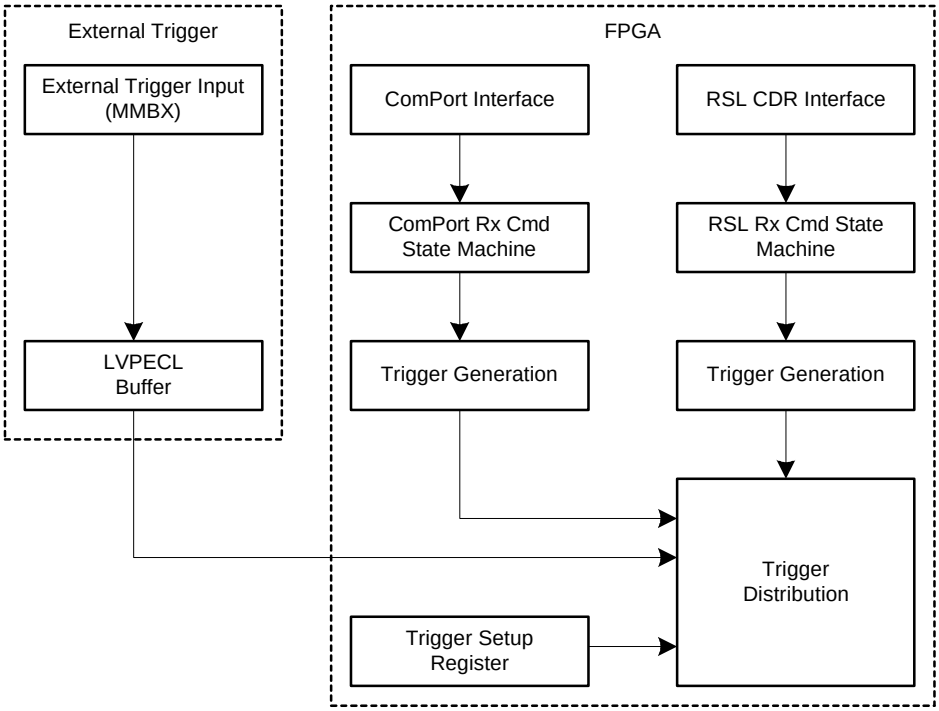



**Figure 5 – Module Trigger Structure.**

## 2.8 Power Supply and Reset Structure

The SMT391-VP conforms to the TIM standard for single width modules. The TIM connectors supply the module with 5.0V, +12V and -12V. The module also requires an additional 3.3V power supply, which must be provided by the two diagonally opposite mounting holes. This 3.3V is present on all *Sundance* TIM carrier boards. From the 5.0V the FPGA Core Voltage ($V_{CCINT}$ = 1.5V), the FPGA Auxiliary voltage ($V_{CCAUX}$ = 2.5V) is generated. The FPGA IO Voltage ($V_{CCO}$ = 3.3V) is taken straight from the TIM mounting holes. The 3.3V, 5.0V, +12V and -12V present on the TIM connector is passed up to the daughter card (SMT391) over the daughter card power connector. 1.5V and 2.5V is also available on the smaller two mounting holes on the SMT338-VP (but not used by the SMT391). The daughter card is responsible for generating its own required voltages.

A TI MSP430 low power microprocessor is located on the main module. This microprocessor controls the power sequencing for the main module. High efficiency DC/DC converters are used to generated the lower voltages.

On the daughter card the Atmel ADC requires digital 3.3V, analog 3.3V and digital 2.25V. The 3.3V from the main module to daughter card power connector is used for the digital 3.3V. This voltage is filtered to provide the analog 3.3V. The 2.25V is generated by a TI low noise low dropout regulator.

The MSP430 microprocessor also controls the reset structure for the SMT391-VP. There are two possible reset sources for the SMT391:

1. A reset is received over the TIM connector
2. After power up an internal POR in the MSP430 causes a reset

The following two diagrams illustrate the power distribution on the SMT391-VP:

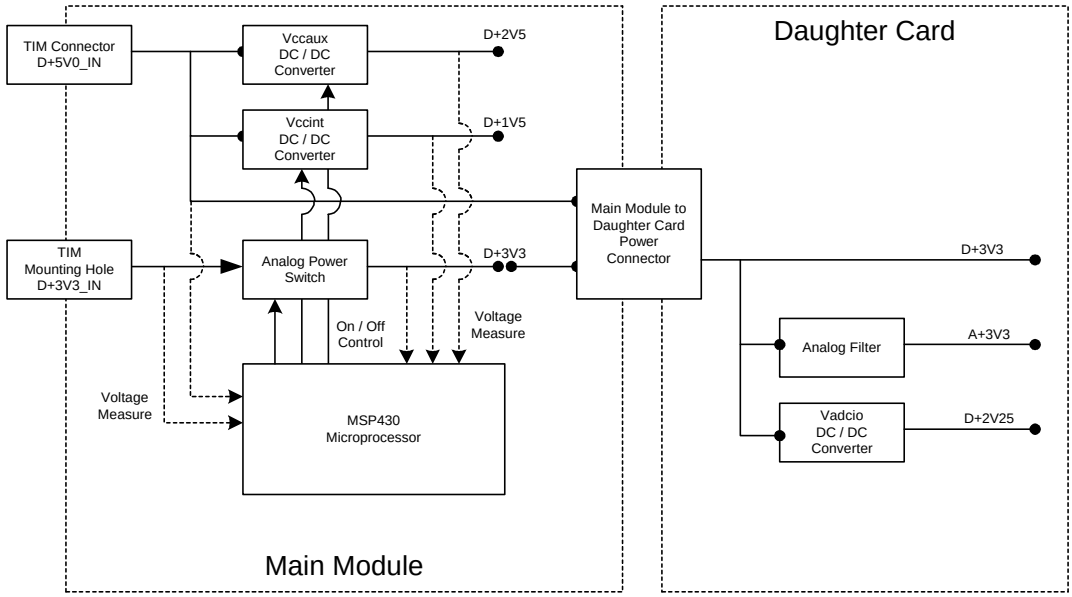



**Figure 6 – Power Generation and Distribution.**

## 2.9 MSP430 Functionality

The MSP430 implements analog control functionality that is difficult to implement in the FPGA. The microprocessor

- Controls the power start-up sequence
- Controls the reset structure on the module

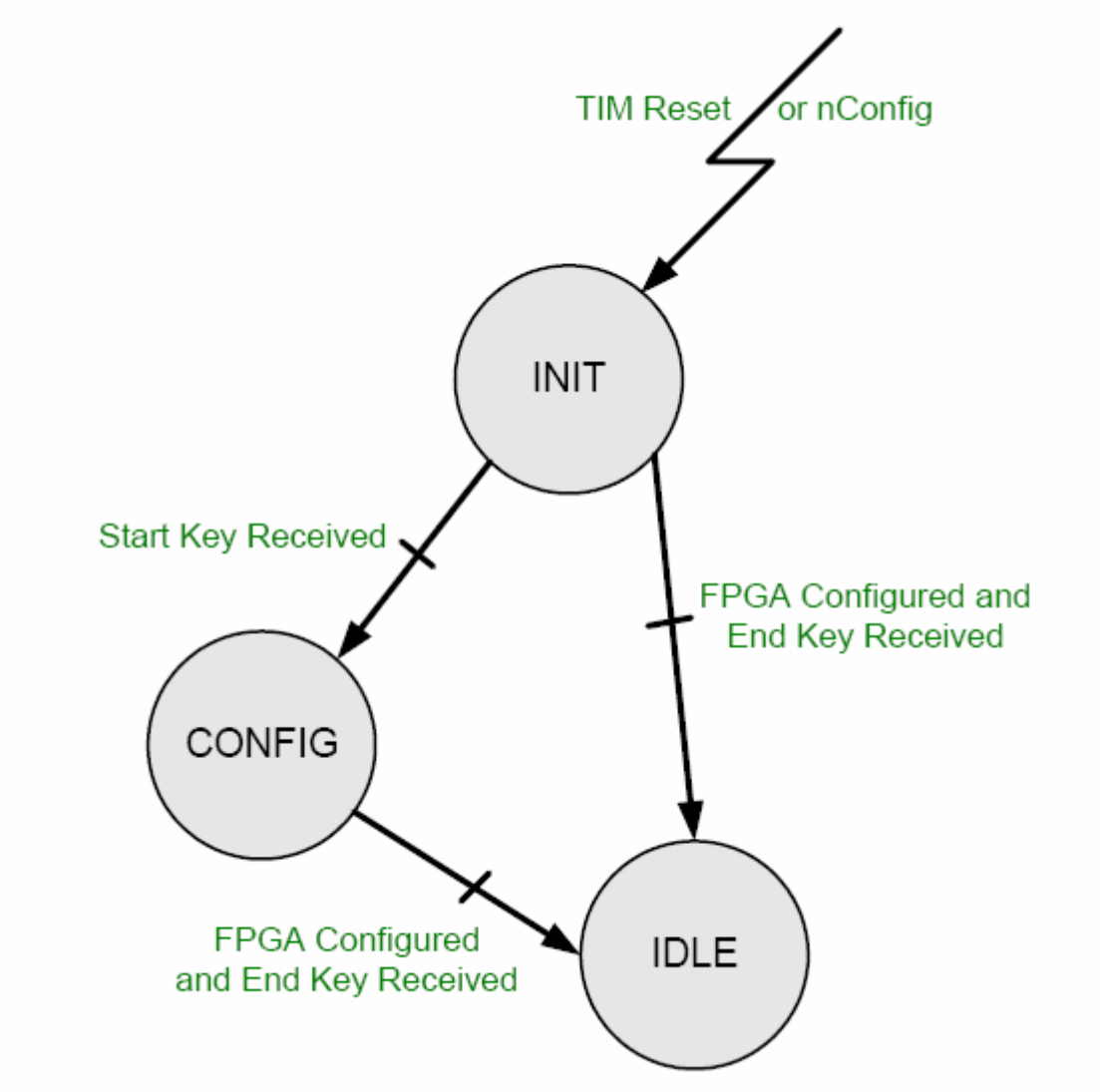



**Figure 7 – Microcontroller State Machine.**

At power-up or on a TIM Reset or on a nConfig line going low, the state machine goes into an *INIT State*. TIM Reset and nConfig lines are available on the carrier module – see TIM Specifications for location on TIM connectors).

From there, it has two choices depending on the state of the FPGA (configured i.e. DONE pin high or un-programmed i.e. DONE Pin Low). To configure the FPGA, simply send a Start Key followed by the bitstream and then and End Key. To re-start the FPGA with the current bitstream loaded, simply send a End Key.

Start Key = 0xBCBCBCBC and End Key = 0xBCBCBC00.

A TIM Reset can be issued to reconfigure the FPGA at anytime, but may reset other modules as well. In the case of reconfiguring a particular module, the nConfig line is used.

MSP430 is connected to ComPort 3 of the TIM. With the standard firmware implementation ComPort 3 is used to communicate with the FPGA. ComPort 0 is open for custom applications as it is not used by the SMT391-VP.

## 2.10 FPGA Configuration

In a typical Sundance system a carrier and host module (most likely a DSP module) is needed to configure the SMT391-VP.

After a hardware reset the FPGA of the SMT391-VP is un-configured and the microprocessor (MSP430) waits for a data stream. At this point the microprocessor is in control of ComPort 3. The host can then send a data stream over ComPort 3 starting with a STARTKEY, then the data, and ending with an ENDKEY. This will configure the FPGA via the microprocessor, and after configuration the microprocessor will release ComPort3 so that the host can talk straight to the FPGA.

If at any time the host want to reset the FPGA the host must send a reset command to it the SMT391-VP over the ComPort – Any hardware resets coming over the TIM site will be caught by the microprocessor but will not be passed on to the FPGA.

If the FPGA is configured, but the host restarts its application, it must send an ENDKEY only. This will 'wake up' the FPGA and the uP will release ComPort 3 so that the host can use it for FPGA communication.

If the host want to reconfigure the FPGA it must toggle the nConfig line on the TIM site. This will give control of the ComPort back to the microprocessor, but it will not un-configure the FPGA. If the host then start sending a new bit-stream starting with a STARTKEY, the FPGA will be un-configured and the new bit-stream will load. If after toggling the nConfig line, if the host does not want to re-configure the FPGA, it must send an ENDKEY like described above.

The above structure makes it possible to:

1) Reset only the FPGA in the system and
2) Make sure that the FPGA is not un-configured every time the host application is re-run as it takes time for the FPGA to re-configure (approximately 35 seconds).

## 2.11 Analog input section

The SMT391 comes with two analogue input options – AC Coupled (SMT391-AC. This is the default option) and DC Coupled (SMT391-DC).

The AC Coupled option uses a twisted pair balun (MACOM TP-101) transformer to convert a single ended signal to a balanced AC Coupled input on the ADC. The figure on the following page shows this setup. Note that the input on the ADC is differential and that for each of these two signals there are two pads on the ADC. One pad connects to the transformer and the second pad is terminated through a 50 Ohm resistor to ground.

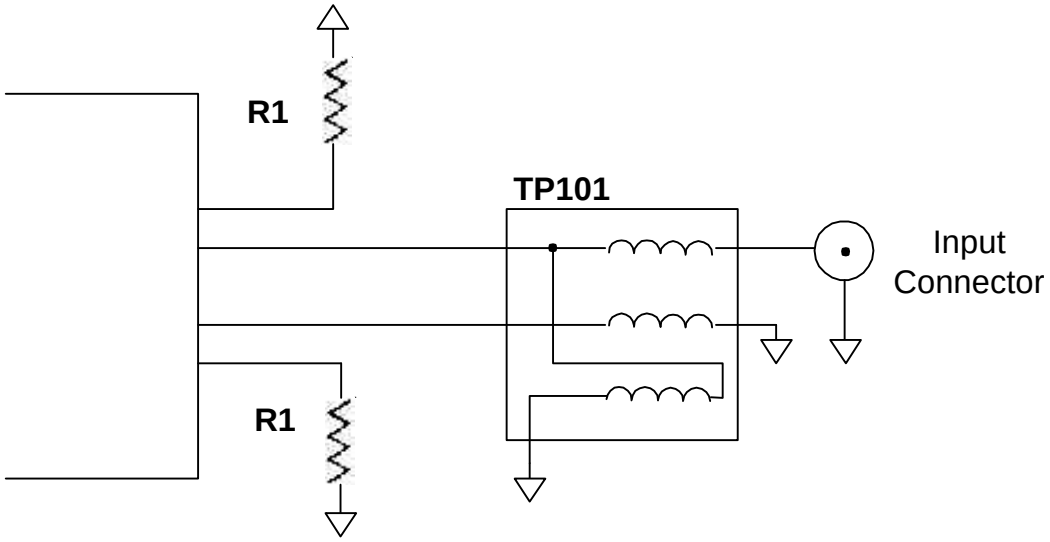



**Figure 8 – AC Coupled Analog Input stage.**

The DC option requires the addition of an “add-on board” which fits onto the MACOM TP-101 footprint. The board uses a 1:1 Balun (Mini-Circuits ADTL1-4-75) transformer to DC couple the input. The advantage of this circuit is that DC signals are preserved, but the drawbacks are that there is a dissymmetry at low frequencies and that only half of the power is transmitted from the source to the receiver. The following figure shows this setup.

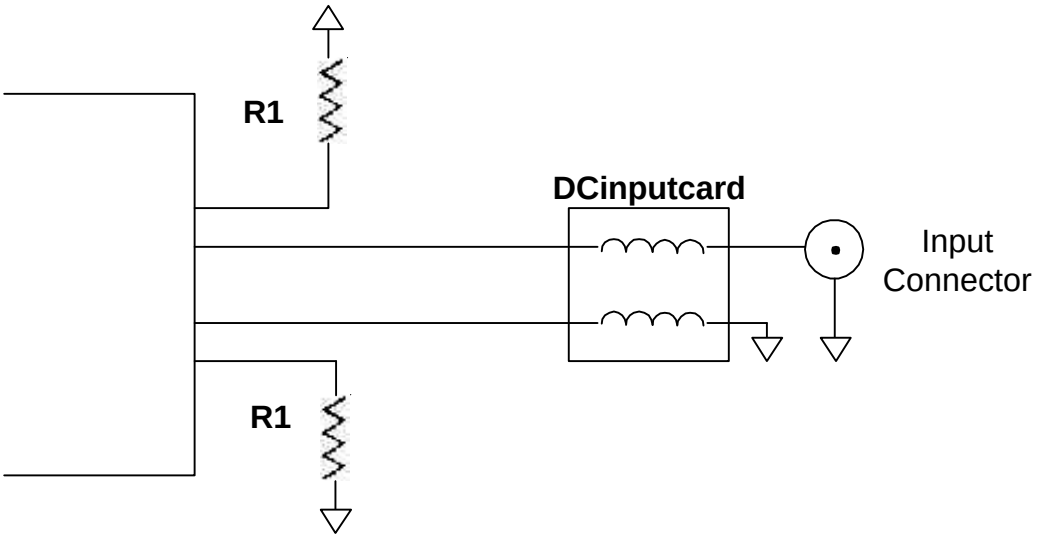



**Figure 9 – DC Coupled Analog Input stage.**

## 2.12 ADC Settings

Support for a sub-set of the command controllable features of the Atmel ADC is implemented in the example firmware of the SMT391-VP. Some of the ADC features are preset on the module and can not be changed by the user. These settings are as follows:

- Data Demux 1:2 mode
- Output Clock Fs/4

The following features may be set by the user:

- Standby / Operational Mode
- Analog Input Mux Setup
- Test Mode / Ramp Mode / Data Mode
- Decimation Mode On / Off

# 3 Description of Interfaces

## 3.1 Memory Interface

Two groups of two 16 bit Micron DDR SDRAMs form the volatile sample storage space of the module. Each DDR SDRAM is 256 MBits in size. This provides the module with a total of 64Mbytes (or 32 Mega samples) of storage space per channel.

Each channel contains a 32 bit DDR SDRAM controller. This interface is capable of data transfer at 1 GBytes / s. It is thus fast enough to write the incoming ADC data stream into memory.

## 3.2 MSP430 Interface

After configuration the microprocessor communicates with the FPGA using the IO pins of the FPGA Slave Select Configuration interface. The MSP is the master of the interface and will continually write the serial number and the measured on-board voltages to the FPGA. A system host can then read this data from the FPGA over the ComPort interface.

## 3.3 Serial Number

A Maxim 1-Wire silicon serial number device is located on the SMT391 and the SMT338-VP. This is used to assign a unique serial number to each module

## 3.4 ADC Control Interface

A three wire uni-directional control interface is implemented between the FPGA and the ADC. This interface is used to clocking configuration information into the ADC. Refer to the ADC datasheet for more information about these settings.

## 3.5 ADC Data Interface

The output of each channel of the ADC is a 16 bit LVDS data bus with a LVDS clock. This clock and data bus is connected straight to high speed LVDS transceivers on the Xilinx Virtex II Pro FPGA. The Data from the I channel maps 1:1 to the data pins on the FPGA. Data from the Q Channel is flipped in hardware. This data must be inverted in the FPGA (this operation is performed in the sampled firmware).

## 3.6 PLL Interface

A three wire uni-directional control interface is implemented between the FPGA and the PLL on the daughter card. This PLL sets and controls the voltage for the VCO that generates the main clock.

## 3.7 Clock Synthesizer Interface

A three wire uni-directional control interface is implemented between the FPGA and the Micrel clock synthesizer on the daughter card. The clock synthesizer can generate a variable 50 – 950 MHz clock. The jitter on this clock is higher than on the main PLL+VCO clock, but it is convenient for testing.

## 3.8 TIM Interface

The SMT391-VP implements ComPorts 0 and 3. There are no DIP switches on the module and all configuration data is received and transmitted over these two ports. The ComPorts are not used for ADC data transfer. ComPort 3 is implemented as a bi-directional transceiver interface for FPGA configuration and control operations. ComPort 0 is available but not used in the default firmware provided with the board.

The Global Bus Interface is not implemented on the SMT391. Refer to [3] for a more detailed description of the TIM interface.

## 3.9 External Trigger

The external trigger input is received by a LVPECL input buffer on the SMT391. The buffered signal is passed down as a differential LVPECL to the FPGA on the SMT338-VP. For compatibility reasons with other daughter card modules there are no ECL termination resistors mounted on the SMT338-VP. For this reason the pulse width of the input trigger must be at least 1uS before the FPGA will register it.

As this might be a problem for some applications this issue has been resolved on the newer SMT338-VP modules and appropriate termination resistors are provided to improve the response time of the FPGA to an external trigger.

For most systems it is likely that there will be a system host (DSP Module). For this reason it is also possible to send a software trigger to the SMT391-VP over ComPort 3. There will however be a latency from the time that the command is sent to the time that data is written into the memory.

## 3.10 RSL Interface (RSL not yet available)

### 3.10.1 RSL Connector and Pinout Definition

The Rocket Serial Link (RSL) is a serial based communications interconnection standard that is capable of transfer speeds of up to 2.5GBit/s per link. Up to four links can be combined to form a Rocket Serial Link Communications Channel (RSLCC) that is capable of data transfer up to 10GBit/s.

Each RSL is made up of a differential Tx and Rx pair. A single RSL can thus transfer data at 2.5GBit/s in both directions at the same time. Rocket Serial Link interconnections are based on the RocketIO standard used on Xilinx Virtex-II Pro FPGAs. Rocket Serial Links uses Low Voltage Differential Signaling (LVDS).

The SMT391-VP uses a subset of the RSL specification. Four RSLs are combined to form a 10GBit/s RSLCC. One RSLCC per ADC channel is implemented on the

SMT391-VP. The RSLCC is thus capable to transfer the raw data stream of the ADC in real time.

The connector used for the RSL interface is a 0.8mm pitch differential Samtec connector. The part number for this connector is: QSE-014-01-F-D-DP-A. The RSL connector takes the place of the optional 3rd and 4th SHB connector on a TIM module. The following diagram shows the position of the RSL connectors on the SMT391-VP:

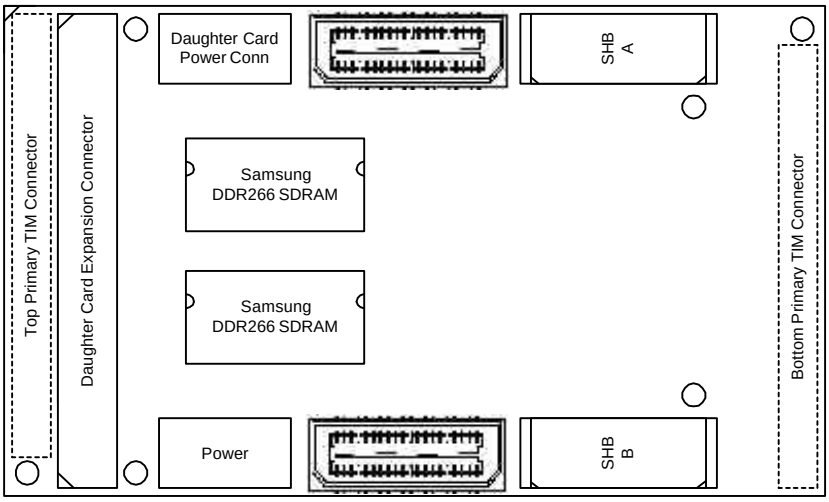
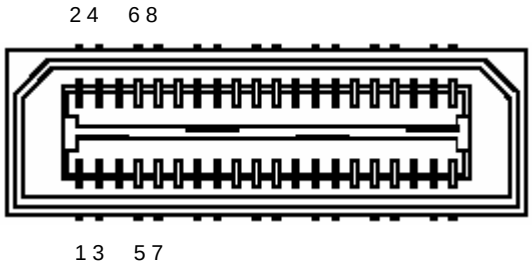



**Figure 10 – Rocket Serial Link Interface.**

There are two additional RSL footprints underneath the module (by default not mounted) in the same place as top RSL connectors. By mounting these two connectors and not the top two it is possible to plug the SMT391-VP straight onto an RSL enabled carrier without having to interconnect the links with cables.




## RSL A

| Pin No | Pin Name | Signal Description | Pin No | Pin Name | Signal Description |
|---|---|---|---|---|---|
| Dir | Carrier / Other Module to SMT391-VP | | Dir | SMT391-VP to Carrier / Other Module | |
| 1 | RxLink0p | Receive Link 0, positive | 2 | TxLink0p | Transmit Link 0, positive |
| 3 | RxLink0n | Receive Link 0, negative | 4 | TxLink0n | Transmit Link 0, negative |
| Dir | Carrier / Other Module to SMT391-VP | | Dir | SMT391-VP to Carrier / Other Module | |
| 5 | RxLink1p | Receive Link 1, positive | 6 | TxLink1p | Transmit Link 1, positive |
| 7 | RxLink1n | Receive Link 1, negative | 8 | TxLink1n | Transmit Link 1, negative |
| Dir | Carrier / Other Module to SMT391-VP | | Dir | SMT391-VP to Carrier / Other Module | |
| 9 | RxLink2p | Receive Link 2, positive | 10 | TxLink2p | Transmit Link 2, positive |
| 11 | RxLink2n | Receive Link 2, negative | 12 | TxLink2n | Transmit Link 2, negative |
| Dir | Carrier / Other Module to SMT391-VP | | Dir | SMT391-VP to Carrier / Other Module | |
| 13 | RxLink3p | Receive Link 3, positive | 14 | TxLink3p | Transmit Link 3, positive |
| 15 | RxLink3n | Receive Link 3, negative | 16 | TxLink3n | Transmit Link 3, negative |
| Dir | Reserved | | Dir | Reserved | |
| 17 | Reserved | Reserved | 18 | Reserved | Reserved |
| 19 | Reserved | Reserved | 20 | Reserved | Reserved |
| Dir | Reserved | | Dir | Reserved | |
| 21 | Reserved | Reserved | 22 | Reserved | Reserved |
| 23 | Reserved | Reserved | 24 | Reserved | Reserved |
| Dir | Reserved | | Dir | Reserved | |
| 25 | Reserved | Reserved | 26 | Reserved | Reserved |
| 27 | Reserved | Reserved | 28 | Reserved | Reserved |

**Figure 11 – Rocket Serial Link Interface Connector and Pinout (RSL A).**

## RSL B

| Pin No | Pin Name | Signal Description | Pin No | Pin Name | Signal Description |
|---|---|---|---|---|---|
| Dir | Carrier / Other Module to SMT391-VP | | Dir | SMT391-VP to Carrier / Other Module | |
| 1 | RxLink0p | Receive Link 0, positive | 2 | TxLink0p | Transmit Link 0, positive |
| 3 | RxLink0n | Receive Link 0, negative | 4 | TxLink0n | Transmit Link 0, negative |
| Dir | Carrier / Other Module to SMT391-VP | | Dir | SMT391-VP to Carrier / Other Module | |
| 5 | RxLink1p | Receive Link 1, positive | 6 | TxLink1p | Transmit Link 1, positive |
| 7 | RxLink1n | Receive Link 1, negative | 8 | TxLink1n | Transmit Link 1, negative |
| Dir | Carrier / Other Module to SMT391-VP | | Dir | SMT391-VP to Carrier / Other Module | |

| | | | | | |
|---|---|---|---|---|---|
| 9 | RxLink2p | Receive Link 2, positive | 10 | TxLink2p | Transmit Link 2, positive |
| 11 | RxLink2n | Receive Link 2, negative | 12 | TxLink2n | Transmit Link 2, negative |
| Dir | Carrier / Other Module to SMT391-VP | | Dir | SMT391-VP to Carrier / Other Module | |
| 13 | RxLink3p | Receive Link 3, positive | 14 | TxLink3p | Transmit Link 3, positive |
| 15 | RxLink3n | Receive Link 3, negative | 16 | TxLink3n | Transmit Link 3, negative |
| Dir | Reserved | | Dir | Reserved | |
| 17 | Reserved | Reserved | 18 | Reserved | Reserved |
| 19 | Reserved | Reserved | 20 | Reserved | Reserved |
| Dir | Reserved | | Dir | Reserved | |
| 21 | Reserved | Reserved | 22 | Reserved | Reserved |
| 23 | Reserved | Reserved | 24 | Reserved | Reserved |
| Dir | Reserved | | Dir | Reserved | |
| 25 | Reserved | Reserved | 26 | Reserved | Reserved |
| 27 | Reserved | Reserved | 28 | Reserved | Reserved |

**Figure 12 – Rocket Serial Link Interface Connector and Pinout (RSL B).**

### 3.10.2 RSL Cable Definition

The matching cable for the RSL connector is a Samtec High Speed Data Link Cable (Samtec HFEM Series). The cable may be ordered with different length and mating connector options. The following diagram shows such a typical cable:

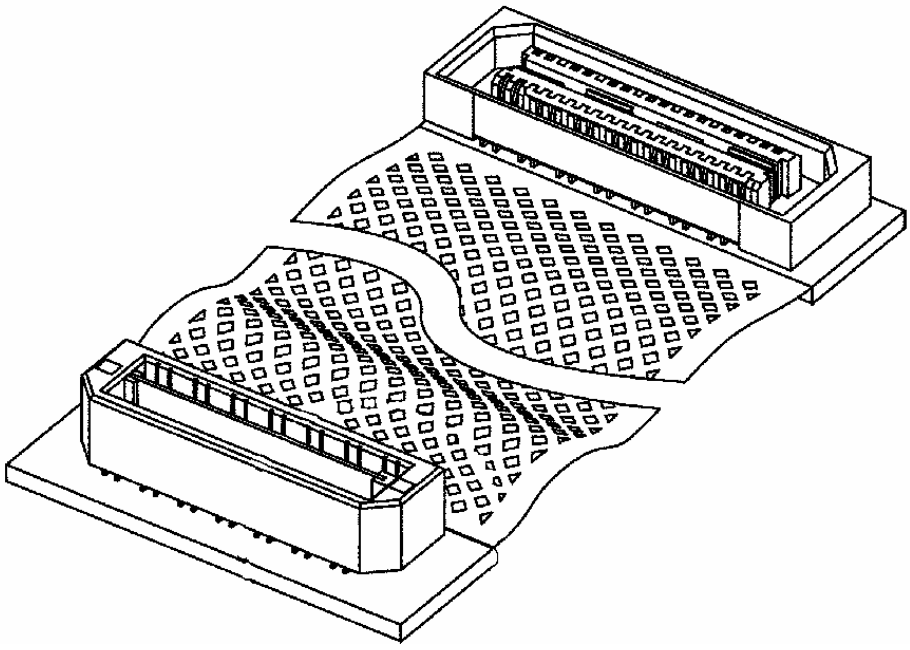


**Figure 13 – Samtec HFEM Series Data Cable.**

## 3.11 SHB Interface

The SMT391-VP implements a subset of the full SHB implementation. Two configurations are possible

1. SHB A is configured to transmit 32-bit data words for channel A and SHB B is configured to transmit 32-bit data words for channel B. Both SHB interfaces are configured as outputs only. Control and configuration data is received over ComPort 3. The SHB interface is clocked by the SMT338-VP system clock of 53MHz.
2. SHB A is configured to transmit two 16-bit half-words. The first 16-bits is used for data from channel A and the second 16-bits is used for data from channel B. SHB B is configured in exactly the same way and transmit a copy of the data SHB A transmits. (This option is not implemented in firmware.)

The first configuration is ideal for higher speed data transfer. The second configuration can be used if (a) just one SHB is available on a module that the SMT391-VP interfaces to, or (b) when the data stream must be passed on to two different end points. The two possible configurations are illustrated in the following figure:

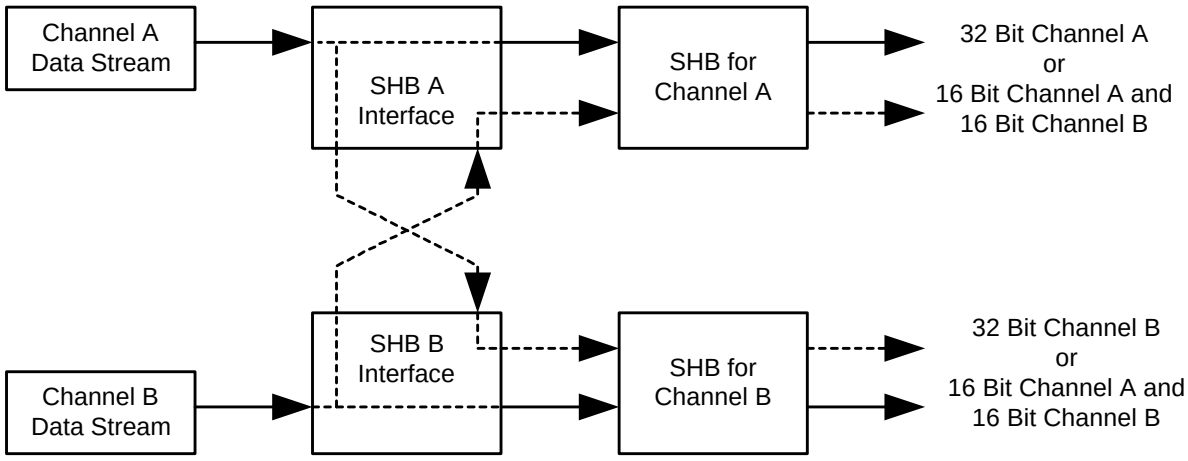
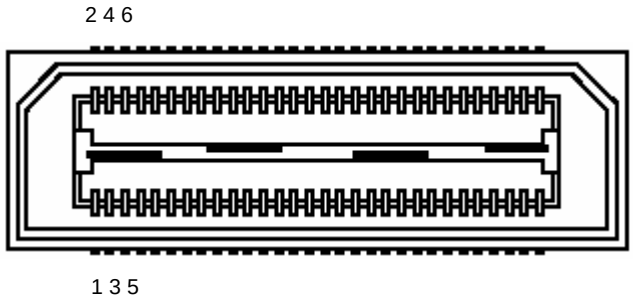



**Figure 14 – Possible SHB Configurations.**

The connector used for the SHB interface is a 0.5mm Samtec QSH Type connector. The full part number for this connector is: QSH-030-01-L-D-A-K

The pinout information for the two possible configurations for both SHB connectors is given in the following table:

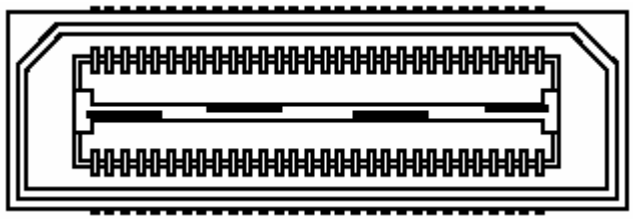



## SHB A and SHB B, Configuration 1 (X = A for SHB A, X = B for SHB B)

| Pin No | Pin Name | Direction | Signal Description | Pin No | Pin Name | Direction | Signal Description |
|---|---|---|---|---|---|---|---|
| 1 | ChXClk | From 391 | Ch X, Word Clock | 31 | ChXD29 | From 391 | Ch X, Word Data 29 |
| 2 | ChXD0 | From 391 | Ch X, Word Data 0 | 32 | ChXD30 | From 391 | Ch X, Word Data 30 |
| 3 | ChXD1 | From 391 | Ch X, Word Data 1 | 33 | ChXD31 | From 391 | Ch X, Word Data 31 |
| 4 | ChXD2 | From 391 | Ch X, Word Data 2 | 34 | ChXWen | From 391 | Ch X, Write Enable |
| 5 | ChXD3 | From 391 | Ch X, Word Data 3 | 35 | ChXReq | Reserved | Not Implemented |
| 6 | ChXD4 | From 391 | Ch X, Word Data 4 | 36 | ChXAck | Reserved | Not Implemented |
| 7 | ChXD5 | From 391 | Ch X, Word Data 5 | 37 | Reserved | Reserved | Reserved |
| 8 | ChXD6 | From 391 | Ch X, Word Data 6 | 38 | Reserved | Reserved | Reserved |
| 9 | ChXD7 | From 391 | Ch X, Word Data 7 | 39 | Reserved | Reserved | Reserved |
| 10 | ChXD8 | From 391 | Ch X, Word Data 8 | 40 | Reserved | Reserved | Reserved |
| 11 | ChXD9 | From 391 | Ch X, Word Data 9 | 41 | Reserved | Reserved | Reserved |
| 12 | ChXD10 | From 391 | Ch X, Word Data 10 | 42 | Reserved | Reserved | Reserved |
| 13 | ChXD11 | From 391 | Ch X, Word Data 11 | 43 | Reserved | Reserved | Reserved |
| 14 | ChXD12 | From 391 | Ch X, Word Data 12 | 44 | Reserved | Reserved | Reserved |
| 15 | ChXD13 | From 391 | Ch X, Word Data 13 | 45 | Reserved | Reserved | Reserved |
| 16 | ChXD14 | From 391 | Ch X, Word Data 14 | 46 | Reserved | Reserved | Reserved |
| 17 | ChXD15 | From 391 | Ch X, Word Data 15 | 47 | Reserved | Reserved | Reserved |
| 18 | ChXD16 | From 391 | Ch X, Word Data 16 | 48 | Reserved | Reserved | Reserved |
| 19 | ChXD17 | From 391 | Ch X, Word Data 17 | 49 | Reserved | Reserved | Reserved |
| 20 | ChXD18 | From 391 | Ch X, Word Data 18 | 50 | Reserved | Reserved | Reserved |
| 21 | ChXD19 | From 391 | Ch X, Word Data 19 | 51 | Reserved | Reserved | Reserved |
| 22 | ChXD20 | From 391 | Ch X, Word Data 20 | 52 | Reserved | Reserved | Reserved |
| 23 | ChXD21 | From 391 | Ch X, Word Data 21 | 53 | Reserved | Reserved | Reserved |
| 24 | ChXD22 | From 391 | Ch X, Word Data 22 | 54 | Reserved | Reserved | Reserved |
| 25 | ChXD23 | From 391 | Ch X, Word Data 23 | 55 | Reserved | Reserved | Reserved |
| 26 | ChXD24 | From 391 | Ch X, Word Data 24 | 56 | Reserved | Reserved | Reserved |
| 27 | ChXD25 | From 391 | Ch X, Word Data 25 | 57 | Reserved | Reserved | Reserved |
| 28 | ChXD26 | From 391 | Ch X, Word Data 26 | 58 | Reserved | Reserved | Reserved |
| 29 | ChXD27 | From 391 | Ch X, Word Data 27 | 59 | Reserved | Reserved | Reserved |
| 30 | ChXD28 | From 391 | Ch X, Word Data 28 | 60 | Reserved | Reserved | Reserved |

**Figure 15 –SHB Connector Configuration 1 Pinout.**

2 4 6



1 3 5

## SHB A and SHB B, Configuration 2

| Pin No | Pin Name | Direction | Signal Description | Pin No | Pin Name | Direction | Signal Description |
|---|---|---|---|---|---|---|---|
| 1 | ChAClk | From 391 | Ch A, ½Word Clock | 31 | Reserved | Reserved | Reserved |
| 2 | ChAD0 | From 391 | Ch A, ½Word Data 0 | 32 | Reserved | Reserved | Reserved |
| 3 | ChAD1 | From 391 | Ch A, ½Word Data 1 | 33 | Reserved | Reserved | Reserved |
| 4 | ChAD2 | From 391 | Ch A, ½Word Data 2 | 34 | Reserved | Reserved | Reserved |
| 5 | ChAD3 | From 391 | Ch A, ½Word Data 3 | 35 | Reserved | Reserved | Reserved |
| 6 | ChAD4 | From 391 | Ch A, ½Word Data 4 | 36 | Reserved | Reserved | Reserved |
| 7 | ChAD5 | From 391 | Ch A, ½Word Data 5 | 37 | ChBClk | From 391 | Ch B, ½Word Clock |
| 8 | ChAD6 | From 391 | Ch A, ½Word Data 6 | 38 | ChBD0 | From 391 | Ch B, ½Word Data 0 |
| 9 | ChAD7 | From 391 | Ch A, ½Word Data 7 | 39 | ChBD1 | From 391 | Ch B, ½Word Data 1 |
| 10 | ChAD8 | From 391 | Ch A, ½Word Data 8 | 40 | ChBD2 | From 391 | Ch B, ½Word Data 2 |
| 11 | ChAD9 | From 391 | Ch A, ½Word Data 9 | 41 | ChBD3 | From 391 | Ch B, ½Word Data 3 |
| 12 | ChAD10 | From 391 | Ch A, ½Word Data 10 | 42 | ChBD4 | From 391 | Ch B, ½Word Data 4 |
| 13 | ChAD11 | From 391 | Ch A, ½Word Data 11 | 43 | ChBD5 | From 391 | Ch B, ½Word Data 5 |
| 14 | ChAD12 | From 391 | Ch A, ½Word Data 12 | 44 | ChBD6 | From 391 | Ch B, ½Word Data 6 |
| 15 | ChAD13 | From 391 | Ch A, ½Word Data 13 | 45 | ChBD7 | From 391 | Ch B, ½Word Data 7 |
| 16 | ChAD14 | From 391 | Ch A, ½Word Data 14 | 46 | ChBD8 | From 391 | Ch B, ½Word Data 8 |
| 17 | ChAD15 | From 391 | Ch A, ½Word Data 15 | 47 | ChBD9 | From 391 | Ch B, ½Word Data 9 |
| 18 | ChAUser0 | Reserved | Not Implemented | 48 | ChBD10 | From 391 | Ch B, ½Word Data 10 |
| 19 | ChAUser1 | Reserved | Not Implemented | 49 | ChBD11 | From 391 | Ch B, ½Word Data 11 |
| 20 | ChAUser2 | Reserved | Not Implemented | 50 | ChBD12 | From 391 | Ch B, ½Word Data 12 |
| 21 | ChAUser3 | Reserved | Not Implemented | 51 | ChBD13 | From 391 | Ch B, ½Word Data 13 |
| 22 | ChAWen | From 391 | Ch A, Write Enable | 52 | ChBD14 | From 391 | Ch B, ½Word Data 14 |
| 23 | ChAReq | Reserved | Not Implemented | 53 | ChBD15 | From 391 | Ch B, ½Word Data 15 |
| 24 | ChAAck | Reserved | Not Implemented | 54 | ChBUser0 | Reserved | Not Implemented |
| 25 | Reserved | Reserved | Reserved | 55 | ChBUser1 | Reserved | Not Implemented |
| 26 | Reserved | Reserved | Reserved | 56 | ChBUser2 | Reserved | Not Implemented |
| 27 | Reserved | Reserved | Reserved | 57 | ChBUser3 | Reserved | Not Implemented |
| 28 | Reserved | Reserved | Reserved | 58 | ChBWen | From 391 | Ch B, Write Enable |
| 29 | Reserved | Reserved | Reserved | 59 | ChBReq | Reserved | Not Implemented |
| 30 | Reserved | Reserved | Reserved | 60 | ChBAck | Reserved | Not Implemented |

**Figure 16 –SHB Connector Configuration 2 Pinout.**

## 3.12 Daughter-card Interface

The daughter-card interface is made up of two connectors. The one is a 0.5mm pitch differential Samtec connector. This connector is for transferring the ADC LVDS output data to the FPGA on the main module. The second one is a 1mm pitch Samtec header type connector. This connector is for providing power to the daughter-card.

The figure underneath illustrates this configuration. The bottom view of the daughter card is shown on the right. This view must the mirrored to understand how it connects to the main module.

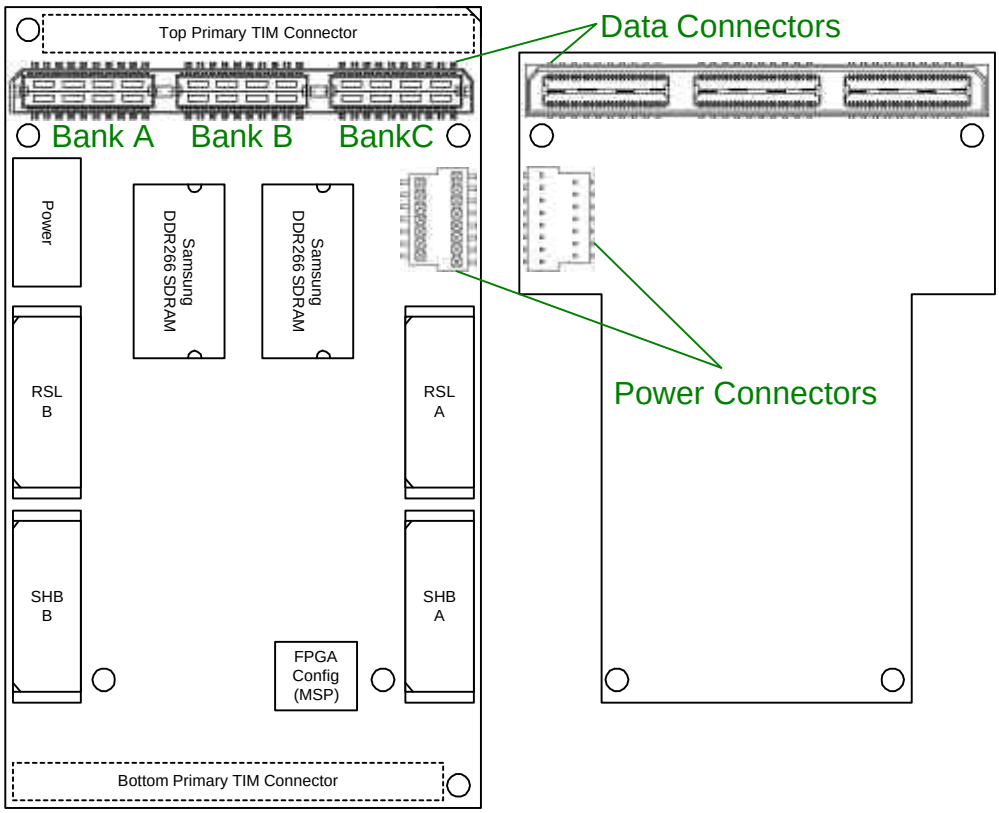



**Figure 17 – Daughter Card Connector Interface.**

The female differential connector is located on the main module. The Samtec Part Number for this connector is QTH-060-01-F-D-DP-A.

The female power connector is located on the main module. The Samtec Part Number for this connector is BKS-107-01-F-V-A

The male differential connector is located on the daughter card. The Samtec Part Number for this connector is QSH-060-01-F-D-DP-A

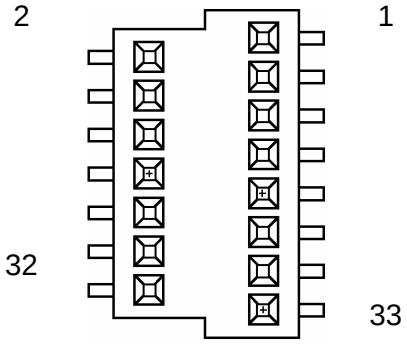
The male power connector is located on the daughter card. The Samtec Part Number for this connector is BKT-107-03-F-V-A

The mated height between the main module and the daughter card is 5 mm.

Each pin on the power connector (33 pins in total) can carry 1.5 A. Digital 5V (D+5V0), digital 3V3 (D+3V3), -12V (D-12V0), +12V (D+12V0) and digital ground (DGND) is provided over this connector. D+3V3 and D+5V0 are assigned four pins each. The daughter card can thus draw a total of 6A of each of these two supplies. The integral ground plane on the differential connector provides additional grounding.

DSP JTAG lines are also mapped onto this connector to be used in case the Daughter module contains a TI DSP on it. They would allow easy debugging and programming via JTAG as Sundance carriers are 'JTAG enabled'.

The following table shows the pin assignment on the power connector:

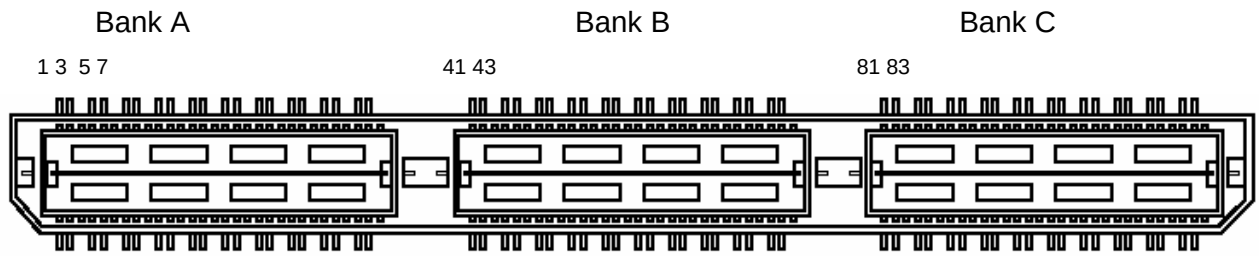



| Pin Number | Pin Name | Description of Signal |
|---|---|---|
| 1 | D+3V3 | Digital 3.3 Volts |
| 2 | DGND | Digital Ground |
| 3 | D+3V3 | Digital 3.3 Volts |
| 4 | DGND | Digital Ground |
| 5 | D+3V3 | Digital 3.3 Volts |
| 6 | DGND | Digital Ground |
| 7 | D+3V3 | Digital 3.3 Volts |
| 8 | DGND | Digital Ground |
| 9 | D+5V0 | Digital 5.0 Volts |
| 10 | DGND | Digital Ground |
| 11 | D+5V0 | Digital 5.0 Volts |
| 12 | DGND | Digital Ground |
| 13 | D+5V0 | Digital 5.0 Volts |
| 14 | DGND | Digital Ground |
| 15 | D+5V0 | Digital 5.0 Volts |
| 16 | DGND | Digital Ground |
| 17 | D+12V0 | Digital 12.0 Volts |
| 18 | DGND | Digital Ground |
| 19 | D+12V0 | Digital 12.0 Volts |
| 20 | DGND | Digital Ground |
| 21 | D-12V0 | Digital -12.0 Volts |
| 22 | DGND | Digital Ground |

| | | |
|---|---|---|
| 23 | D-12V0 | Digital -12.0 Volts |
| 24 | DGND | Digital Ground |
| 25 | DGND | Digital Ground |
| 26 | EMU0 | Emulation Control 0 |
| 27 | EMU1 | Emulation Control 1 |
| 28 | TMS | JTAG Mode Control |
| 29 | nTRST | JTAG Reset |
| 30 | TCK | JTAG Test Clock |
| 31 | TDI | JTAG Test Input |
| 32 | TDO | JTAG Test Output |
| 33 | DGND | Digital Ground |

**Figure 18 – Daughter Card Interface Power Connector and Pinout.**

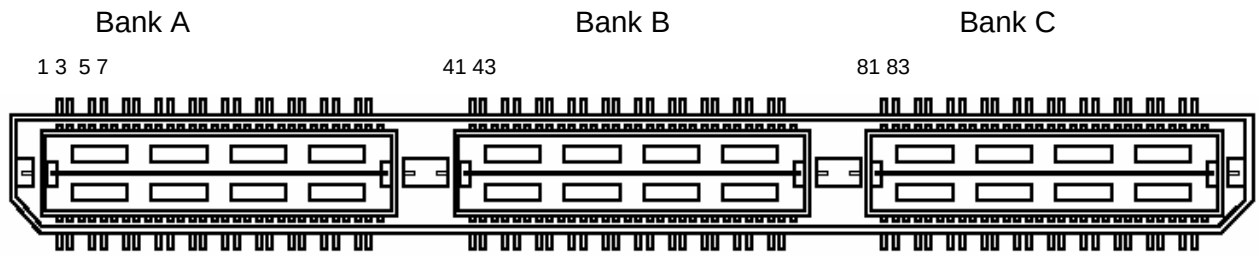
The following few pages describes the signals on the data connector between the main module and the daughter card. Bank A on the connector is used for the ADC I Channel data bus. Bank C is used for the ADC Q channel data bus. Bank B is used for system clock and trigger signals, ADC control signals and general system control signals. The general system control signals include: PLL control interface (for the VCO circuit), daughter card serial number signal, clock synthesizer control, ADC control, power control signals and daughter card reset signal. All reserved signals are connected to the FPGA on the main module for future expansion.




## Bank A

| Pin No | Pin Name | Signal Description | Pin No | Pin Name | Signal Description |
|---|---|---|---|---|---|
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 1 | DOAI0p | Data Out 0 A, I channel, pos. | 2 | DOBI0p | Data Out 0 B, I channel, pos. |
| 3 | DOAI0n | Data Out 0 A, I channel, neg. | 4 | DOBI0n | Data Out 0 B, I channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 5 | DOAI1p | Data Out 1 A, I channel, pos. | 6 | DOBI1p | Data Out 1 B, I channel, pos. |
| 7 | DOAI1n | Data Out 1 A, I channel, neg. | 8 | DOBI1n | Data Out 1 B, I channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 9 | DOAI2p | Data Out 2 A, I channel, pos. | 10 | DOBI2p | Data Out 2 B, I channel, pos. |
| 11 | DOAI2n | Data Out 2 A, I channel, neg. | 12 | DOBI2n | Data Out 2 B, I channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 13 | DOAI3p | Data Out 3 A, I channel, pos. | 14 | DOBI3p | Data Out 3 B, I channel, pos. |
| 15 | DOAI3n | Data Out 3 A, I channel, neg. | 16 | DOBI3n | Data Out 3 B, I channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 17 | DOAI4p | Data Out 4 A, I channel, pos. | 18 | DOBI4p | Data Out 4 B, I channel, pos. |
| 19 | DOAI4n | Data Out 4 A, I channel, neg. | 20 | DOBI4n | Data Out 4 B, I channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 21 | DOAI5p | Data Out 5 A, I channel, pos. | 22 | DOBI5p | Data Out 5 B, I channel, pos. |
| 23 | DOAI5n | Data Out 5 A, I channel, neg. | 24 | DOBI5n | Data Out 5 B, I channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 25 | DOAI6p | Data Out 6 A, I channel, pos. | 26 | DOBI6p | Data Out 6 B, I channel, pos. |
| 27 | DOAI6n | Data Out 6 A, I channel, neg. | 28 | DOBI6n | Data Out 6 B, I channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 29 | DOAI7p | Data Out 7 A, I channel, pos. | 30 | DOBI7p | Data Out 7 B, I channel, pos. |
| 31 | DOAI7n | Data Out 7 A, I channel, neg. | 32 | DOBI7n | Data Out 7 B, I channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 33 | ClkOIp | Output Ready, I channel, pos | 34 | DOIRIp | In Range, I channel, pos |
| 35 | ClkOIn | Output Ready, I channel, neg | 36 | DOIRIn | In Range, I channel, neg |
| Dir | Reserved | | Dir | Reserved | |
| 37 | Reserved | Reserved | 38 | Reserved | Reserved |
| 39 | Reserved | Reserved | 40 | Reserved | Reserved |

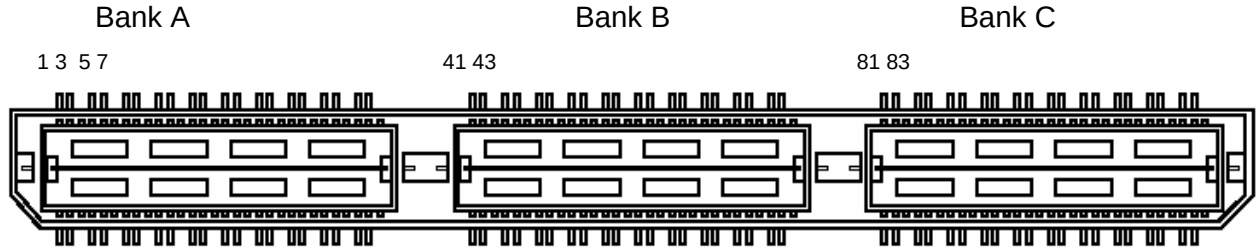
**Figure 19 – Daughter Card Interface: Data Signals Connector and Pinout (Bank A).**




## Bank B

| Pin No | Pin Name | Signal Description | Pin No | Pin Name | Signal Description |
|---|---|---|---|---|---|
| **Type** | **Reserved** | | **Type** | **Reserved** | |
| Dir | Reserved | | Dir | Reserved | |
| 41 | SMBClk | Temperature Sensor Clock | 42 | SMBData | Temperature Sensor Data |
| 43 | SMBnAlert | Temperature Sensor Alert | 44 | Serial No | Serial Number Data Line |
| Dir | Reserved | | Dir | Reserved | |
| 45 | AdcVDacI | Reserved | 46 | AdcVDacI | Reserved |
| 47 | AdcVRes | Reserved | 48 | AdcReset | ADC Reset |
| Dir | Reserved | | Dir | Reserved | |
| 49 | D3v3Enable | 3.3V Power Enable | 50 | D2V5Enable | 2.5V Power Enable |
| 51 | AdcMode | ADC Mode Select | 52 | AdcClock | ADC Serial Clock |
| **Type** | **Reserved** | | **Type** | **Reserved** | |
| Dir | Reserved | | Dir | Reserved | |
| 53 | AdcLoad | ADC Serial Load | 54 | AdcData | ADC Serial Data |
| 55 | AdcCal | ADC Calibration | 56 | AdjClkCntr0 | Adj Clock Serial Clock |
| Dir | Reserved | | Dir | Reserved | |
| 57 | AdjClkCntrl1 | Adj Clock Serial Data | 58 | AdjClkCntrl2 | Adj Clock Serial Load |
| 59 | AdjClkCntrl3 | Adj Clock Serial Test | 60 | PllCntrl0 | Pll Serial Clock |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 61 | PllCntrl1 | Pll Serial Data | 62 | PllCntrl2 | Pll Serial Load |
| 63 | PllCntrl3 | Pll Serial Test | 64 | AdcAClkSel | Clock Selection, Ch A |
| **Type** | **Reserved** | | **Type** | **Reserved** | |
| Dir | Reserved | | Dir | Reserved | |
| 65 | AdcBClkSel | Clock Selection, Ch B | 66 | IntClkDivEn | Internal Clock Divide Enable |
| 67 | IntClkDivnReset | Int Clock Divide Reset | 68 | IntExtClkDivEn | Int Ext Clock Divide Enable |
| Dir | Reserved | | Dir | Reserved | |
| 69 | IntExtClkDivnReset | | 70 | FpgaVRef | JTAG FPGA VRef |
| 71 | FpgaTck | JTAG FPGA Tck | 72 | FpgaTms | JTAG FPGA Tms |
| Dir | Reserved | | Dir | Reserved | |
| 73 | FpgaTdi | JTAG FPGA Tdi | 74 | FpgaTdo | JTAG FPGA Tdo |
| 75 | MspVRef | JTAG MSP430 VRef | 76 | MspTck | JTAG MSP430 Tck |
| Dir | Reserved | | Dir | Reserved | |
| 77 | MspTms | JTAG MSP430 Tms | 78 | MspTdi | JTAG MSP430 Tdi |
| 79 | MspTdo | JTAG MSP430 Tdo | 80 | MspnTrst | JTAG MSP430 nTrst |

**Figure 20 – Daughter Card Interface: Data Signals Connector and Pinout (Bank B).**




## Bank C

| Pin No | Pin Name | Signal Description | Pin No | Pin Name | Signal Description |
|---|---|---|---|---|---|
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 81 | DOAQ0p | Data Out 0 A, Q channel, pos. | 82 | DOBQ0p | Data Out 0 B, Q channel, pos. |
| 83 | DOAQ0n | Data Out 0 A, Q channel, neg. | 84 | DOBQ0n | Data Out 0 B, Q channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 85 | DOAQ1p | Data Out 1 A, Q channel, pos. | 86 | DOBQ1p | Data Out 1 B, Q channel, pos. |
| 87 | DOAQ1n | Data Out 1 A, Q channel, neg. | 88 | DOBQ1n | Data Out 1 B, Q channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 89 | DOAQ2p | Data Out 2 A, Q channel, pos. | 90 | DOBQ2p | Data Out 2 B, Q channel, pos. |
| 91 | DOAQ2n | Data Out 2 A, Q channel, neg. | 92 | DOBQ2n | Data Out 2 B, Q channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 93 | DOAQ3p | Data Out 3 A, Q channel, pos. | 94 | DOBQ3p | Data Out 3 B, Q channel, pos. |
| 95 | DOAQ3n | Data Out 3 A, Q channel, neg. | 96 | DOBQ3n | Data Out 3 B, Q channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 97 | DOAQ4p | Data Out 4 A, Q channel, pos. | 98 | DOBQ4p | Data Out 4 B, Q channel, pos. |
| 99 | DOAQ4n | Data Out 4 A, Q channel, neg. | 100 | DOBQ4n | Data Out 4 B, Q channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 101 | DOAQ5p | Data Out 5 A, Q channel, pos. | 102 | DOBQ5p | Data Out 5 B, Q channel, pos. |
| 103 | DOAQ5n | Data Out 5 A, Q channel, neg. | 104 | DOBQ5n | Data Out 5 B, Q channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 105 | DOAQ6p | Data Out 6 A, Q channel, pos. | 106 | DOBQ6p | Data Out 6 B, Q channel, pos. |
| 107 | DOAQ6n | Data Out 6 A, Q channel, neg. | 108 | DOBQ6n | Data Out 6 B, Q channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 109 | DOAQ7p | Data Out 7 A, Q channel, pos. | 110 | DOBQ7p | Data Out 7 B, Q channel, pos. |
| 111 | DOAQ7n | Data Out 7 A, Q channel, neg. | 112 | DOBQ7n | Data Out 7 B, Q channel, neg. |
| Dir | Daughter Card to Main Module | | Dir | Daughter Card to Main Module | |
| 113 | ClkOQp | Output Ready, Q channel, pos | 114 | DOIRQp | In Range, Q channel, pos |
| 115 | ClkOQn | Output Ready, Q channel, neg | 116 | DOIRQn | In Range, Q channel, neg |
| Dir | Reserved | | Dir | Reserved | |
| 117 | Reserved | Reserved | 118 | Reserved | Reserved |
| 119 | Reserved | Reserved | 120 | Reserved | Reserved |

**Figure 21 – Daughter Card Interface: Data Signals Connector and Pinout (Bank C).**

# 4 Firmware Description

## 4.1 Main States

At reset, the FPGA is in the INIT state where internal memory and registers are reset. It then waits for an acquisition trigger command to happen to start storing data into the internal memory (state “STORE”). Once the memory is full, data starts to be read back (state “READ BACK”). When the whole memory has been read back the FPGA goes back into the “WAIT START CMD” state and wait for a new acquisition trigger command to happen. The following diagram describes the sequence of events during an acquisition:

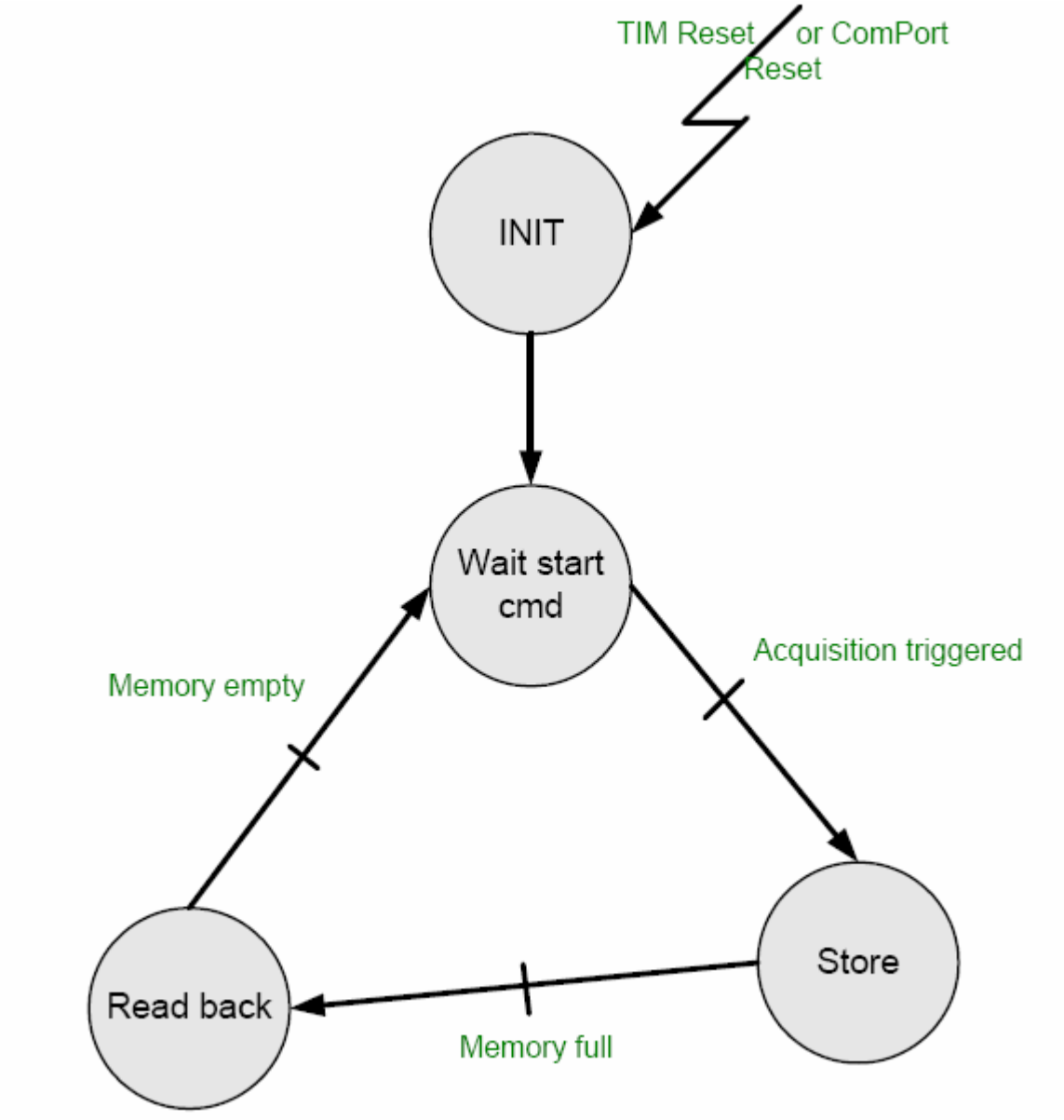



**Figure 22 – SMT391-VP Firmware State Diagram.**

## 4.2 Configuring the FPGA

The default for the FPGA configuration mode is using ComPort3. Configuring the FPGA from ComPort 3 makes it possible not to have to use a JTAG cable. Having a direct ComPort link enhances debugging and testing and therefore reduces the products time to market.

The configuration data can be downloaded into a DSP TIM module external memory (SMT6001) along with the DSP application, or configuration data can be sent from a PC application using a Sundance carrier with a DSP host (SMT6500).

The bitstream is presented on ComPort 3 and the microcontroller embedded on the SMT391-VP provides the mechanism to deliver it to the Virtex-II Pro device (configuration takes about 35 seconds and the process is similar to the configuration of the SMT398. For more into refer to the SMT398 User Manual).

After configuration the ComPort is available to the FPGA for data transfers.

## 4.3 Setting up an Acquisition

- Configure the FPGA over ComPort 3 like described above
- Initialize the SMT391-VP registers with the required values. See Control Register Settings section underneath for the description of these registers
- Start the acquisition: SMT391-VP is waiting for a trigger to start the Acquisition. This command can come either from the external trigger connectors, or from ComPort 3 (see acquisition trigger register section for more information).
- Once it receives a trigger command, the SMT391-VP will grab data coming from the daughter card module and store it into the DDR SDRAM memory.
- Once the memory has been filled up data can be read out over the SHB interface.

# 5 Control Register Settings

The Control Registers in the SMT391 example firmware control the complete functionality of the SMT391-VP. These Control Registers are setup via ComPort 3. The settings of the ADC, the trigger settings, the clock settings, the configuration of the SHB and RSL interfaces and the internal FPGA data path settings can be configured via the Control Registers.

## 5.1 Control Packet Structure

The data passed on to the SMT391 over the ComPorts must conform to a certain packet structure (for compatibility with example firmware). Only valid packets will be accepted and only after acceptance of a packet will the appropriate settings be implemented. Each packet will start with a certain command indicating a write (0x1) or a read (0x2). The address to write the data payload into (or where to read from) will follow next. After the address the data will follow.

A 32-bit packet is received on ComPort3 and decoded. A write command will write data into a register. A read command will request data from the FPGA. Once the data is collected it will be transmitted over ComPort3. When issuing a read command the return value must first be received before issuing the next read command.

All maximum size of registers that can be written to or read is 16 Bits. When performing a read bits 31 downto 16 will reflect the command and address. The lower 16 bits will contain the actual data.

This structure is illustrated in the following figure:

| | Byte Content | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Byte** | **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| **3** | Cmnd 3 | Cmnd 2 | Cmnd 1 | Cmnd 0 | Address 11 | Address 10 | Address 9 | Address 8 |
| **2** | Address 7 | Address 6 | Address 5 | Address 4 | Address 3 | Address 2 | Address 1 | Address 0 |
| **1** | Data 15 | Data 14 | Data 13 | Data 12 | Data 11 | Data 10 | Data 9 | Data 8 |
| **0** | Data 7 | Data 6 | Data 5 | Data 4 | Data 3 | Data 2 | Data 1 | Data 0 |

**Or**

| **31 .. 28** | **27 .. 24** | **23 .. 20** | **19 .. 16** | **15 .. 12** | **11 .. 8** | **7 .. 4** | **3 .. 0** |
|---|---|---|---|---|---|---|---|
| Command | Address | | | Data MSB | | Data LSB | |

**Figure 23 – Setup Packet Structure.**

The defined commands are:

| Command Value | Command Description |
|---|---|
| 0x0 | Reserved |
| 0x1 | FGPA Write |
| 0x2 | FPGA Read |
| 0x3 | Reserved |
| 0x4 | Reserved |
| 0x5 | Reserved |
| 0x6 | Reserved |
| 0x7 | Reserved |
| 0x8 | Reserved |
| 0x9 | Reserved |
| 0xA | Reserved |
| 0xB | Reserved |
| 0xC | Reserved |
| 0xD | Reserved |
| 0xE | Reserved |
| 0xF | FPGA Reset |

**Figure 24 – Packet Structure – Defined Commands.**

## 5.2 Reading and Writing Registers

Control packets are sent to the SMT391-VP over ComPort 3. This is a bi-directional interface and data can be sent to the SMT391-VP over ComPort 3 and also received over it. ComPort 3 is used to write control information to the SMT391-VP. Data is written by sending a ‘Write Packet’ (Command 0x1). Data is read by first writing a ‘Read Request’ (Command 0x2) packet containing the address to be read over ComPort 3. The SMT391-VP will collect the required data and send a ‘Read Packet’ out over ComPort 3 containing the requested data. The format of a ‘Read Packet’ is the same as that of a write packet. (For the example firmware ComPort 3 is the designated communications port on the SMT391-VP. This ComPort may however be connected to any ComPort on the Host.)

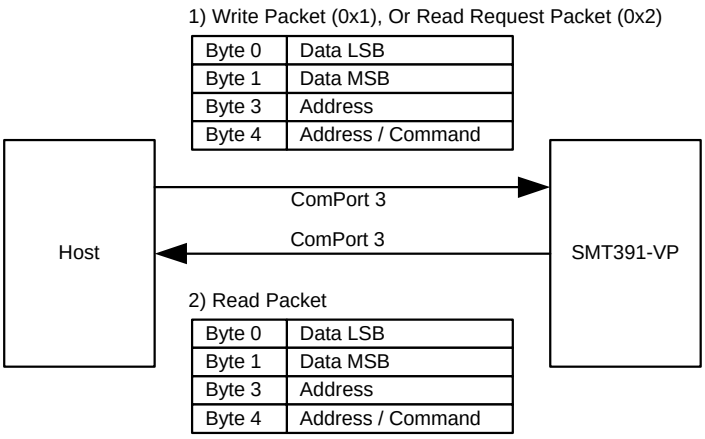



**Figure 25 – Control Register Read Sequence.**

Example 1:

Sending 0x1001FFFF over ComPort3 from the Host to the SMT391-VP will Write, to Address 0x001, Data FFFF

Example 2:

Sending 0x2801xxxx over ComPort3 from the Host to the SMT391-VP will request a Read, from Address 0x801. Once this command is received by the SMT391-VP, the requested data will automatically be transmitted back over ComPort 3, following the same packet structure.

## 5.3 Memory Map

The write packets must contain the address where the data must be written to and the read packets must contain the address where the required data must be read. The following figure shows the memory map for the writable and readable Control Registers on the SMT391-VP:

| Write Side | | | Read Side | |
|---|---|---|---|---|
| **Address** | **Register** | | **Address** | **Register** |
| 0x000 | Reserved | | 0x000 | FirmwareVersion |
| 0x001 | ComInScratchReg0 | | 0x001 | ComOutScratchReg0 |
| 0x002 | ComInScratchReg1 | | 0x002 | ComOutScratchReg1 |
| 0x003 | ShbACntrlReg | | 0x003 | ShbAStatusReg |
| 0x004 | ShbBCntrlReg | | 0x004 | ShbBStatusReg |
| 0x005 | ShbAComTestWordInLsb | | 0x005 | ShbAComTestWordOutLsb |
| 0x006 | ShbAComTestWordInMsb * | | 0x006 | ShbAComTestWordOutMsb |
| 0x007 | ShbBComTestWordInLsb | | 0x007 | ShbBComTestWordOutLsb |
| 0x008 | ShbBComTestWordInMsb * | | 0x008 | ShbBComTestWordOutMsb |
| 0x009 | Reserved | | 0x009 | Reserved |
| 0x00A | Reserved | | 0x00A | Reserved |
| 0x00B | Reserved | | 0x00B | Reserved |
| 0x00C | Reserved | | 0x00C | Reserved |
| 0x00D | Reserved | | 0x00D | Reserved |
| 0x00E | DdrACPCntrlReg | | 0x00E | DdrACPStatusReg |
| 0x00F | DdrBCPCntrlReg | | 0x00F | DdrBCPStatusReg |
| 0x010 | DdrACPCommand0In | | 0x010 | Reserved |
| 0x011 | DdrACPCommand1In | | 0x011 | Reserved |
| 0x012 | DdrACPCommand2In | | 0x012 | Reserved |
| 0x013 | DdrACPCommand3In * | | 0x013 | Reserved |
| 0x014 | DdrACPData0In | | 0x014 | DdrACPData0Out |
| 0x015 | DdrACPData1In | | 0x015 | DdrACPData1Out |
| 0x016 | DdrACPData2In | | 0x016 | DdrACPData2Out |
| 0x017 | DdrACPData3In * | | 0x017 | DdrACPData3Out + |
| 0x018 | DdrBCPCommand0In | | 0x018 | Reserved |
| 0x019 | DdrBCPCommand1In | | 0x019 | Reserved |
| 0x01A | DdrBCPCommand2In | | 0x01A | Reserved |
| 0x01B | DdrBCPCommand3In * | | 0x01B | Reserved |
| 0x01C | DdrBCPData0In | | 0x01C | DdrBCPData0Out |
| 0x01D | DdrBCPData1In | | 0x01D | DdrBCPData1Out |
| 0x01E | DdrBCPData2In | | 0x01E | DdrBCPData2Out |
| 0x01F | DdrBCPData3In * | | 0x01F | DdrBCPData3Out + |
| 0x020 | Reserved | | 0x020 | Smt338AirTempReg |
| 0x021 | Reserved | | 0x021 | Smt338DiodeTempReg |
| 0x022 | Reserved | | 0x022 | Smt338SerialNoA |
| 0x023 | Reserved | | 0x023 | Smt338SerialNoB |
| 0x024 | Reserved | | 0x024 | Smt338SerialNoC |

| | | | | |
|---|---|---|---|---|
| 0x025 | Reserved | | 0x025 | Smt338SerialNoD |
| 0x026 | Reserved | | 0x026 | Reserved |
| 0x027 | Reserved | | 0x027 | Reserved |
| 0x028 | Reserved | | 0x028 | DaughterCardAirTempReg |
| 0x029 | Reserved | | 0x029 | DaughterCardDiodeTempReg |
| 0x02A | Reserved | | 0x02A | DaughterCardSerialNoA |
| 0x02B | Reserved | | 0x02B | DaughterCardSerialNoB |
| 0x02C | Reserved | | 0x02C | DaughterCardSerialNoC |
| 0x02D | Reserved | | 0x02D | DaughterCardSerialNoD |
| 0x02E | Reserved | | 0x02E | Reserved |
| 0x02F | Reserved | | 0x02F | Reserved |
| 0x030 | AdcDataCaptureCntrl | | 0x030 | Reserved |
| 0x031 | Reserved | | 0x031 | AdcADataOut (Fifo, will auto Rd Next after a read) |
| 0x032 | Reserved | | 0x032 | AdcBDataOut (Fifo, will auto Rd Next after a read) |
| 0x033 | AdcResetReg | | 0x033 | Reserved |
| 0x034 | AdcModeReg | | 0x034 | Reserved |
| 0x035 | FifoResetReg | | 0x035 | Reserved |
| 0x036 | FifoEnableReg | | 0x036 | Reserved |
| | | | | |
| | **ADC Module Specific** | | | **ADC Module Specific** |
| 0x800 | Smt391AdjClkCntrlReg * | | 0x800 | Reserved |
| 0x801 | Smt391ClockSourceSelect | | 0x801 | Reserved |
| 0x802 | Smt391Pll_IfR_Reg1 | | 0x802 | Reserved |
| 0x803 | Smt391Pll_IfR_Reg2 | | 0x803 | Reserved |
| 0x804 | Smt391Pll_IfN_Reg1 | | 0x804 | Reserved |
| 0x805 | Smt391Pll_IfN_Reg2 | | 0x805 | Reserved |
| 0x806 | Smt391Pll_RfR_Reg1 | | 0x806 | Reserved |
| 0x807 | Smt391Pll_RfR_Reg2 | | 0x807 | Reserved |
| 0x808 | Smt391Pll_RfN_Reg1 | | 0x808 | Reserved |
| 0x809 | Smt391Pll_RfN_Reg2 * | | 0x809 | Reserved |
| 0x80A | Smt391AdcCntrlReg | | 0x80A | Reserved |
| 0x80B | Smt391AdcCntrlAddress | | 0x80B | Reserved |
| 0x80C | Smt391AdcCntrlData * | | 0x80C | Reserved |
| 0x80D | Reserved | | 0x80D | Reserved |
| 0x80E | Reserved | | 0x80E | Reserved |
| 0x80F | Reserved | | 0x80F | Reserved |

* Write Data Valid pulse is generated when this register is written to.

+ A pre-read is generated on the first read. A second read is required to read the real data.

**Figure 26 – Register Memory Map.**

For registers larger than 16 bits with an LSB and MSB part always write the LSB part first and then the MSB.

## 5.4 Register Descriptions

### 5.4.1 The Reset Register

As with normal register reading (command 0x2) and writing (command 0x1), there is a command defined for reset. This is command 0xF. The reset command will write to a reset register. Writing 0x0001 to it will keep the FPGA in reset, and writing 0x0000 to it will take the FPGA out of reset. This register is at address 0x000.

| 31 .. 28 | 27 .. 24 | 23 .. 20 | 19 .. 16 | 15 .. 12 | 11 .. 8 | 7 .. 4 | 3 .. 0 |
|---|---|---|---|---|---|---|---|
| **Command** | **Address** | | | **Data MSB** | | **Data LSB** | |
| 0xF | 0x000 | | | 0x00 | | 0x00 – Not in Reset | |
| 0xF | 0x000 | | | 0x00 | | 0x01 – FPGA in Reset | |

**Figure 27 – Reset Register (Write Only).**

### 5.4.2 Firmware Version Register (Read Add 0x000)

A read from address 0x000 will display the firmware version register. The value of this register is hard coded during VHDL compiles and must be stepped for each new version of the firmware. Even though 32 bits are read over the ComPort, the firmware version register is a 16 bit register (16 least significant bits of the returned value).

Read Request Format:

| 31 .. 28 | 27 .. 24 | 23 .. 20 | 19 .. 16 | 15 .. 12 | 11 .. 8 | 7 .. 4 | 3 .. 0 |
|---|---|---|---|---|---|---|---|
| **Command** | **Address** | | | **Data MSB** | | **Data LSB** | |
| 0x2 | 0x000 | | | xx | | xx | |

Read Response Format:

| 31 .. 28 | 27 .. 24 | 23 .. 20 | 19 .. 16 | 15 .. 12 | 11 .. 8 | 7 .. 4 | 3 .. 0 |
|---|---|---|---|---|---|---|---|
| **Command** | **Address** | | | **Data MSB** | | **Data LSB** | |
| 0x2 | 0x000 | | | Firmware Version | | Firmware Version | |

**Figure 28 – Firmware Version Register (Read Only).**

### 5.4.3 Temperature Registers (Read Add 0x020, 0x021, 0x028, 0x029)

There are four temperature registers. Each register is 16 bits long. When the bit value of the register is converted to a decimal number, that number is the temperature in degrees Celsius.

Read Request Format:

| 31 .. 28 | 27 .. 24 | 23 .. 20 | 19 .. 16 | 15 .. 12 | 11 .. 8 | 7 .. 4 | 3 .. 0 |
|---|---|---|---|---|---|---|---|
| **Command** | **Address** | | | **Data MSB** | | **Data LSB** | |
| 0x2 | 0x020 (Smt338AirTempReg) (1) | | | xx | | xx | |
| 0x2 | 0x021 (Smt338DiodeTempReg) (2) | | | xx | | xx | |
| 0x2 | 0x028 (DaughterCardAirTempReg) (3) | | | xx | | xx | |
| 0x2 | 0x029 (DaughterCardDiodeTempReg) (4) | | | xx | | xx | |

(1) - SMT338-VP Air Temperature on Top of PCB

(2) – SMT338-VP FPGA temperature on Bottom of PCB

(3) – SMT391 Air Temperature on Bottom of PCB

(4) – SMT391 ADC temperature on Top of PCB (Not implemented)

Read Response Format:

| 31 .. 28 | 27 .. 24 | 23 .. 20 | 19 .. 16 | 15 .. 12 | 11 .. 8 | 7 .. 4 | 3 .. 0 |
|---|---|---|---|---|---|---|---|
| **Command** | **Address** | | | **Data MSB** | | **Data LSB** | |
| 0x2 | 0x020 | | | SMT338-VP | | Air Temperature | |
| 0x2 | 0x021 | | | SMT338-VP | | Diode Temperature | |
| 0x2 | 0x028 | | | SMT391 | | Air Temperature | |
| 0x2 | 0x029 | | | SMT391 | | Diode Temperature | |

**Figure 29 – Temperature Registers (Read Only).**

### 5.4.4 Serial Number Registers (Read Add 0x022 - 0x025 and 0x02A - 0x02D)

There is a unique silicon serial number IC on both the SMT338-VP and the SMT391. Each serial number is 64 bits long and is thus requires four 16 bit registers to store the value.

Read Request Format:

| 31 .. 28 | 27 .. 24 | 23 .. 20 | 19 .. 16 | 15 .. 12 | 11 .. 8 | 7 .. 4 | 3 .. 0 |
|---|---|---|---|---|---|---|---|
| **Command** | **Address** | | | **Data MSB** | | **Data LSB** | |
| 0x2 | 0x022 (Smt338SerialNoA) | | | xx | | xx | |
| 0x2 | 0x023 (Smt338SerialNoB) | | | xx | | xx | |
| 0x2 | 0x024 (Smt338SerialNoC) | | | xx | | xx | |
| 0x2 | 0x025 (Smt338SerialNoD) | | | xx | | xx | |
| 0x2 | 0x02A (DaughterCardSerialNoA) | | | xx | | xx | |
| 0x2 | 0x02B (DaughterCardSerialNoB) | | | xx | | xx | |
| 0x2 | 0x02C (DaughterCardSerialNoC) | | | xx | | xx | |
| 0x2 | 0x02D (DaughterCardSerialNoD) | | | xx | | xx | |

**Figure 30 – Serial Number Registers (Read Only).**

Read Response Format:

| 31 .. 28 | 27 .. 24 | 23 .. 20 | 19 .. 16 | 15 .. 12 | 11 .. 8 | 7 .. 4 | 3 .. 0 |
|---|---|---|---|---|---|---|---|
| **Command** | **Address** | | | **Data MSB** | | **Data LSB** | |
| 0x2 | 0x022 | | | SMT338-VP Serial No | | Byte A | |
| 0x2 | 0x023 | | | SMT338-VP Serial No | | Byte B | |
| 0x2 | 0x024 | | | SMT338-VP Serial No | | Byte C | |
| 0x2 | 0x025 | | | SMT338-VP Serial No | | Byte D | |
| 0x2 | 0x02A | | | SMT391 Serial No | | Byte A | |
| 0x2 | 0x02B | | | SMT391 Serial No | | Byte B | |
| 0x2 | 0x02C | | | SMT391 Serial No | | Byte C | |
| 0x2 | 0x02D | | | SMT391 Serial No | | Byte D | |

**Figure 31 – Serial Number Registers Cont. (Read Only).**

### 5.4.5 ADC Clock Source Registers (Write Add 0x801)

The I and Q channels of the ADC can receive a clock from the on-board VCO, the on-board clock synthesizer, or from an external clock (there are two external clock inputs, one for each channel). The following table shows the different combinations for setting up the SMT391 clock tree.

| Register Value | I Channel Clock Source | Q Channel Clock Source |
|---|---|---|
| 0x0000 | On-board VCO | On-board VCO |
| 0x0001 | On-board Clock Synthesizer | On-board Clock Synthesizer |
| 0x0002 | External I Channel Clock | On-board VCO |
| 0x0003 | External I Channel Clock | On-board Clock Synthesizer |
| 0x0004 | On-board VCO | External Q Channel Clock |
| 0x0005 | On-board Clock Synthesizer | External Q Channel Clock |
| 0x0006 | External I Channel Clock | External Q Channel Clock |

**Figure 32 – Clock Source Selection Table (Write Only).**

| 31 .. 28 | 27 .. 24 | 23 .. 20 | 19 .. 16 | 15 .. 12 | 11 .. 8 | 7 .. 4 | 3 .. 0 |
|---|---|---|---|---|---|---|---|
| **Command** | **Address** | | | **Data MSB** | | **Data LSB** | |
| 0x1 | 0x801 | | | 0x00 | | Clock Register Value | |

**Figure 33 – Clock Source Register (Write Only).**

### 5.4.6 Clock Synthesizer Setup Register (Write Add 0x800)

This register sets up the frequency of the clock synthesizer on the SMT391. Any write operation to this register will trigger the clock synthesizer interface control logic to initialize the clock synthesizer with its new value.

| 31 .. 28 | 27 .. 24 | 23 .. 20 | 19 .. 16 | 15 .. 12 | 11 .. 8 | 7 .. 4 | 3 .. 0 |
|---|---|---|---|---|---|---|---|
| **Command** | **Address** | | | **Data MSB** | | **Data LSB** | |
| 0x1 | 0x800 | | | Data | | Data | |

**Figure 34 – Clock Synthesizer Setup Register (Write Only).**

For a detailed description of the configurable bits in the Clock Synthesizer register please refer to the “Clock Synthesizer” section under “Firmware Building Blocks” at the end of this document.

### 5.4.7 PLL Setup Registers (Write Add 0x802 – 0x809)

These registers set up the frequency of the PLL circuit on the SMT391. There are two sets of registers – one set for setting up the IF side of the PLL, and the other set for setting up the RF side of the PLL. The IF side is connected to a 200 – 350 MHz VCO circuit and the RF side is connected to a 600 – 1000 MHz VCO circuit. All registers must be initialized, and only when writing to the final register will both the IF and RF side be configured to their new values.

| 31 .. 28 | 27 .. 24 | 23 .. 20 | 19 .. 16 | 15 .. 12 | 11 .. 8 | 7 .. 4 | 3 .. 0 |
|---|---|---|---|---|---|---|---|
| **Command** | **Address** | | | **Data MSB** | | **Data LSB** | |
| 0x1 | 0x802 | | | Smt391Pll_IfR_Reg1 | | Smt391Pll_IfR_Reg1 | |
| 0x1 | 0x803 | | | Smt391Pll_IfR_Reg2 | | Smt391Pll_IfR_Reg2 | |
| 0x1 | 0x804 | | | Smt391Pll_IfN_Reg1 | | Smt391Pll_IfN_Reg1 | |
| 0x1 | 0x805 | | | Smt391Pll_IfN_Reg2 | | Smt391Pll_IfN_Reg2 | |
| 0x1 | 0x806 | | | Smt391Pll_RfR_Reg1 | | Smt391Pll_RfR_Reg1 | |
| 0x1 | 0x807 | | | Smt391Pll_RfR_Reg2 | | Smt391Pll_RfR_Reg2 | |
| 0x1 | 0x808 | | | Smt391Pll_RfN_Reg1 | | Smt391Pll_RfN_Reg1 | |
| 0x1 | 0x809 | | | Smt391Pll_RfN_Reg2 | | Smt391Pll_RfN_Reg2 | |

**Figure 35 – PLL Setup Registers (Write Only).**

For a detailed description of the configurable bits in the PLL registers please refer to the “PLL Configuration” section under “Firmware Building Blocks” at the end of this document.

### 5.4.8 ADC Setup Registers (Write Add 0x80B, 0x80C)

These registers configure the internal functionality of the ADC on the SMT391. There are two registers – a data register and an address register. The address register must be set up before the data register. Once the data register is written to the data and address information contained in the two registers will be transferred to the ADC over a serial interface.

| 31 .. 28 | 27 .. 24 | 23 .. 20 | 19 .. 16 | 15 .. 12 | 11 .. 8 | 7 .. 4 | 3 .. 0 |
|---|---|---|---|---|---|---|---|
| **Command** | **Address** | | | **Data MSB** | | **Data LSB** | |
| 0x1 | 0x80B | | | Smt391AdcCntrlAddress | | Smt391AdcCntrlAddress | |
| 0x1 | 0x803 | | | Smt391AdcCntrlData | | Smt391AdcCntrlData | |

**Figure 36 – ADC Setup Registers (Write Only).**

For a detailed description of the configurable bits in the ADC registers please refer to the “ADC Configuration” section under “Firmware Building Blocks” at the end of this document.

# 6 PCB Layout

## 6.1 SMT391 PCB View

The following figures show the top and bottom view of the daughter card (SMT391).

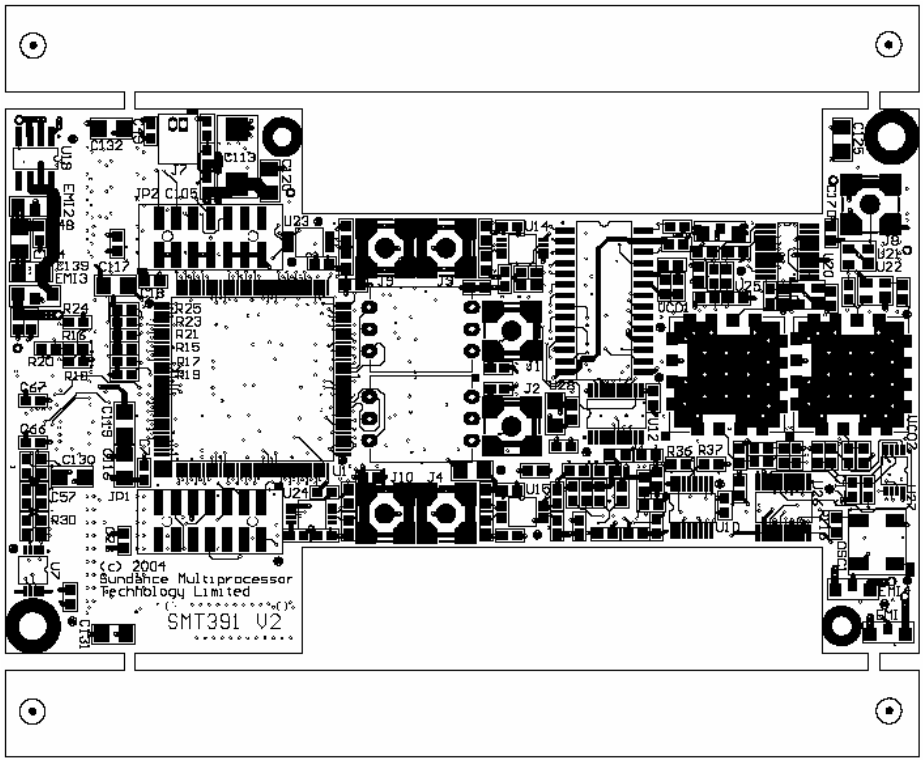



**Figure 37 – Daughter-card Top View.**

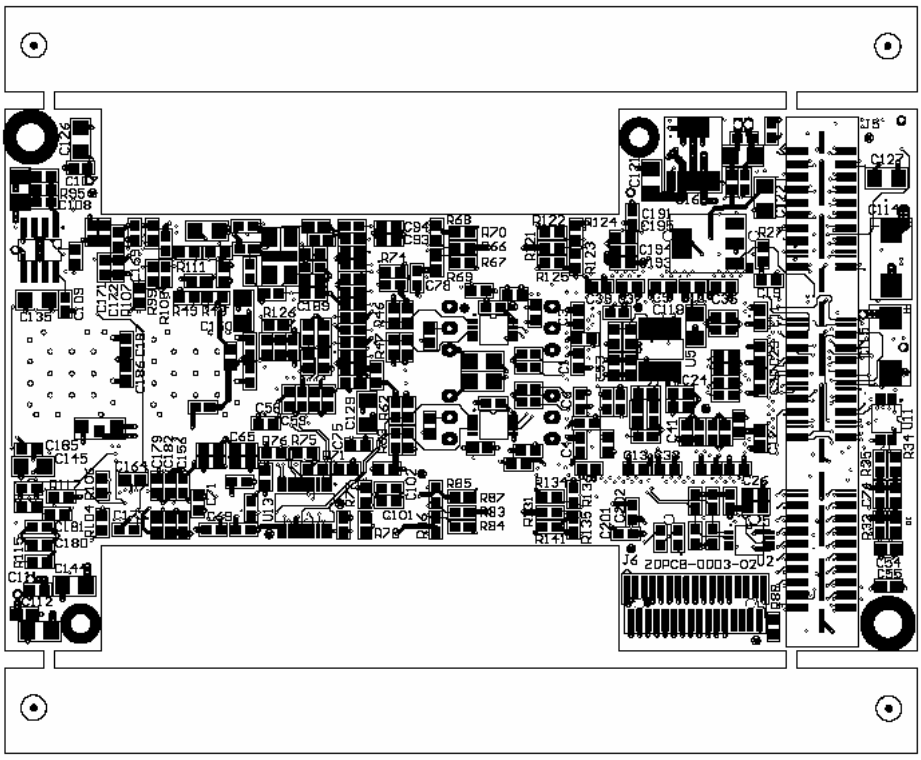



**Figure 38 – Daughter-card Bottom View.**

## 6.2 SMT391 Assembly Drawings

The following figures show the top and bottom assembly drawings of the SMT391.

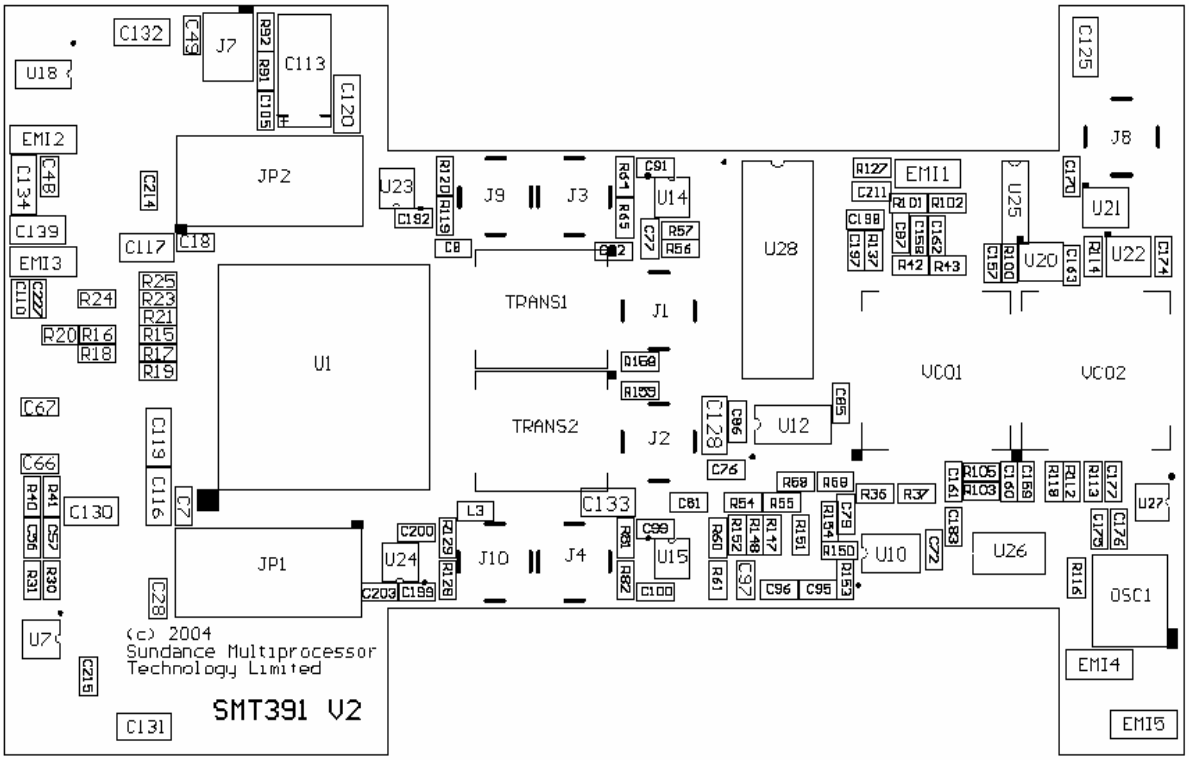



**Figure 39 – Daughter-card Top Assembly Drawing.**

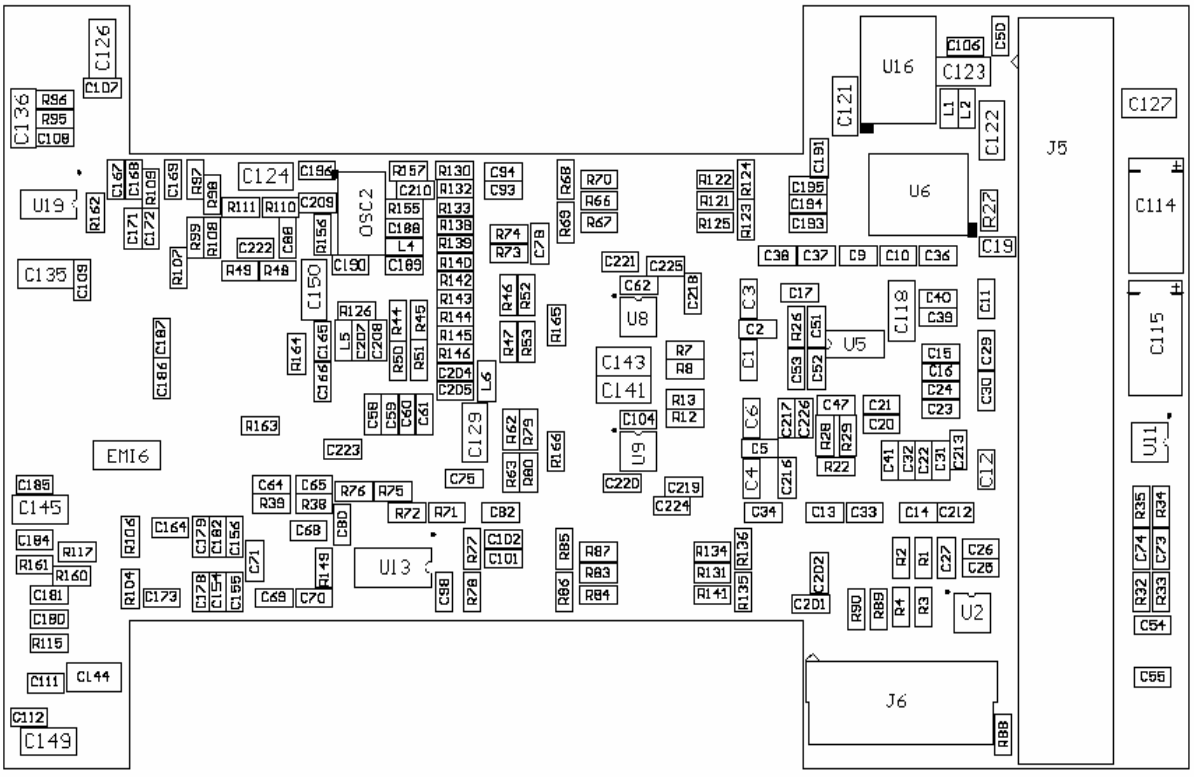



**Figure 40 – Daughter-card Bottom Assembly Drawing.**

## 6.3 SMT338-VP Assembly Drawings

The following figures show the top and bottom assembly drawings of the SMT338-VP.

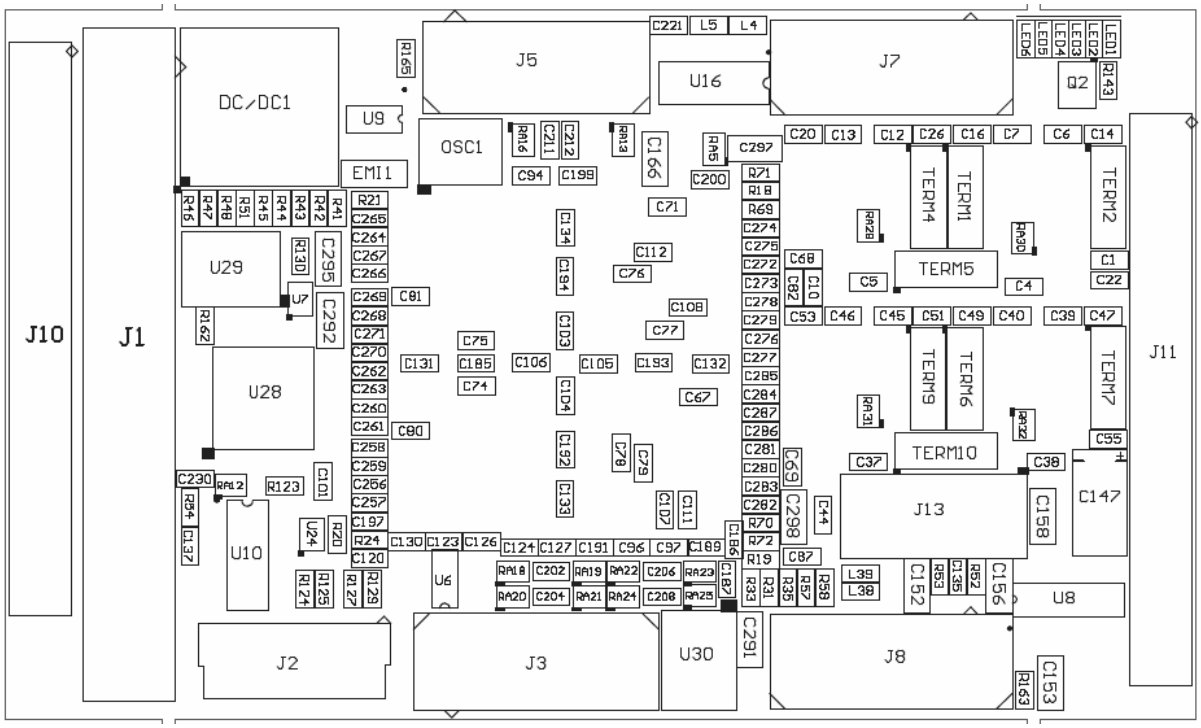



**Figure 41 – Main Module Top Assembly Drawing.**

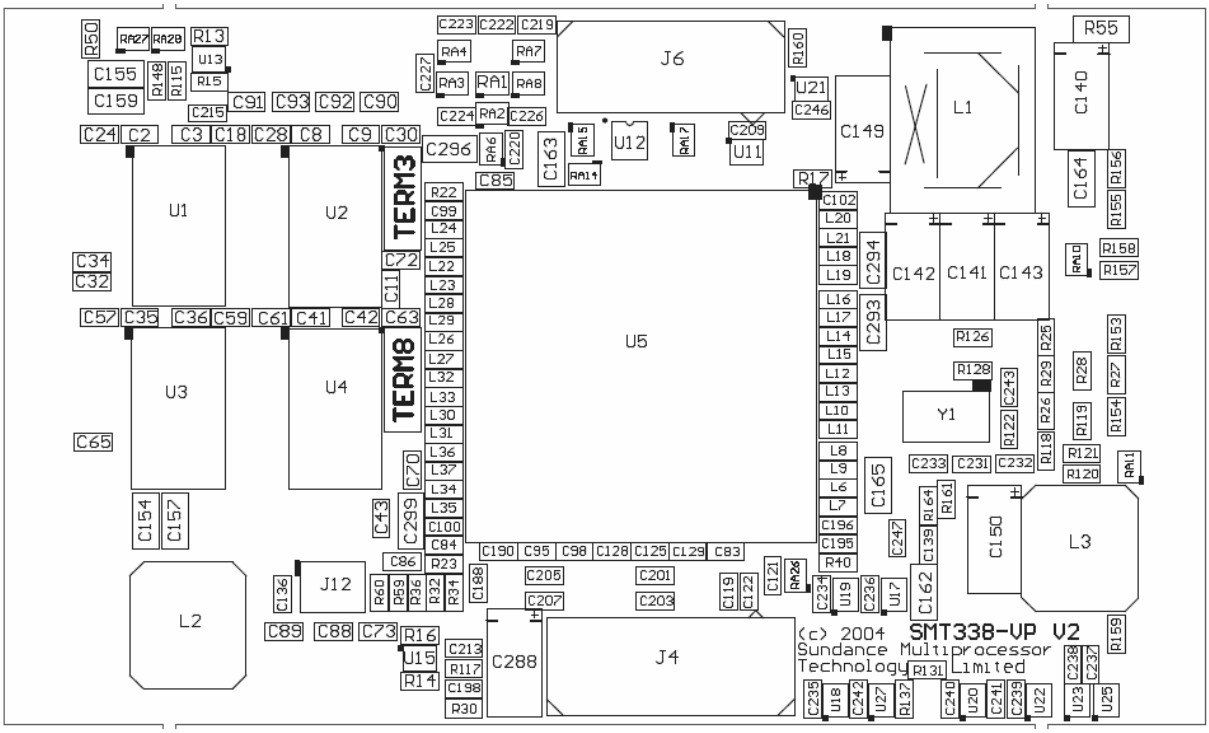



**Figure 42 – Main Module Bottom Assembly Drawing.**

## 6.4 SMT391 PCB View

If the SMT391-VP is mated with a PCI carrier two PCI slots will be required for the Module + Carrier combination. If the SMT391-VP is mated with a cPCI carrier the Module + Carrier will require two cPCI slots.

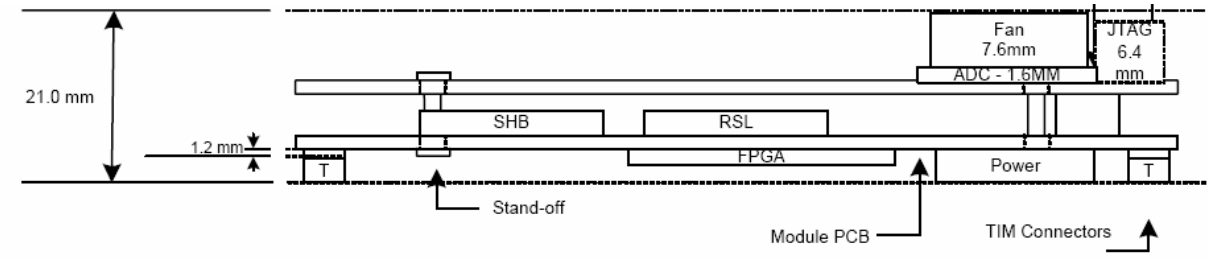



**Figure 43 – Side view of SMT391-VP (Height).**

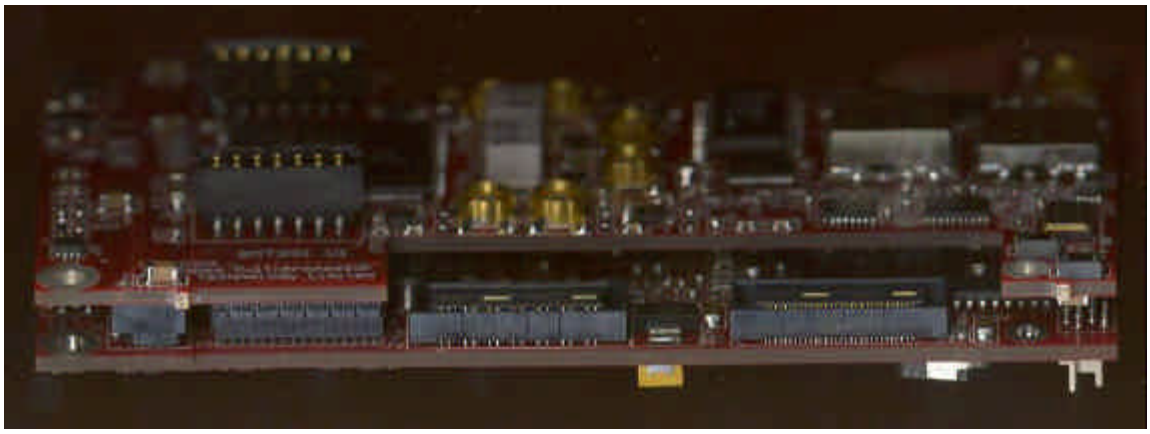


**Figure 44 – Side view of SMT391-VP (No Heat Sinks, Rev1 PCB).**

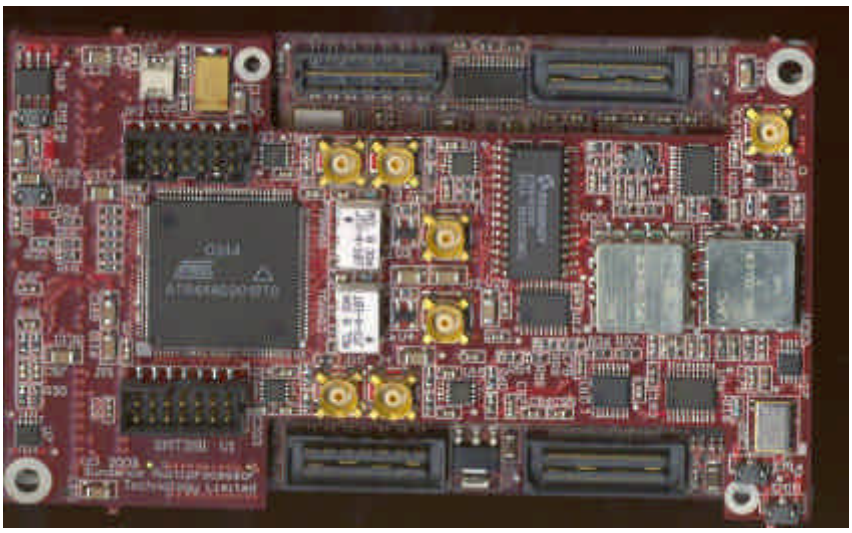


**Figure 45 – Top view of SMT391-VP (No Heat Sinks, Rev1 PCB).**

The following diagram indicates the location of all the important connectors and components on the SMT391 (Rev 2) PCB. This specific diagram is for an AC coupled analog input stage using a Macom transformer. It is also possible to order the module with a different input stage for DC coupled applications.

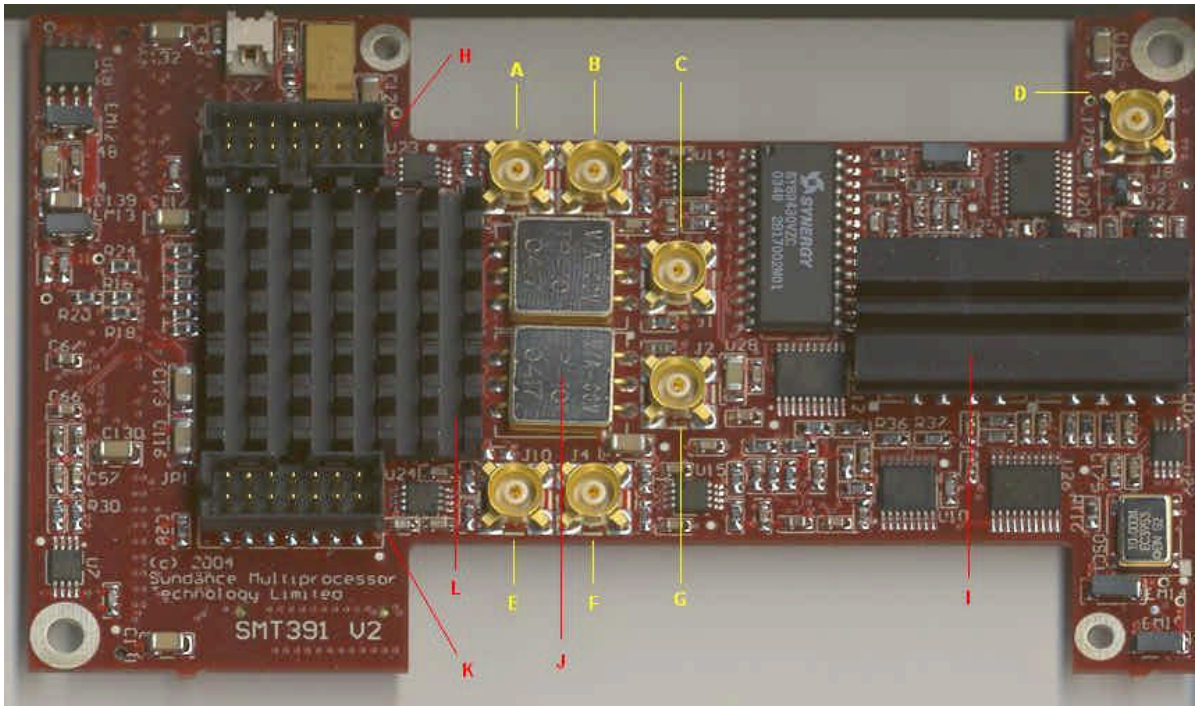



**Figure 46 – Connector Location on SMT391 (Rev 2 PCB, AC Coupled).**

| Diagram Ref | Pcb RefDes | Description | Notes |
|---|---|---|---|
| A | J9 | External Trigger I Channel | LVPECL Signal. Positive on inside of connector. Negative on outside of connector. |
| E | J10 | External Trigger Q Channel | LVPECL Signal. Positive on inside of connector. Negative on outside of connector. |
| B | J3 | External Clock I Channel | LVPECL Signal. Positive on inside of connector. Negative on outside of connector. |
| F | J4 | External Clock Q Channel | LVPECL Signal. Positive on inside of connector. Negative on outside of connector. |
| C | J1 | ADC I Channel Input | Analog signal input for ADC Channel I. Signal on inside of connector. Analog ground on outside of connector. |
| G | J2 | ADC Q Channel Input | Analog signal input for ADC Channel Q. Signal on inside of connector. Analog ground on outside of connector. |
| H | J8 | Analog Test Signal | Analog output test signal. Variable between 200 and 350MHz. Signal on inside of connector, Analog ground on outside of connector. Use a 1:1 RF cable to connect J8 to either J1 or J2 for easy verification of the working of the ADC. |

**Figure 47 – Table of Connector Locations on SMT391.**

| Diagram Ref | Pcb RefDes | Description | Notes |
|---|---|---|---|
| H | JP2 | FPGA JTAG Connector | FPGA on SMT338-VP JTAG Chain. Only routed down to SMT338-VP. Use for easy access without having to remove the SMT391. |
| K | JP1 | MSP JTAG Connector | MSP430 on SMT338-VP JTAG Chain. Only routed down to SMT338-VP. Use for easy access without having to remove the SMT391. |
| L | U1 | Atmel Dual ADC | ADC Requires heat-sink with air-flow cooling in a system setup |
| I | VCO1 | UMC 600 – 1000MHz VCO | Main Clock source for SMT391. VCO Requires heat-sink with air-flow cooling in a system setup. |
| I | VCO2 | UMC 200 – 350MHz VCO | Test Clock for testing the analog input of the ADC. VCO Requires heat-sink with air-flow cooling in a system setup. |
| J | TRANS1 | M/A Com TP101 Transformer | By default the SMT391 analog input is AC coupled through a twisted pair balum transformer (single ended to differential). It is possible to order the SMT391 with a DC coupled input using a 1:1 balum transformer (circuit also wired as single ended input on connector side to differential input on ADC side). Refer to section 2.11 for more details. |
| J | TRANS2 | M/A Com TP101 Transformer | By default the SMT391 analog input is AC coupled through a twisted pair balum transformer (single ended to differential). It is possible to order the SMT391 with a DC coupled input using a 1:1 balum transformer (circuit also wired as single ended input on connector side to differential input on ADC side). Refer to section 2.11 for more details. |

**Figure 48 – Table of Component Locations on SMT391.**

# 7 General Properties

## 7.1 FPGA Mounted on SMT338-VP

All FPGA interfaces on the SMT338-VP require 508 IOs. The following table is a summary of the amount of IOs available on Xilinx Virtex-II Pro devices.

| | Size (mm) | XC2VP7 | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
|---|---|---|---|---|---|---|
| **FF672** | 27 x 27 | 396 / 8 | | | | |
| **FF896** | 31 x 31 | 396 / 8 | **556 / 8** | **556 / 8** | | |
| **FF1152** | 35 x 35 | | 564 / 8 | 644 / 8 | 692 / 12 | 692 / 16 |

**Figure 49 – Virtex-II Pro IO Count.**

By default all SMT338-VPs are assembled with VP30 devices. The example firmware is also for a VP30 FPGA. If a VP7 is mounted some of the SHB interface IOs and the DDR SDRAM memory interface will be lost.

## 7.2 Design Resource Usage

The following table is a summary of the FPGA resources used by the demo design that comes with the SMT391-VP (compiled for a VP30 device).

| Resource | Utilization | Percentage |
|---|---|---|
| Number of External DIFFMs | 37 out of 276 | 13% |
| Number of External DIFFSs | 37 out of 276 | 13% |
| Number of External IOBs | 266 out of 556 | 47% |
| Number of LOCed External IOBs | 249 out of 266 | 93% |
| | | |
| Number of RAMB16s | 72 out of 136 | 52% |
| Number of SLICEs | 6640 out of 13696 | 48% |
| | | |
| Number of BUFGMUXs | 13 out of 16 | 81% |
| Number of DCMs | 7 out of 8 | 87% |

**Figure 50 – Virtex-II Pro Device Utilization Summary.**

## 7.3 Power Supply

The following voltages are required by the SMT391 and must be supplied over the daughter card power connector.

| Voltage | Current Required |
|---|---|
| D+3V3_IN | 2.0 A |
| D+5V0_IN | 500 mA |
| D+12V0_IN | 250 mA |
| D-12V0_IN | 250 mA |
| DGND | |

**Figure 51 – SMT391 Power Supply Voltages.**

The following voltages are required by the SMT391-VP and must be supplied over the TIM connectors and TIM mounting hole

| Voltage | Current Required |
|---|---|
| D+3V3_IN | 4.0 – 6.0 A |
| D+5V0_IN | 4.0 A |
| D+12V0_IN | 500 mA |
| D-12V0_IN | 500 mA |
| DGND | |

**Figure 52 – SMT391-VP Power Supply Voltages.**

The following table lists the internal SMT391 voltages that are derived from the voltages that are provided over the daughter card power connector.

| Voltage | Description |
|---|---|
| D+3V3 | Derived from D+3V3_IN |
| D+2V25 | Derived from D+3V3 on SMT391 |
| A+3V3 | Derived from D+3V3_IN |
| VCO+5V0 | Derived from D+5V0_IN |
| VCO+12V0 | Derived from D+12V0_IN |
| ECL-5V2 | Derived from D-12V0_IN |
| AGND | Derived from DGND |

**Figure 53 – Internal Power Supply Voltages.**

## 7.4 Module Dimensions

The following table lists the dimensions for the SMT391 and the SMT391-VP.

| Description | Value |
|---|---|
| Module Dimensions (Only SMT391) | Width: 63.5 mm<br>Length: 106.68 mm<br>Height: 21mm (Maximum) |
| Module Dimensions (SMT391-VP) | Width: 63.5 mm<br>Length: 106.68 mm<br>Height: 21mm (Maximum) |
| Weight | TBD Grams (including heat sinks) |

**Figure 54 – SMT391-VP Dimensions.**

## 7.5 FPGA JTAG Connector

The following table describes the pin assignments of the FPGA JTAG chain routing through the SMT391 through the daughter card interface connector to the SMT338-VP

| SMT391-VP Side – Connector JP2<br>2mm IDC Type Connector | | | Xilinx Parallel cable IV<br>2mm IDC Type Connector | |
|---|---|---|---|---|
| Pin | Signal Description | | Pin | Signal Description |
| 1 | DGND | | 1 | DGND |
| 2 | FPGA VREF | | 2 | FPGA VREF |
| 3 | DGND | | 3 | DGND |
| 4 | FPGA TMS | | 4 | FPGA TMS |
| 5 | DGND | | 5 | DGND |
| 6 | FPGA TCK | | 6 | FPGA TCK |
| 7 | DGND | | 7 | DGND |
| 8 | FPGA TDO | | 8 | FPGA TDO |
| 9 | DGND | | 9 | DGND |
| 10 | FPGA TDI | | 10 | FPGA TDI |
| 11 | DGND | | 11 | DGND |
| 12 | Not Used | | 12 | Not Used |
| 13 | DGND | | 13 | DGND |
| 14 | Not Used | | 14 | Not Used |

**Figure 55 – FPGA JTAG Cable Connection.**

## 7.6 MSP430 JTAG Connector

The following table describes the pin assignments of the MSP430 microprocessor JTAG chain routing through the SMT391 through the daughter card interface connector to the SMT338-VP

| SMT391-VP Side – Connector JP1<br>2mm IDC Type Connector | | | MSP430 JTAG Emulator<br>2.54mm IDC Type Connector | |
|---|---|---|---|---|
| **Pin** | **Signal Description** | | **Pin** | **Signal Description** |
| 1 | MSP430 TDO | | 1 | MSP430 TDO |
| 2 | Not Used | | 2 | Not Used |
| 3 | MSP430 TDI | | 3 | MSP430 TDI |
| 4 | Not Used | | 4 | Not Used |
| 5 | MSP430 TMS | | 5 | MSP430 TMS |
| 6 | Not Used | | 6 | Not Used |
| 7 | MSP430 TCK | | 7 | MSP430 TCK |
| 8 | MSP430 Test / Vpp | | 8 | MSP430 Test / Vpp |
| 9 | DGND | | 9 | DGND |
| 10 | Not Used | | 10 | Not Used |
| 11 | MSP430 nTRST | | 11 | MSP430 nTRST |
| 12 | Not Used | | 12 | Not Used |
| 13 | Not Used | | 13 | Not Used |
| 14 | Not Used | | 14 | Not Used |

**Figure 56 – MSP430 JTAG Cable Connection.**

# 8 System Setup

## 8.1 How to connect the SMT391 and SMT338-VP

The following diagram shows both the SMT338-VP and the SMT391 (together they form the SMT391-VP). There are four mounting holes on each board. The two larger holes on the SMT338-VP are the TIM mounting holes and provide the SMT338-VP with 3.3V. The two smaller holes add extra stability when the SMT391 is plugged onto the SMT338-VP (One of these holes on the SMT338-VP carries 1.5V and the other one 2.5V. These voltages are however not used on the SMT391-VP. For this reason it is thus safer to use Nylon screws).

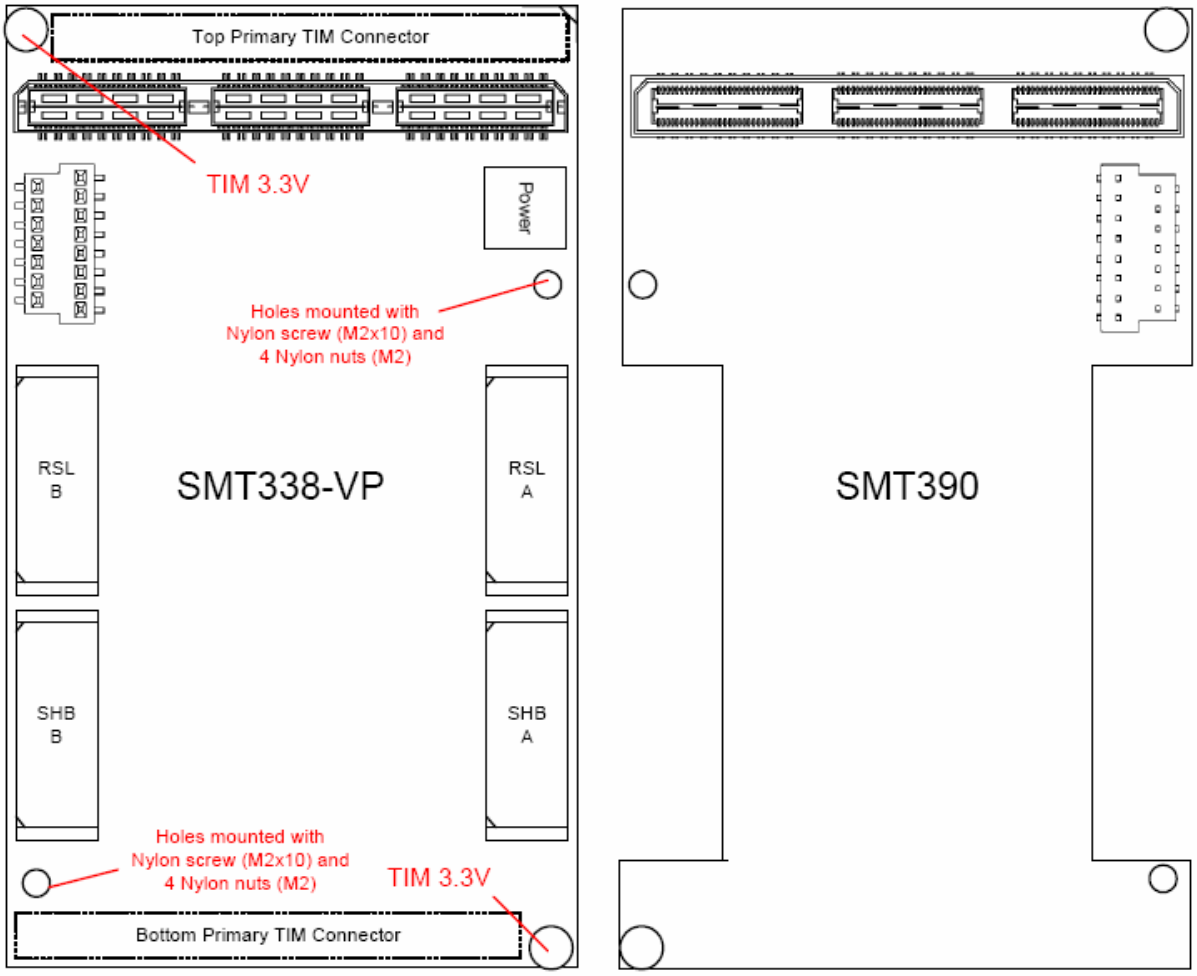



**Figure 57 – SMT391 to SMT338-VP Interconnection.**

The following fixings are required to connect the SMT391 to the SMT338-VP:

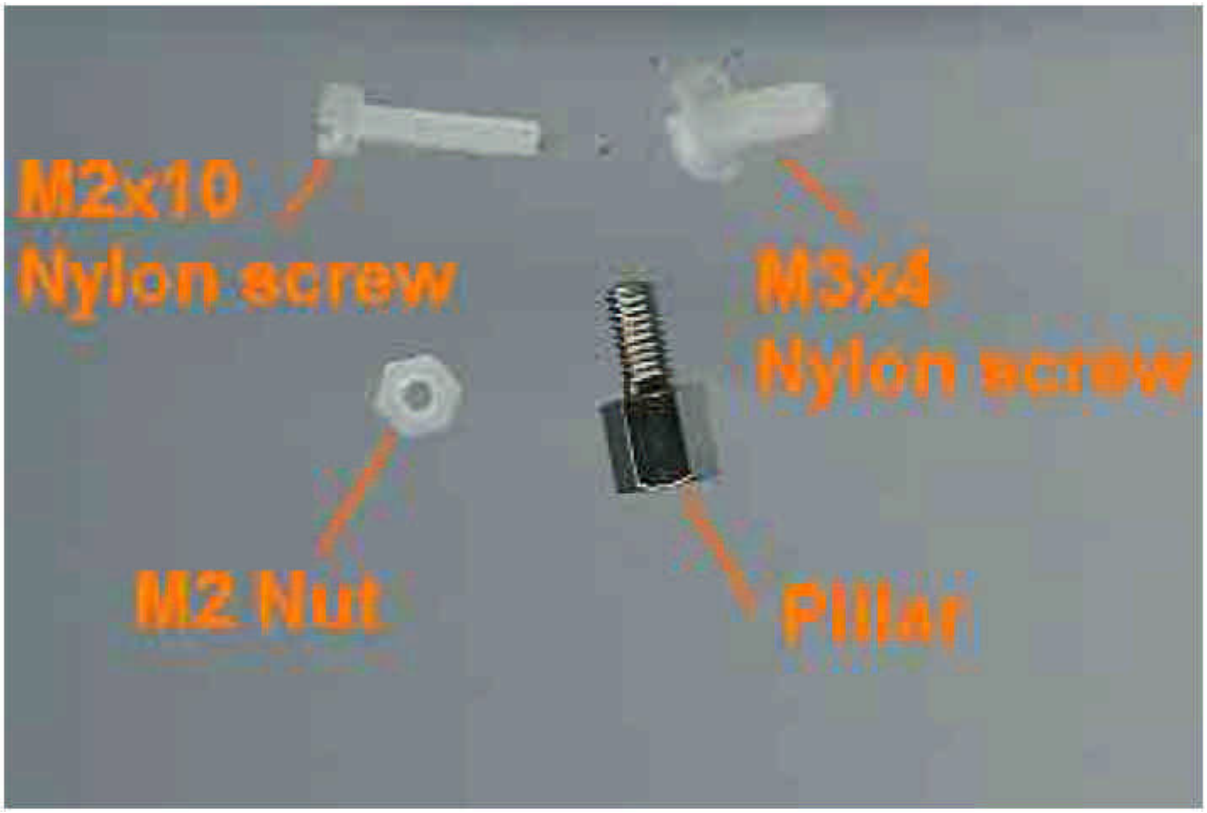



**Figure 58 – Components Used to Connect the SMT391 to the SMT338-VP.**

1) First fit two Nylon screws (M2 x 10), pointing out (the head of the screws on the bottom side of the SMT338-VP).
2) Then fit four M2 nuts on each screw.
3) Place the SMT338-VP on the second TIM site (TIM 1 is for the Host) of a Sundance carrier (like the SMT310Q)
4) Fit the two metal pillars to the TIM mounting holes to give the SMT338-VP 3.3V from the carrier.
5) Place the SMT391-VP on top of the SMT338-VP and make sure that both modules fit firmly (the SMT391 does not need 3.3V of it's mounting hole).
6) Fit two M2 nuts on the Nylon screws and two M3x4 screws in the 3.3V pillars.
7) Connect ComPort3 of the SMT391-VP to an available ComPort on the Host module (eg ComPort 0).

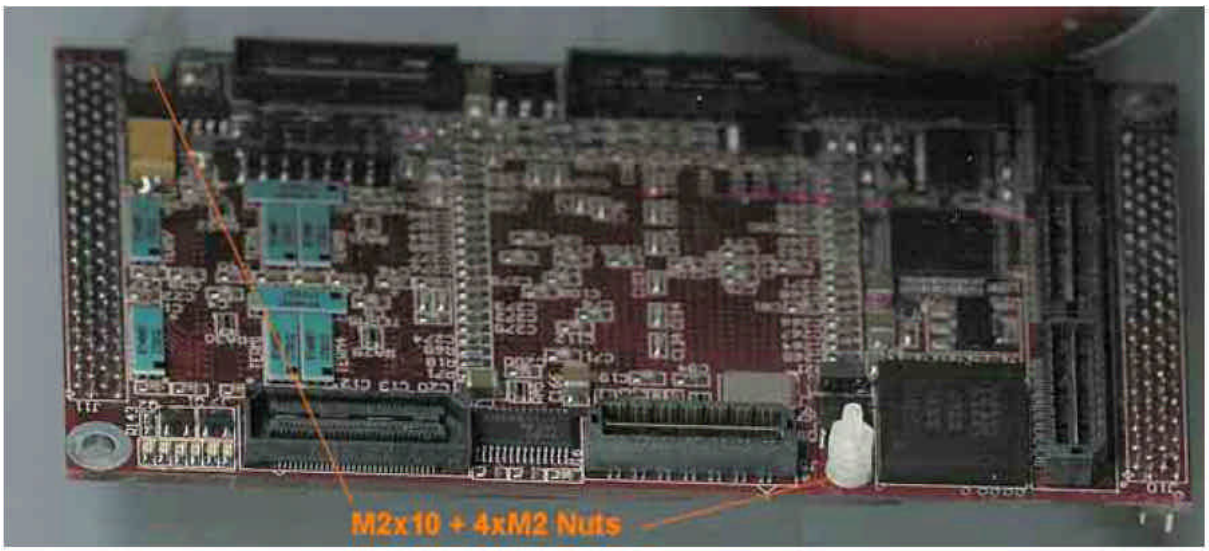



**Figure 59 – Fitting of Nylon Screws and Nuts to the SMT338-VP.**

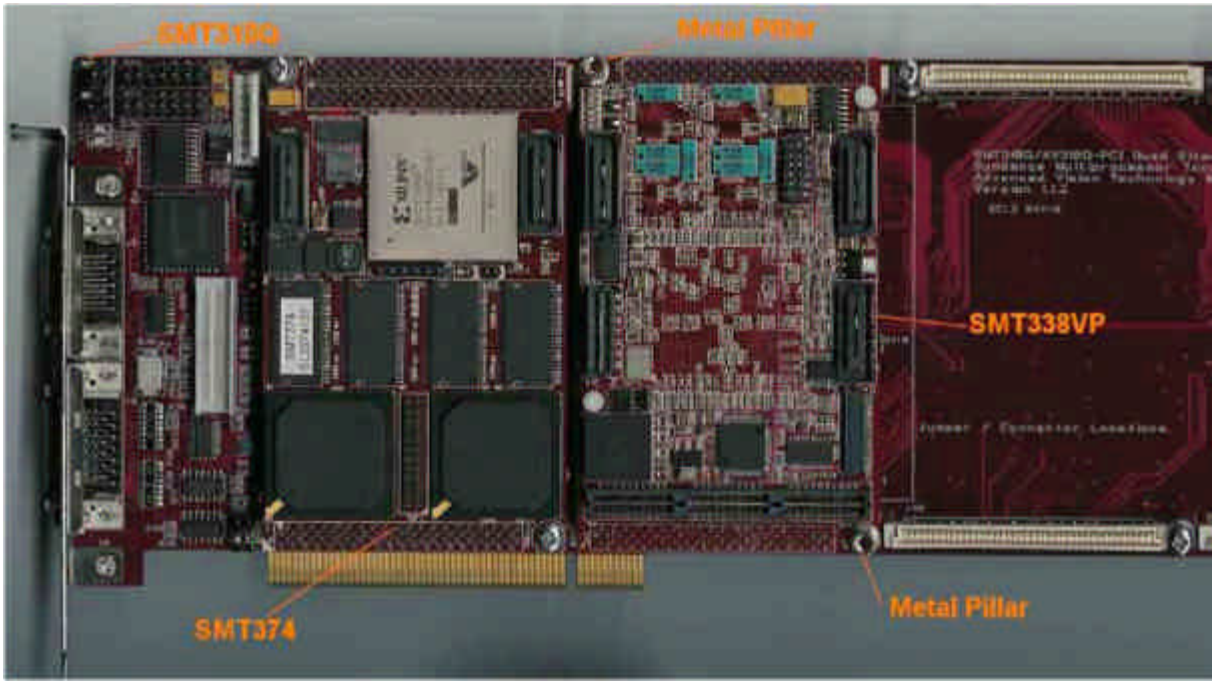



**Figure 60 – Securing the SMT338-VP onto a Sundance Carrier.**

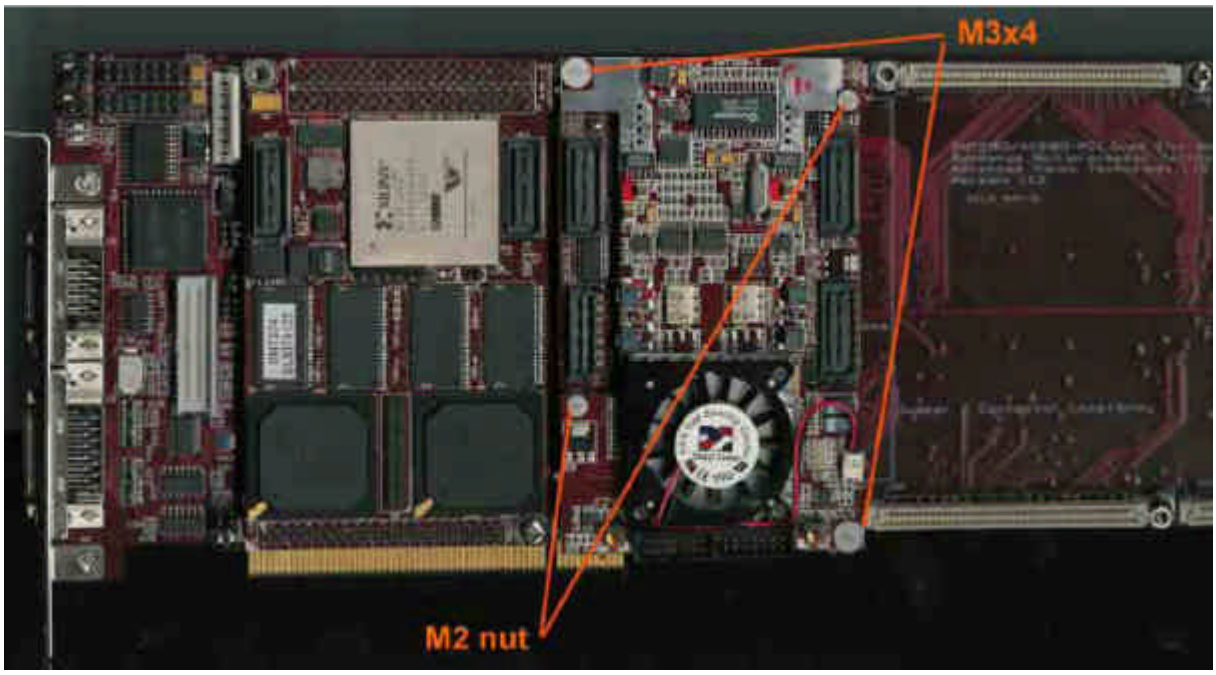



**Figure 61 – Connecting the SMT391 to the SMT338-VP.**

# 9 Module Performance

## 9.1 Introduction

The following figures show data captures using the SMT391-VP to capture the data and Matlab to plot and display it. As the SMT391-VP is a broadband converter no type of band-pass filtering were used when capturing these results. FFT Spurs might thus seem high at certain points, but in a specific system application selective signal filtering will significantly increase the quality of the captured signal. The analog input signal used is also not derived from the same clock source as the sampling clock. There is thus also no frequency coherence, which will once again add additional spurs to the FFT. All captures are with the AC coupled version of the module using the broadband Macon transformer on the input stage. There are three possible clock sources for captures – the on-board clock synthesizer (50 – 950 MHz range), the on-board VCO (600 – 1000 MHz range) and a separate external clock for each channel. The following figures show captures using these three clock sources.

## 9.2 Internal Clock - VCO

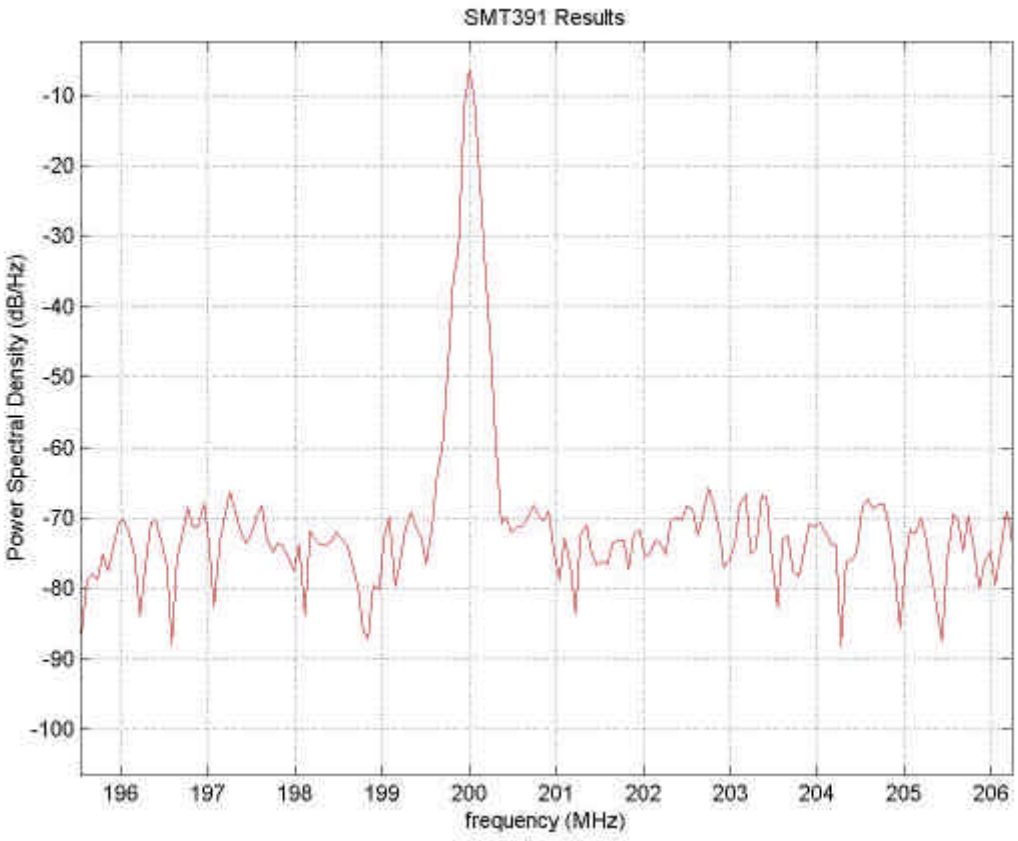



**Figure 62 – 200MHz Input, 1000MHz Internal VCO Clock (Zoom In).**

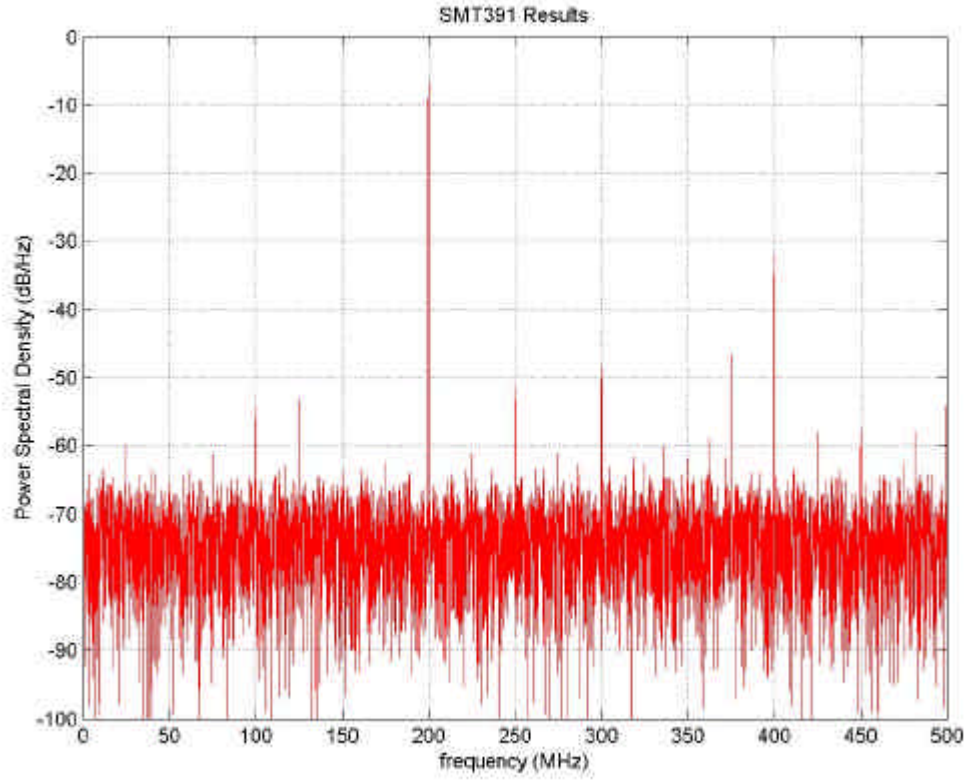



**Figure 63 – Channel I, Internal VCO 1000MHz Clock, 200MHz Input.**

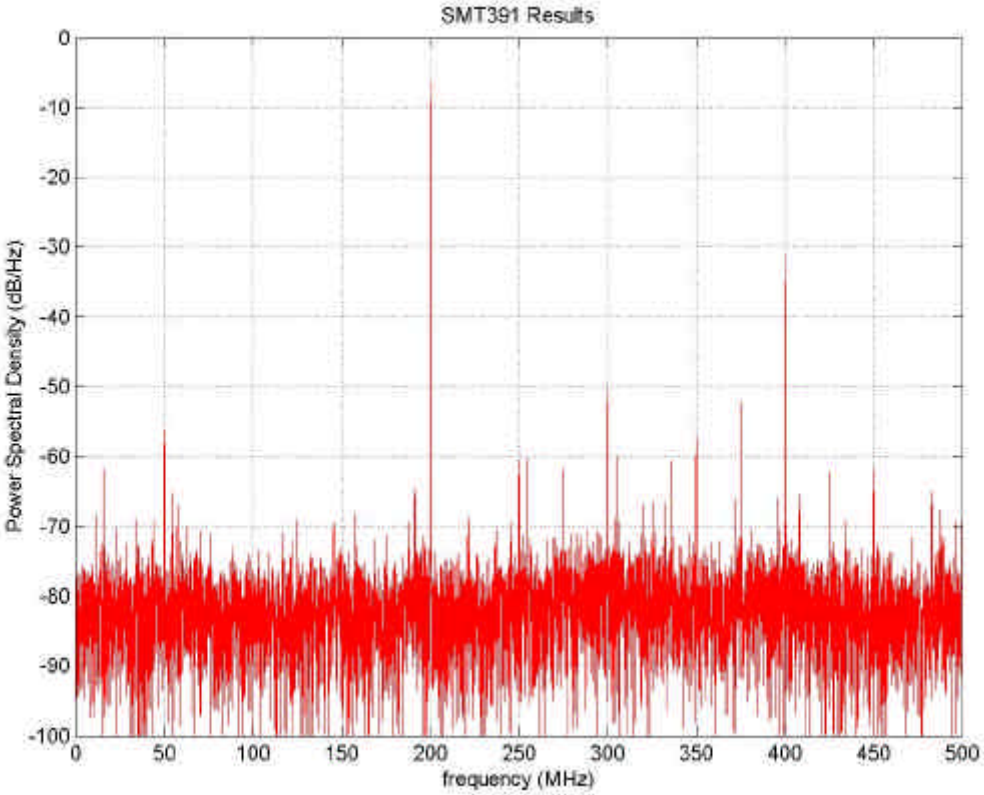



**Figure 64 – Channel Q, Internal VCO 1000MHz Clock, 200MHz Input.**

## 9.3 Internal Clock – Clock Synthesizer

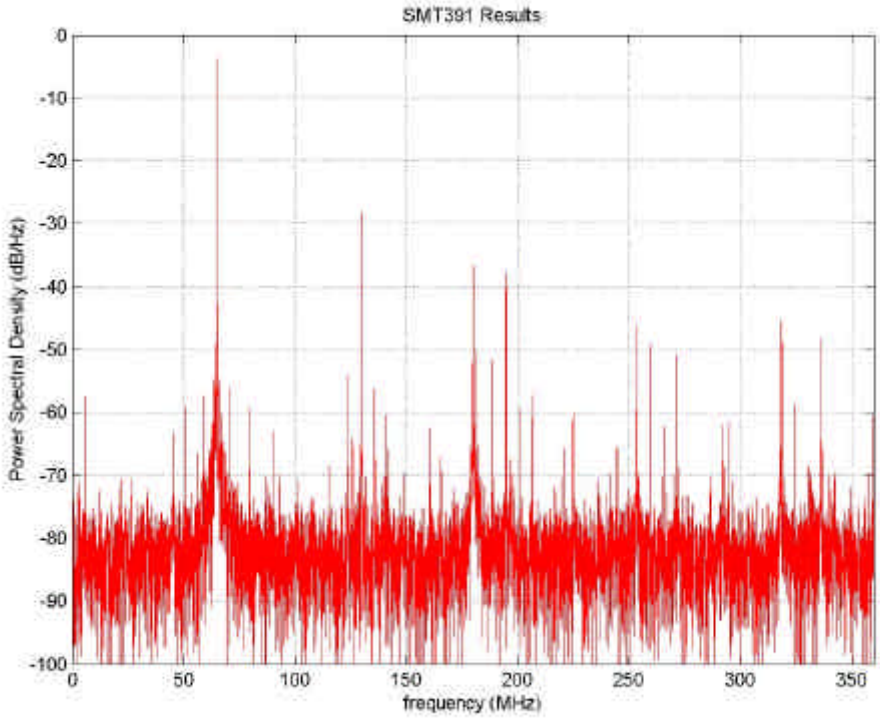



**Figure 65 – Channel I, Internal Synth 720MHz Clock, 65MHz Input.**

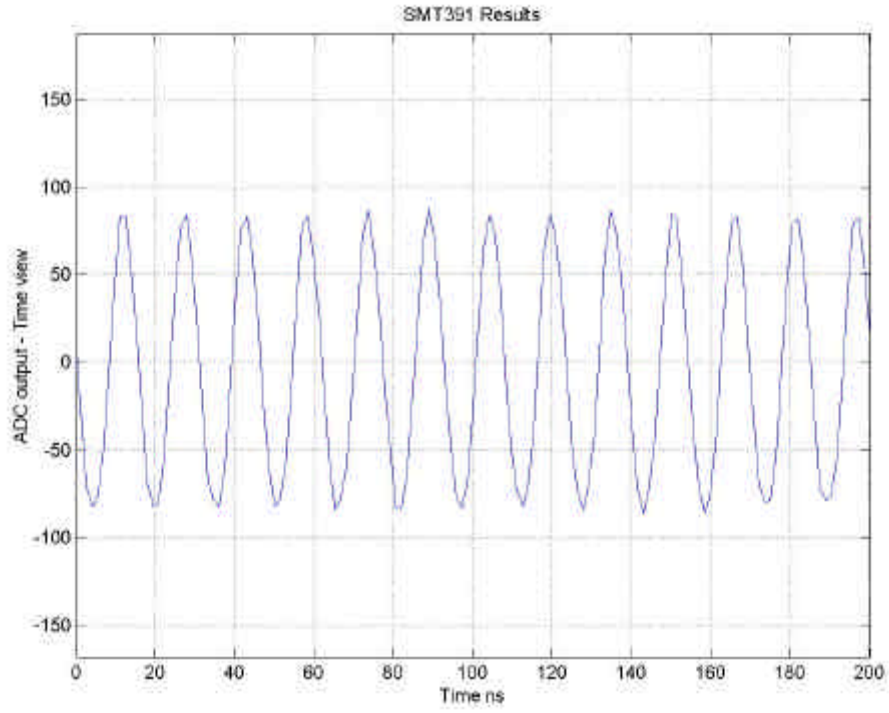



**Figure 66 – Channel I, Internal Synth 720MHz Clock, 65MHz Input – Time View.**

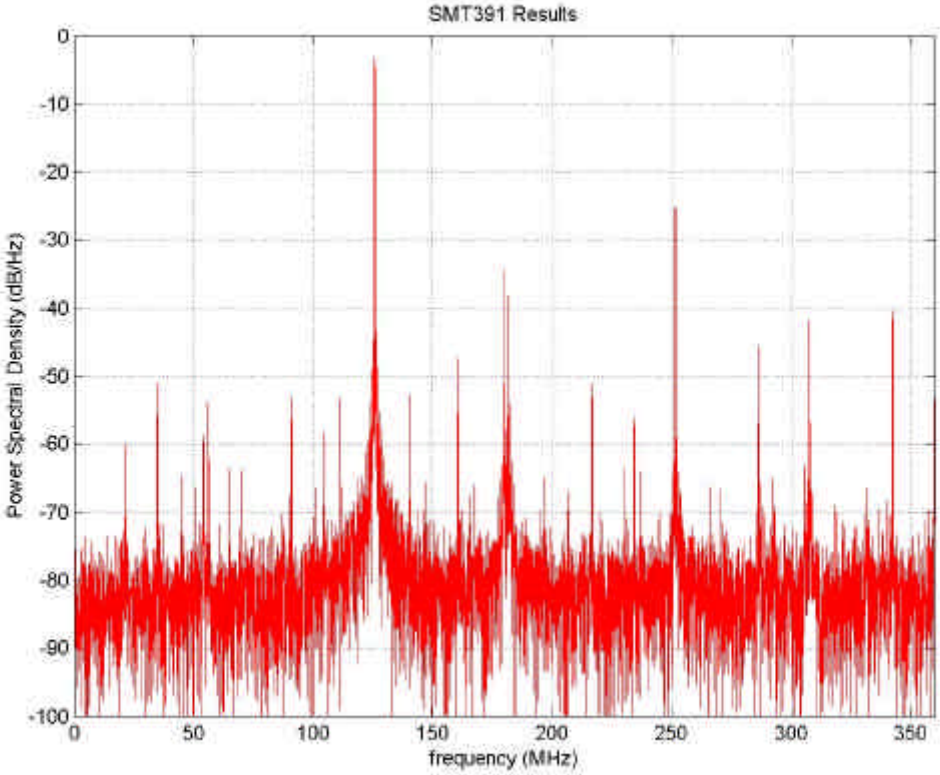



**Figure 67 – Channel Q, Internal Synth 720MHz Clock, 125MHz Input.**

## 9.4 External Clock

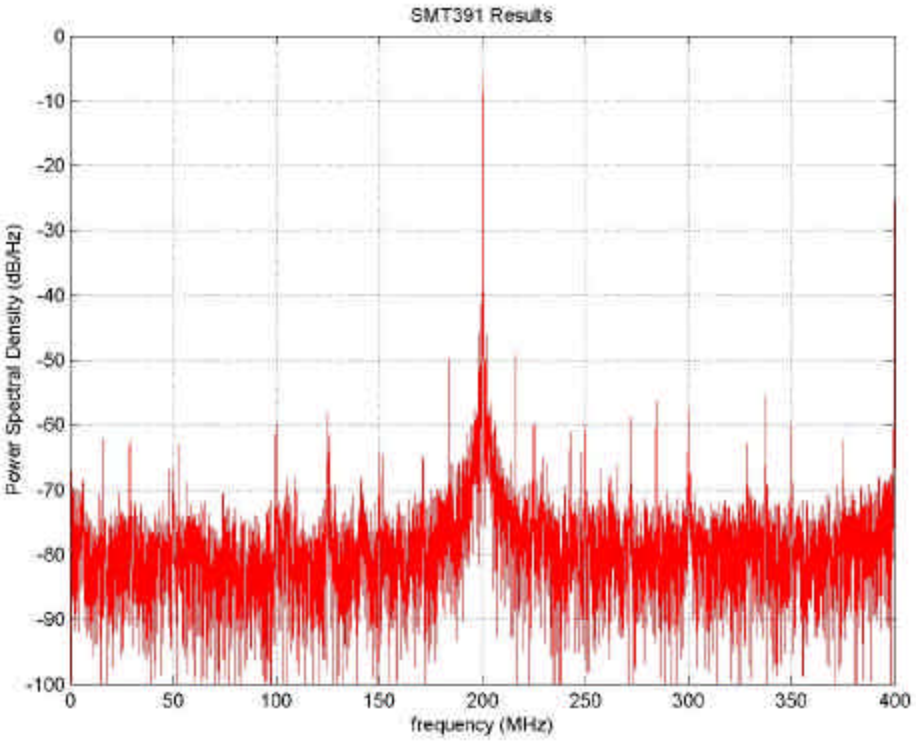



**Figure 68 – Channel I, External 800MHz Clock, 200MHz Input.**

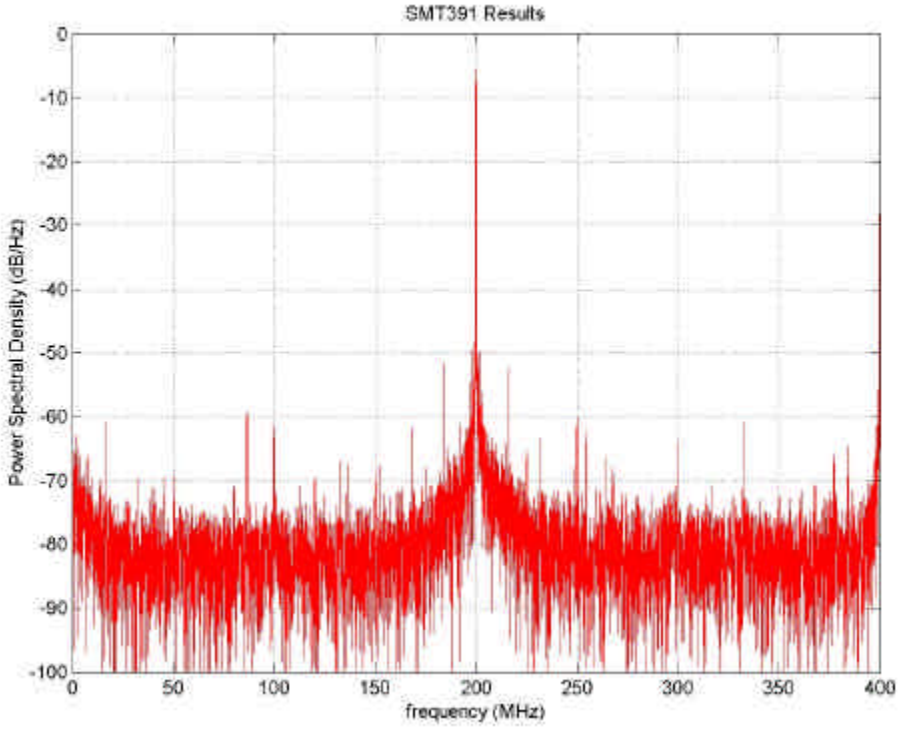



**Figure 69 – Channel Q, External 800MHz Clock, 200MHz Input.**

# 10 Firmware Building Blocks

## 10.1 Introduction

This section explains some of the basic low level firmware blocks that come with the example firmware design of the SMT391-VP.

## 10.2 Clock Synthesizer

A three wire uni-directional control interface is implemented between the FPGA of the SMT338-VP and the clock synthesizer present on the SMT391.

One 16 bit register in the SMT338-VP firmware is used for the setup of the clock synthesizer. The data word needed for the setup of the synthesizer is only 14 bits long - thus the 16 bit register is sufficient to receive data from the ComPort in one write cycle from the Host. When the ComPort receives the data for the clock synthesizer register it configures the internal firmware register accordingly and asserts the enable pin on the Clock Synthesizer State Machine.

The Clock Synthesizer State Machine generates the handshaking signals to clock data into the synthesizer. The synthesizer then generates an output clock depending on the setup given by the user. The output of the Synthesizer is a LVPECL signal.

The Clock Synthesizer register (present on the SMT338-VP firmware side) is used for the setup of the clock synthesizer on the SMT391. The table below shows the setup of this register:

| | Clock Control Register | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Byte** | **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| **1** | Do Not Care | | Test Bits | | | Output Division | | M Count |
| **0** | M Count | | | | | | | |

**Figure 70 – Clock Synthesizer Register.**

As the ComPort bit-stream is 16 bits long both bytes are written simultaneously. The most significant byte (Byte 1) contains the test bits, output division bits and one M count bit. The test bits selects between various internal node values and is controlled by the T[2:0] bits in the serial data stream (This feature is can be set up by the FPGA, but the value of the Test output is not read by the FPGA). The node values are shown in the table below.

| T2 | T1 | T0 | TEST | FOUT / $\overline{FOUT}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | Data Out – Last Bit SR | FVCO ÷ N |
| 0 | 0 | 1 | HIGH | FVCO ÷ N |
| 0 | 1 | 0 | FREF | FVCO ÷ N |
| 0 | 1 | 1 | M Counter Output | FVCO ÷ N |
| 1 | 0 | 0 | FOUT | FVCO ÷ N |
| 1 | 0 | 1 | LOW | FVCO ÷ N |
| 1 | 1 | 0 | S_CLOCK ÷ M | S_CLOCK ÷ N |
| 1 | 1 | 1 | FOUT ÷ 4 | FVCO ÷ N |

**Figure 71 – Clock Synthesizer Test Output.**

Output division on the clock synthesizer is achieved by the two output division bits found in the first byte of the clock control register. These configurations are underneath:

| N[1:0] | Output Division |
|---|---|
| 0 0 | 2 |
| 0 1 | 4 |
| 1 0 | 8 |
| 1 1 | 16 |

**Figure 72 – Clock Synthesizer Division Setup.**

The M count bits are used to configure the clock output frequency given all the constraints set by the hardware and the clock setup bits. The nine bits can be programmed with any value from 200 – 475. All the setup bits are then used to calculate the output with the following equation.

$$FOUT = \left(\frac{FXTAL}{8}\right) \times \frac{M}{N}$$

FXTAL = 16MHz (external oscillator)

N = Value in decimal, set up by the division bits.

M = Value in decimal, set up by the M count bits.

**Figure 73 – Clock Synthesizer Frequency Calculation.**

For more information refer to the Micrel datasheets of this part.

## 10.3 ADC Configuration

The 3-wire serial interface gives write-only access to as many as 8 different internal registers of up to 16 bits each (registers in the ADC). The ADC input format is always fixed with 3 bits of register address followed by 16 bits of data. The data and address are entered with the Most Significant Bit (MSB) first.

The following figure shows the timing diagram for the 3 wire setup interface of the ADC. The three wires are labelled 1 – 3.

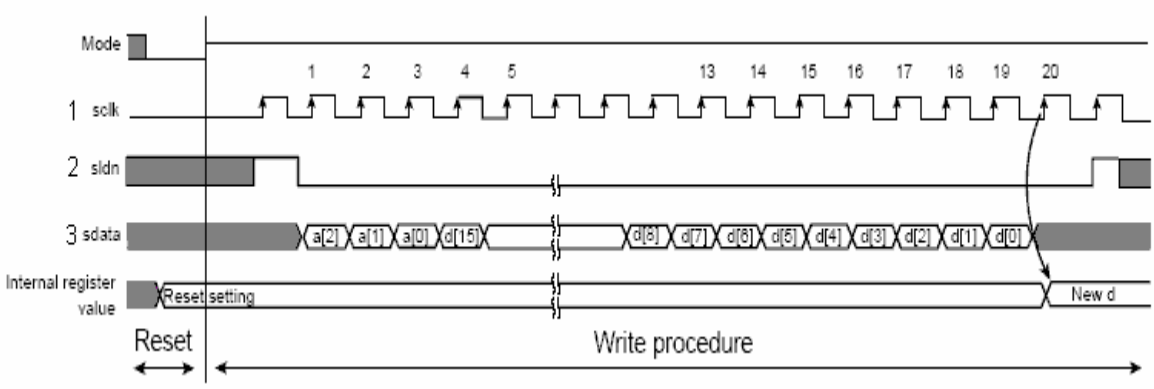



**Figure 74 – Timing Diagram for the Atmel ADC.**

Sdata gets clocked into the ADC on the rising edges of Sclk. For the initialisation of the sequence Sldn must be pulled high for one clock and then low again after the one clock. This will initialize the start condition for the ADC to be configured and then the data bits are clocked into it MSB first.

The state machine that clocks these bits into the ADC is shown in the figure below. This state machine is implemented in the firmware of the SMT338-VP FPGA.

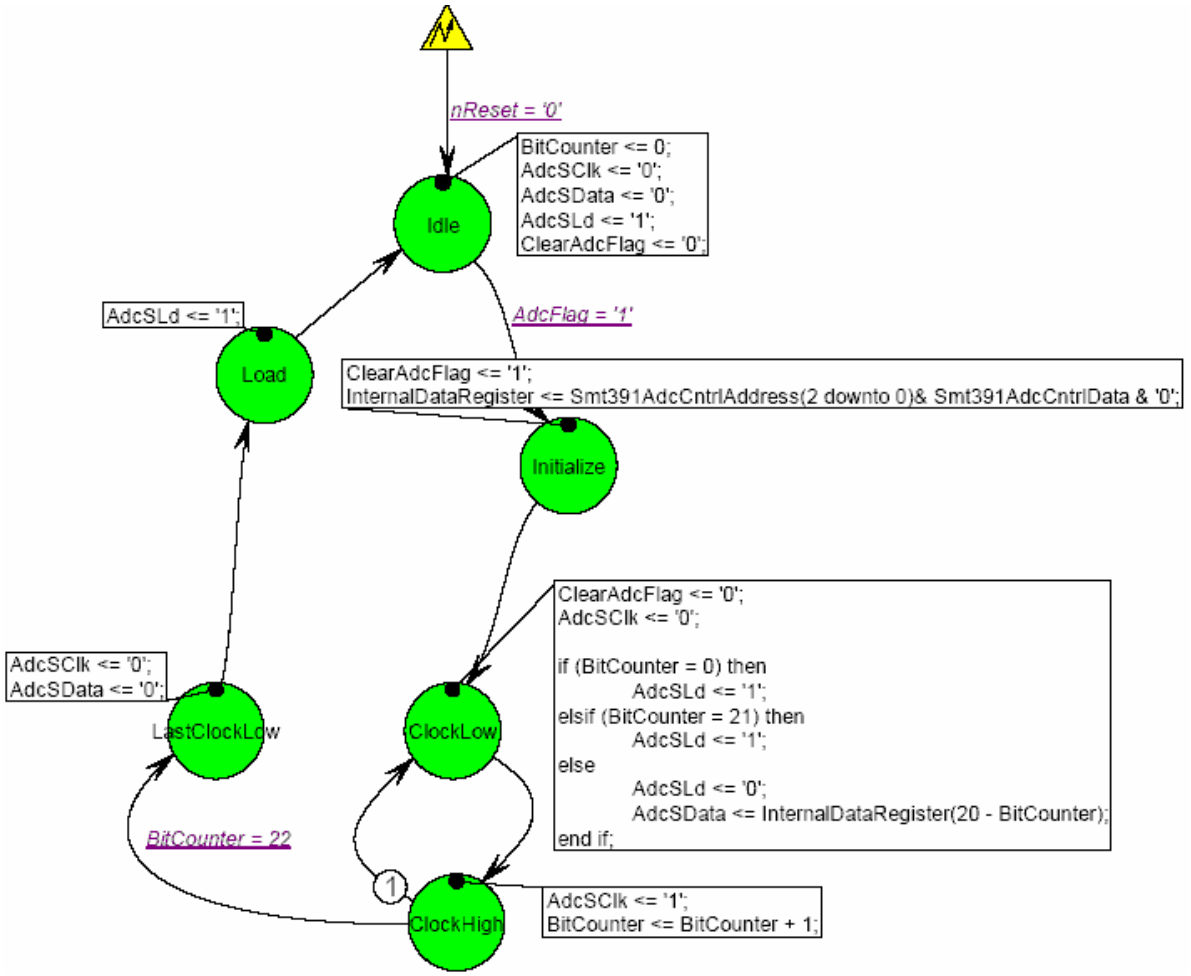



**Figure 75 – State Machine Driving the ADC Serial Interface.**

The state machine waits for the AdcFlag to go high before it switches to the Initialize state. In this state the InternalDataRegister is built up using the data and address input registers and then clocked out during the following two states - ClockLow and ClockHigh. After the counter is finished counting all the bits clocked out in these two states it jumps to LastClockLow which sends the first of the termination sequence and then jumps to the state Load which finalizes the configuration by pulling AdcSLd high.

## 10.4 PLL Configuration

The PLL 22-bit shift register is loaded via a microwire interface. This interface consists of 3 wires. The shift register consists of a 20-bit Data[19:0] Field and a 2-bit Address[1:0] Field. The Address Field is used to decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of 4 control registers depending on the state of the address bits. The MSB of Data is loaded in first. The register is shown in the following figure.

| MSB | | LSB |
|---|---|---|
| Data[19:0] | | Address[1:0] |
| 21 | 2 1 | 0 |

**Figure 76 – Register Setup for PLL.**

First off the LE line is pulled low and then the MSB of data is loaded onto the Data line. The Clock line is then driven high and low and a new Data line value is clocked into the Pll on each rising edge of the Clock line. The Data line is driven with the registers setup and the Clock line driven high and low until the Data line has reached the LSB. To end the sequence the LE line is pulled high.

There are two ways to operate the LE line as also shown in the figure below. The figure also explains how to configure the device.

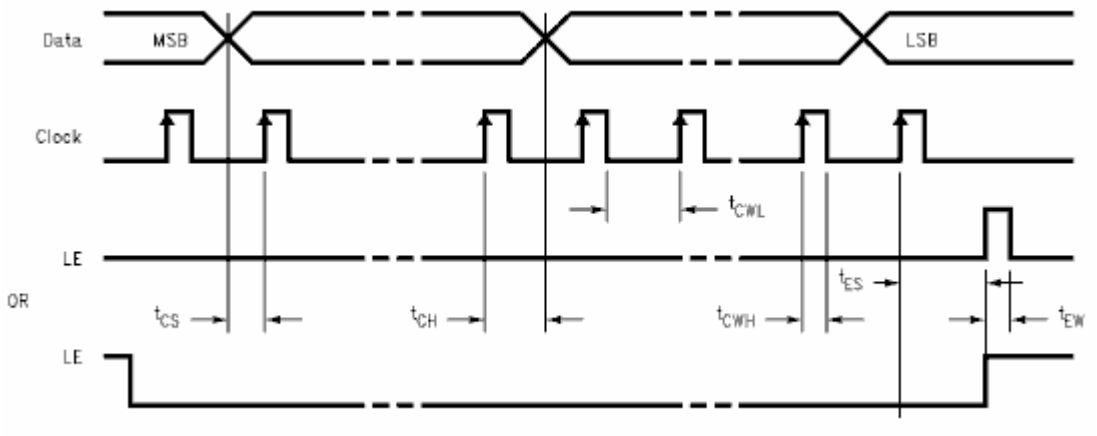



**Figure 77 – PLL Configuration Sequence.**

The figure below explains the state diagram residing in the firmware design (SMT338-VP's Fpga). This design ultimately executes the procedures explained in the previous figures and paragraph.

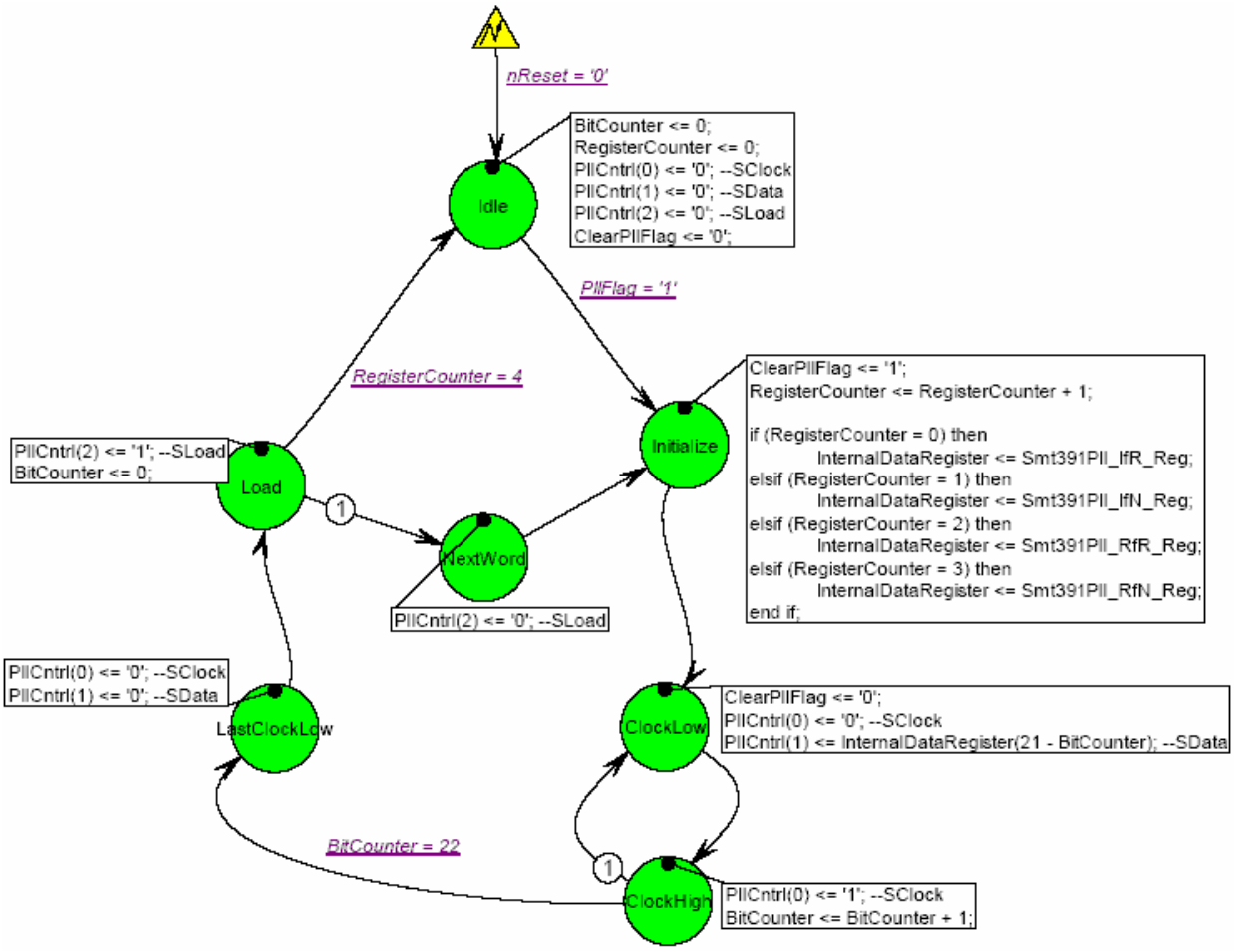



**Figure 78 – State Machine Driving the PLL Serial Interface.**