SMT398

User Manual

Revision History

Date	Comments	Engineer	Version
18.07.03	First released version	E.P	1.0.0
22.08.03	TIM CONFIG signal feature described	E.P	1.1.0
27.08.03	Minor corrections	E.P	1.1.1
05.09.03	Detailed description of FPGA I/Os constraint file signal names.	E.P	1.1.2
14.10.03	Addition of SHB connector names A, B ,C ,D.	E.P	1.1.3
28.10.03	Addition of figure 12 and details about pInout for SHB connectors in basic or full configuration	E.P	1.1.4
02.11.03	Minor clarification about the ZBTRAM Memory banks available depending on the board configuration and speed grade	E.P	1.1.5
27.07.04	Update of the Reset Control section to be more explicit about the various ways of handling reset control.	E.P	1.1.6
01.12.04	Removed statement saying that the FPGAfullconfig and loadbitstream code can be recompiled for any C6x-processor-board to use under Code Composer Studio and/or 3L Diamond.	E.P	1.1.7
12.01.05	Block Diagram update: removed wrong CPLD description (Timer)	E.P	1.1.8
20.05.05	Added: Start and End keys values	SM	1.1.9
17.10.05	Changed: Hyperlink for ZBTRAM datasheets	SM	1.2.0

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Physical Properties

Dimensions	See Physical specifications of TI TIM specification & user's guide
Weight	Varies in function of board configuration
Supply Voltages	See **Power Supplies**
Supply Current	See **Power Supplies**

Introduction

Related Documents

SUNDANCE SHB specification

Sundance SDB specification.

TI TIM specification & user's guide.

Samtec QSH Catalogue page

SMT6500 help file: FPGA support package

Block Diagram

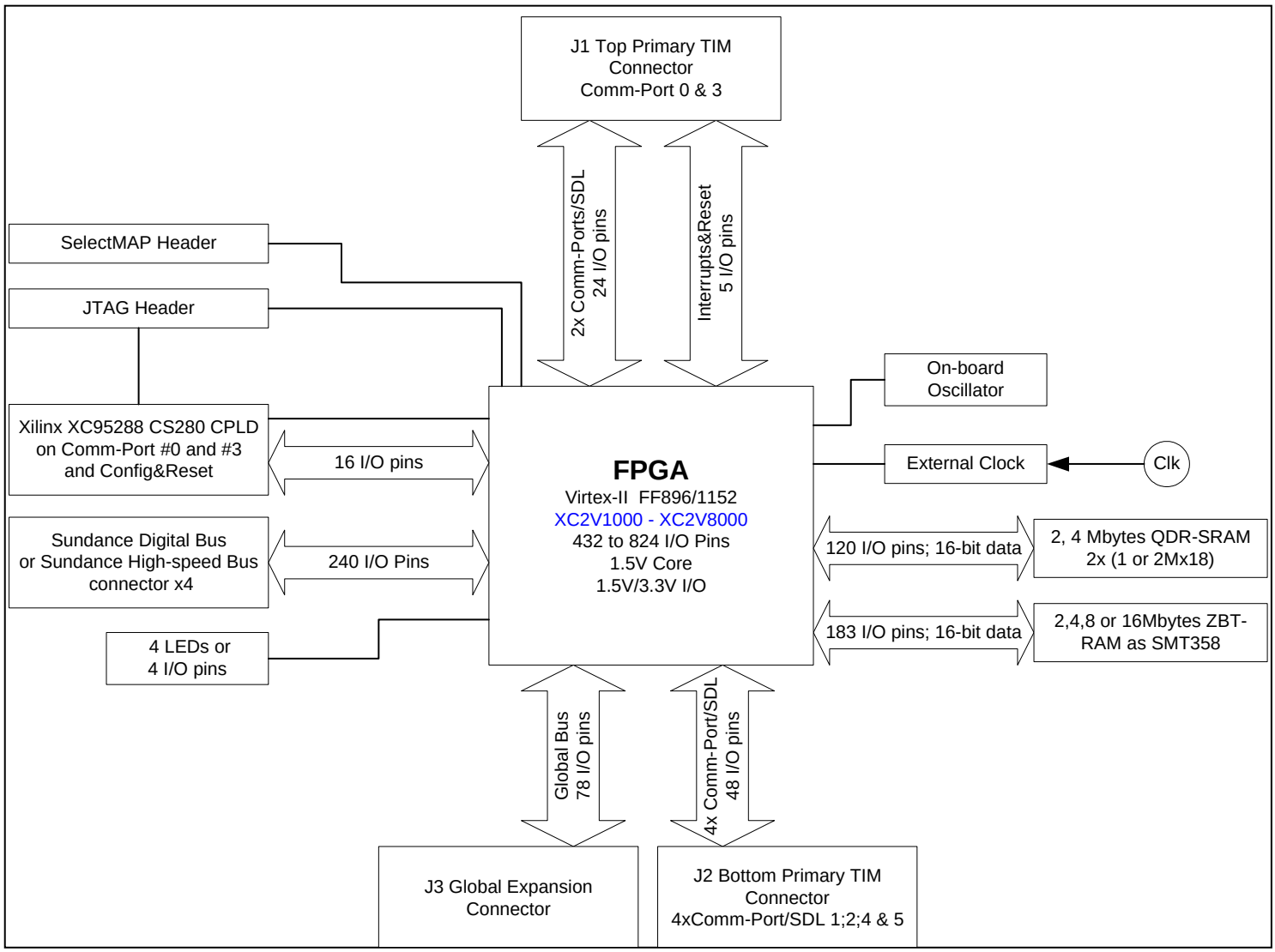


Figure 1:SMT398 Block Diagram

Mechanical Interface: TIM Standard

This module conforms to the TIM standard (**T**exas **I**nstrument **M**odule, See TI TIM specification & user's guide.) for single width modules.

It sits on a carrier board.

The carrier board provides power, Ground, communication links (Comport links) between all the modules fitted and a pathway to the host, for a non stand-alone system.

The SMT398 requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards), which must be provided by the two diagonally opposite mounting holes.

SMT398 Support

The SMT398 is supported by the SMT6500 software package available from SUNDANCE. Please register on SUNDANCE Support Forum if not yet registered. Then enter your company's forum and you can request the SMT6500 from there.

SMT398 Installation

Do NOT connect any external TTL (5v) signals to the SMT398 I/Os as the FPGA is NOT 5v compliant. This implies that the Comports and global bus lines of the carrier board MUST be LVTTL and that any device driving signals on the SHB connectors must drive at LVTTL (3.3v).

Two types of configuration are described here; nevertheless, you shouldn't be restricted and should consult Sundance if your system architecture differs.

SMT398 Alone

You can fit the SMT398 on its own, on the first TIM site of one of Sundance's 3.3v compatible carrier boards plugged in a host computer (PC, PCI, VME carrier etc…), like SMT310Q, SMT328, SMT300 etc…)

Please, follow these steps to install the SMT398 module on a Host system:

1. Remove the carrier board from the host system.
2. Place the SMT398 module on the first TIM site. This TIM site communicates with the host. (See your carrier board User Manual.) This allows you to use Global Bus and Comport 3 to communicate with the host.

3. Make sure that the board is firmly seated, and then provide the 3.3V to the board by screwing the SMT398 on the two main mounting holes with the bolts and screws provided with the board.
4. Connect the SHB links if required by your application.
5. Replace the carrier board in the host system or power on for a stand-alone carrier.

SMT398 + DSP TIM

You can fit the SMT398 coupled with a DSP module on any of Sundance carrier boards: Stand alones or plugged in a Host.

The DSP module can then be used to provide the SMT398 FPGA configuration bitstream and to communicate with the host.

Please, follow these steps to install the SMT398 module and the DSP TIM on a carrier:

1. Remove the carrier board from the host system or turn the power off for a stand-alone carrier.
2. Place the SMT398 module onto one of the TIM sites on the carrier board.
    - Preferably, fit the DSP TIM on the first TIM site. This TIM site communicates with the host. (See your carrier board User Manual.). This allows the processor board to handle the interactions with the Host by software instead of having to implement a communication interface in the SMT398 FPGA. (Global Bus interface or Comport interface on Comport 3).
    - Fit the Comport communication links between the DSP TIM and the SMT398 respecting the rules on polarity at reset. (See your carrier board User Manual.)
    - To configure the SMT398 FPGA using the DSP TIM, then you need a link between the 2 modules: Comport 3 of the SMT398 **MUST** be connected to one of the transmit Comport at Reset (Comport 0,1 or 2) available on the DSP TIM.
3. Make sure that the board is firmly seated, and then provide the 3.3V to the board by screwing the SMT398 on the two main mounting holes with the bolts and screws provided with the board.
4. Connect the SHB links if required by your application.
5. Replace the carrier board in the host system or power on for a stand-alone carrier.

FPGA Configuration

The FPGA can be configured 2 different ways:

- Using Comport 3 to provide the bitstream. (See The service CPLD)
- Using the on-board JTAG header and Xilinx JTAG programming tools. (See FPGA in system programming)

At power up the FPGA is not configured.

LED L5 (See Figure 19:SMT398 Components placement-Top view, bottom right hand corner of the picture) will be lit upon FPGA configuration.

Electrical Interface

The service CPLD

The CPLD allows for FPGA configuration in slave SelectMap mode.

At power up or after a Reset of the SMT398, the CPLD is configured and implements a Comport link receiver on Comport 3.

The CPLD is connected to Comport number 3 of the SMT398 TIM connector. Consequently, the Comport on the other end of the link must be configured as transmitter at power-up or after reset, i.e. Comport channels 0, 1, or 2.

The typical SMT398 user does not need an in depth understanding of the configuration sequence and of the Virtex II. However, for the purpose of debugging and designing for the SMT398 an overview of the necessary configuration protocol and bitstream formatting is recommended.
Therefore, this section describes the CPLD functions, the Virtex II bitstream format and the necessary bitstream re-formatting when downloading the bitstream to the FPGA via CPLD + Comport 3.
Figure 2: FPGA configuration in SelectMap mode using CPLD provides waveforms to illustrate the descriptions below.

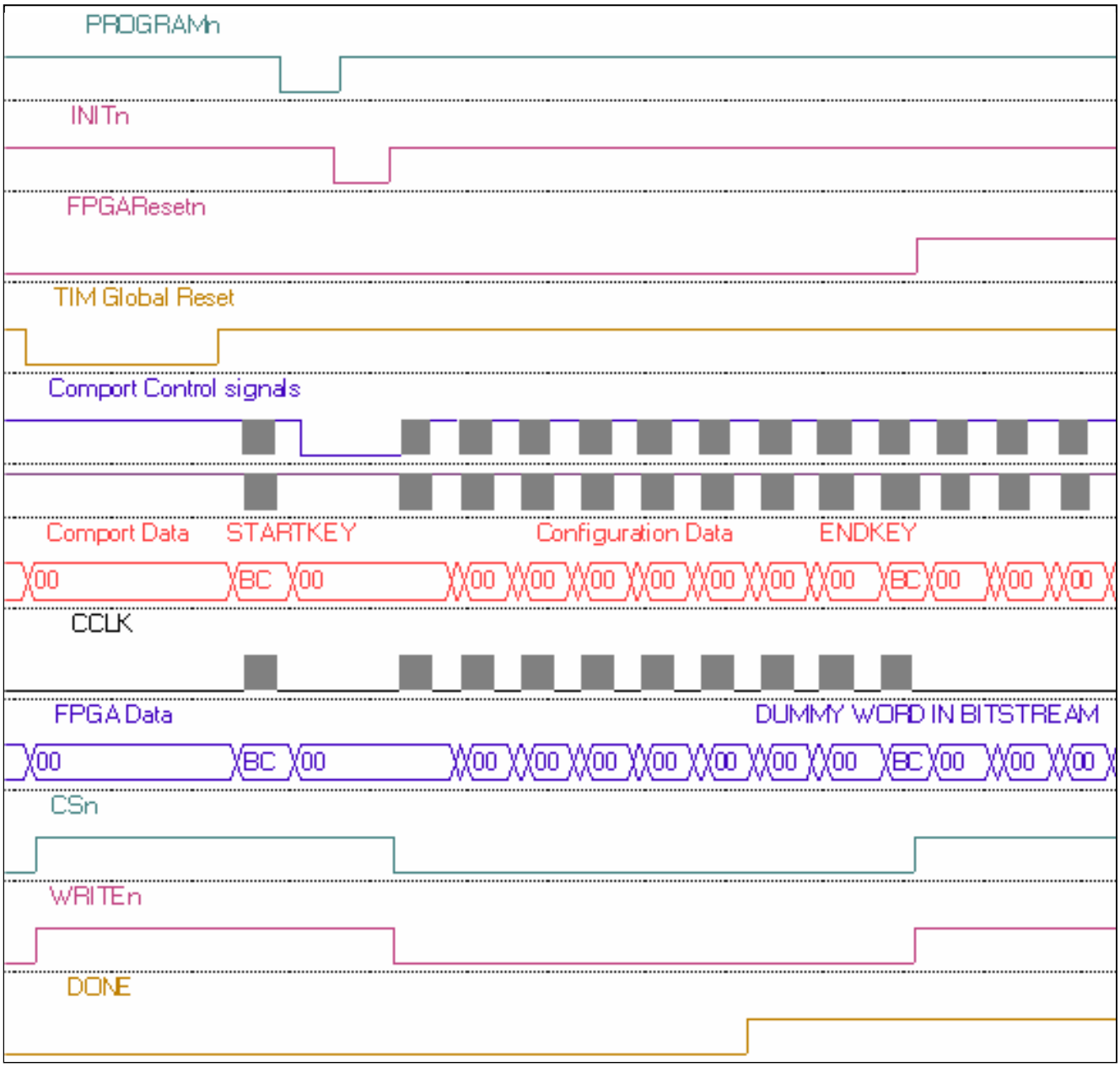


Figure 2: FPGA configuration in SelectMap mode using CPLD

CPLD Functions

- Decode Commands coming on Comport 3.
- To Implement a Comport Receiver on Comport 3 after Reset or at Power up.
- Configure FPGA.
- Reset FPGA.

Decode Commands

At power up, after a TIM global Reset, or once the FPGA configuration process is over, the CPLD reads any word coming on its Comport.

If a received word cannot be recognized as a command, the word is read completely but ignored. The CPLD recognizes the following two commands:

- STARTKEY (0xBCBCBCBC)
- ENDKEY (0xBCBCBC00)

Comport Receiver

At power up or after a TIM global Reset, the CPLD takes control of Comport 3.

Once the ENDKEY command is received, the CPLD releases Comport 3.

The Comport communication is performed in 32-bit words, where each word consists of four consecutive bytes. The Comport protocol transmits words starting with the least-significant byte (LSByte), i.e. byte0, as shown in Figure 3: Comport word Byte order, and 1 byte at a time.

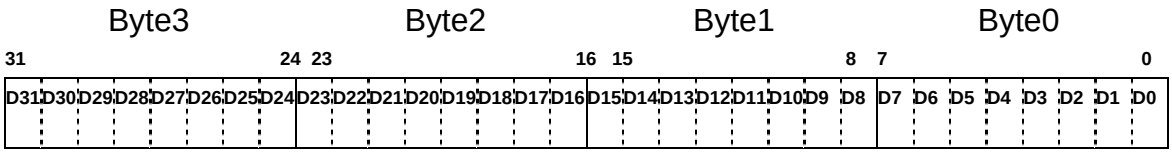


Figure 3: Comport word Byte order

Configure FPGA

The signals INITn and DONE are CPLD inputs, the other one are CPLD outputs that the CPLD drives to configure the FPGA.

On reception of the STARTKEY command the CPLD clears the FPGA configuration memory by asserting the PROGRAMn pin low. On INITn going low, the CPLD brings PROGRAMn high and waits for INITn to come back high before starting the FPGA configuration.

Afterwards, the CPLD asserts CSn and WRITEn low for the rest of the configuration process.

The CPLD pulses high CCLK to loads in the FPGA any new byte present on the Comport by.

The CPLD does not implement any operation on the bitstream and passes it straight through to the FPGA once the STARTKEY has been decoded and until the ENDKEY is decoded.

Once the FPGA DONE pin has gone high, LED L5 (See Figure 19:SMT398 Components placement-Top view, bottom right hand corner of the picture) becomes on, indicating that the FPGA configured.

The CPLD disables the SelectMap interface and waits for the ENDKEY command on Comport3.

Once the ENDKEY command is received, the CPLD releases Comport 3.

Reset Control

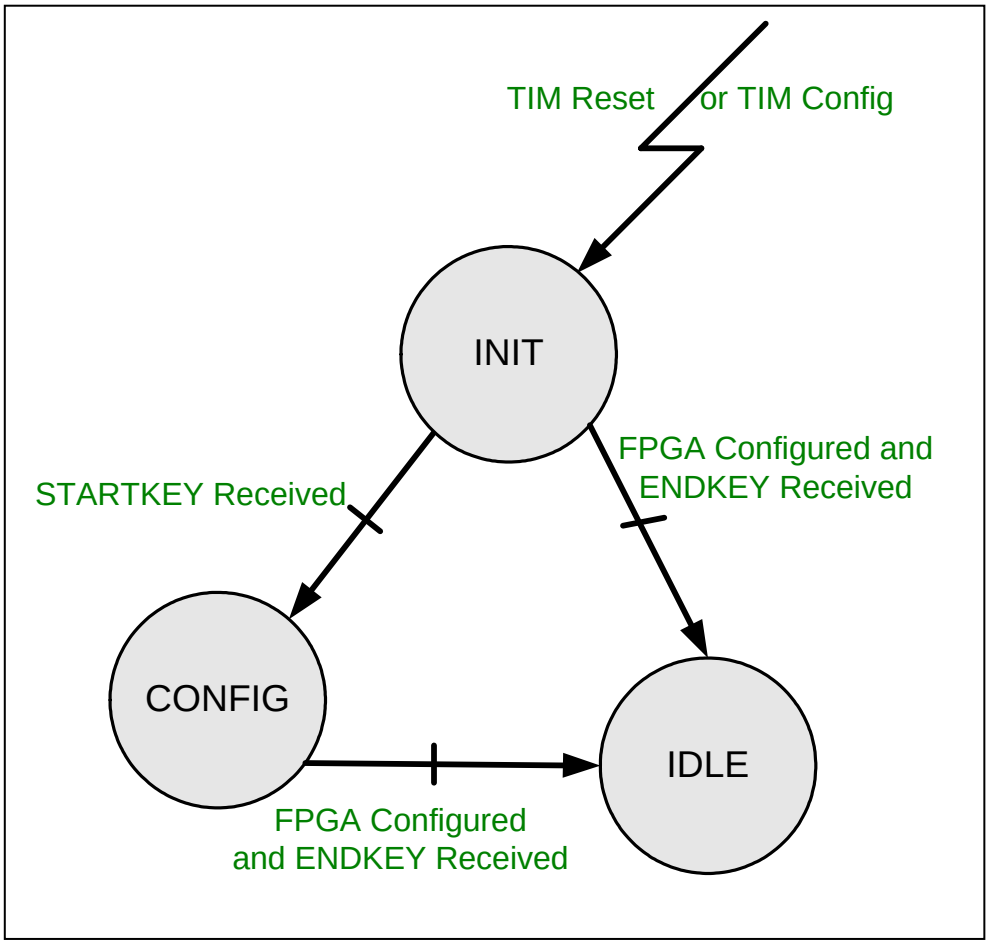


Figure 4: CPLD state machine

TIM Global Reset

The CPLD is connected to a TIM global Reset signal provided to the SMT398 via its TIM connector J4 pin 30. (See Figure 19:SMT398 Components placement-Top view).

The TIM global Reset signal is also available for the FPGA but the CPLD provides another signal called **FPGAReset_In** that offers a better Reset control over the FPGA.
At power up or on reception of a low TIM global Reset pulse, the CPLD drives the FPGAReset_In signal low and keeps it low.
When the ENDKEY has been received, the CPLD drives FPGAReset_in high.
I recommend that you use **FPGAReset_In** for the Global Reset signal of your FPGA designs.
In this manner, you can control your FPGA design Reset activity and you will also avoid possible conflicts on Comport 3 if your FPGA design implements it.

The Reset control is operated by the CPLD line FPGAReset_In.

DO NOT use TIM GLOBAL Reset unless you have a very specific need for your application.

TIM CONFIG

A TIM CONFIG signal coming from the TIM connector J4 pin 74. (See Figure 19:SMT398 Components placement-Top view and Figure 11:SMT398 Comports connections) is available to the CPLD.

CONFIG falling has the same effect on the SMT398 CPLD as a TIM global Reset pulse.

On detection of a falling edge on the CONFIG line, the CPLD drives the FPGAReset_In signal low and keeps it low.

CONFIG provides a means of reprogramming the FPGA without having to drive the TIM Global Reset signal.
Therefore any other modules sensitive to the TIM global Reset signal will not be affected and can keep running their application.

CONFIG is driven from another TIM site on the carrier board, for instance, from a DSP module running an application. (See the SMT6400 help file for information on the DSP TIM CONFIG signal).
Writing ‘1’ to the DSP CONFIG bit in the config register tristates the line (pull-ups on the carrier board pull CONFIG high)
Writing ‘0’ to the DSP CONFIG bit in the config register makes the CONFIG signal go low.

After a Global Reset pulse, a DSP module drives CONFIG low and keeps it low by default.
After Reset and loading of the DSP application, CONFIG can be driven the following way:

```
#include “SMT3xx.h”
#define CONFIG_BIT  1<<6

int main()
{
  *CONFIG |= CONFIG_BIT; //tristates CONFIG (Pull-ups on the carrier board pull CONFIG high)
  *CONFIG &= (UINT32)~CONFIG_BIT;//CONFIG is driven low
//delay while the FPGA is configured
  *CONFIG |= CONFIG_BIT;
}
```

This feature can be interesting in systems where:

- The FPGA needs to implement multiple functions spread in different bitstreams that are needed at different stages of the application.
- The system needs to keep running and can’t be interrupted by a global Reset pulse when the SMT398 FPGA needs to be configured with a new bitstream.
- The FPGA needs to be kept in reset BUT NOT reprogrammed.
    - Config low Pulse: the CPLD drives the FPGAReset_In signal low and keeps it low.
    - ENDKEY: The CPLD drives the FPGAReset_In signal high.

Notes:

- TIM CONFIG is only available on SMT398 v3. The SMT398 version is written on TOP of the board (See Figure 19:SMT398 Components placement-Top view).
- TIM CONFIG needs CPLD code version 2.1 or above (Written on a sticker on the CPLD. (See Figure 19:SMT398 Components placement-Top view).
- The Comport3 is reserved for the CPLD and cannot be made available to the FPGA.
- CONFIG needs switch SW1 position 8 to be ON. (See Figure 20: SMT398 Components placement-Bottom view)
- If you have more than one DSP module on a carrier and that you want to use the CONFIG line, you must decide which TIM is going to be the master and have the other DSP modules to tri-state their CONFIG line at the start of their application by writing '1' to the corresponding register bit. (See the SMT6400 help file for information on the DSP TIM CONFIG signal).

Summary:

The Reset level on the SMT398 FPGA is active low.

The reset line to be used is FPGAReset_in on pad AM20 for FPGAs in the big package (FF1152) and AK18 for the smaller package FPGAs.

Virtex II Bitstream Format

The Virtex II SelectMap interface is an 8-bit interface on the device with data pins labeled D[7:0]. The configuration bitstreams can be written eight bits per clock cycle.

The Virtex II configuration bitstreams generated by BitGen (.bit files) contain a mix of commands and data on 32 bit word boundaries, shown in Xilinx application note 138 page 20. This format assumes D0 is considered the MSBit as shown Figure 5: V II Configuration Bitstream Word Format.

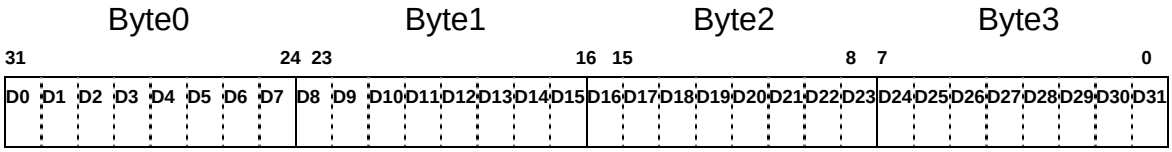


Figure 5: V II Configuration Bitstream Word Format

As a result, to be able to download the bitstream to the FPGA using Comport3 + CPLD, the Virtex II configuration bitstream must be re-formatted to match the Comport word standard.

Bitstream Re-formatting

The re-formatting consists in inverting the bits in a byte and the bytes in a 32-bit word.

Further, the .bit files contain a header section before the pad word and synchronization word. The download function FPGAFullConfiguration() from the SMT6500 package searches for the synchronization sequence and skips the header.

CPLD code versions

- V1.0: Initial release that only receives the bitstream and configures the FPGA. FPGAResetn is **NOT** implemented and Comport 3 is **NOT** released once the FPGA is configured.
- V2.0 Indicated on a sticker on the CPLD. The CPLD implements the functions described above except TIM CONFIG.
- V2.1 Indicated on a sticker on the CPLD. V2.0 + the CPLD implements the reconfiguration feature described in TIM CONFIG.

FPGA

The module can be fitted with a XC2V1000, XC2V1500, XC2V2000, XC2V3000, XC2V4000, XC2V6000 or XC2V8000.

The FPGA comes in two pinout/footprint compatible packages: flip-chip FF896 and FF1152.

The choice of FPGA will be price/performance driven. The following table shows the main FPGA characteristics.

The choice of the FPGA also determines which board architecture you will get (amount of logic available, speed, number and type of I/Os, on-board Memory size and type). For a complete list of the different board architectures, please consult: 0 Ordering information:

This Xilinx Virtex II, is responsible for the provision of up to 4 SHBs, up to 6 Comports, the global bus and QDR/ZBT memory banks (In FULL configuration, see 0 Ordering information:)

Device	**System gates**	**CLB(1 CLB = 4 slices = Max 128 bits)**				SelectRAM Blocks		
		Array Row x Col	**Slices**	Maximum distributed RAM Kbits	Multiplier blocks	18-Kbit Block	Max RAM (Kbits)	DCMs
XC2V1000	1M	40x32	5,120	160	40	40	720	8
XC2V1500	1.5M	48x40	7,680	240	48	48	864	8
XC2V2000	2M	56x48	10,752	336	56	56	1,008	8
XC2V3000	3M	64x56	14,336	448	96	96	1,728	12
XC2V4000	4M	80x72	23,040	720	120	120	2,160	12
XC2V6000	6M	96x88	33,792	1,056	144	144	2,592	12
XC2V8000	8M	112x104	46,592	1,456	168	168	3,024	12

Table 1: FPGA Choices

The Xilinx FPGA is configured from one of several modes:

- Slave SelectMAP.
- JTAG/Boundary scan

And from one of several sources:

- Comport 3 (Using Slave SelectMAP)
- Parallel cable III-IV (Using JTAG)
- MultiLINX cable. (Using JTAG or Slave SelectMAP)

At power up the FPGA is not configured.

LED L5 (See Figure 19:SMT398 Components placement-Top view, bottom right hand corner of the picture) will be lit upon FPGA configuration.

FPGA in system programming

The factory default for the FPGA configuration mode is using Slave SelectMAP mode and the Comport3.

Configuring the FPGA from Comport 3 allows NOT USING any JTAG cables.

Having a direct link enhances debugging and testing, and therefore reduces the product's time to market.

Once the design is complete, the configuration data can be stored on disk and then loaded each time the system powers up or is reset.

The configuration data can also be downloaded into a DSP TIM module external memory along with the DSP application. See TIM CONFIG.

The bitstream is presented on Comport3 and the CPLD provides the mechanism to deliver it quickly to the Virtex-II device using the Slave SelectMAP mode.

Then, the configuration cycle can be transparent to the end user.

After configuration the Comport3 can be available to the FPGA for data transfers if the Virtex II is XC2V3000 or above and if your CPLD design version allows it. See CPLD code versions

SMT398 Alone

Host software can be developed to communicate with the SMT398.

See SMT6025 User Manual on Sundance Web site for more information on how to develop Host applications for Sundance Hardware.

The host Software application BitstreamLd.exe provided in the SMT6500 package is compiled for Windows NT/2000/XP.

It allows downloading a bitstream to the SMT398 FPGA by accessing Comport 3 of the carrier board's first site.

SMT398 + DSP TIM

The DSP software routines provided are the download functions LoadBitstream() and FPGAFullConfiguration().

- LoadBitstream():This function reads a bit file from your local HD and stores it on the DSP board.
- FPGAFullConfiguration(): The FPGA is configured with data from a .bit file stored on your DSP board.

These functions were developped using 3L Diamond's high level Comport link functions and will NOT work under CCStudio. You will have to develop your own functions to work under CCStudio.

- Bit2Asm.exe. This stand alone executable formats a bit file into a Texas instrument's asm file. Then you can embed it in your application's object file at linking time. As a result, the FPGA bitstream is downloaded with the application into the DSP module's memory which provides a faster FPGA configuration process than the standard way. See TIM CONFIG.
- You can find detailed information about the DSP software routines in: Application note about bitstream download software.pdf

JTAG/Boundary Scan

JTAG Programmer (iMPACT)

The JTAG Programmer software is a standard feature of the Alliance Series ™ and Foundation Series ™ software packages. JTAG Programmer is a part of Web Pack, which can be downloaded from the following site:

Xilinx JTAG programmer

- Configuring with the parallel cable III or IV

The JTAG chain is composed of the CPLD and the FPGA.

The CPLD is pre-programmed by Sundance.

Do NOT try to reprogram the CPLD without SUNDANCE approval

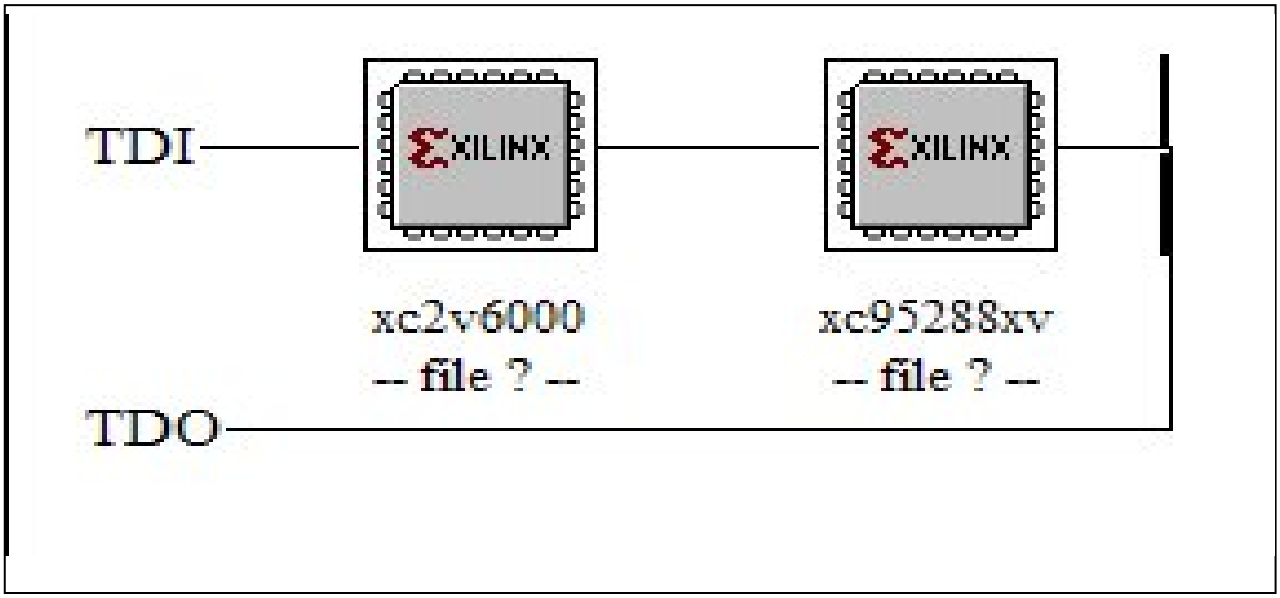


Figure 6: JTAG Chain on the SMT398

When accessing the board using JTAG, the CPLD can be bypassed and you can configure the FPGA only.

Xilinx describe how to connect both download cables at: Parallel cables

Xilinx describe how to configure their devices using these cables at: Configuration Mode General Information.

For complementary and more detailed information please go to: Xilinx 5 software Manuals and Help.

See board header pinout in Table 10: Connector J13-JTAG Header

Configuring with MultiLINX

The Mutilinx cable can be used to configure the FPGA via JTAG or SelectMap mode.

See board header pinout in Table 10: Connector J13-JTAG Header, Table 11: Connector J13-Flying Lead Set #1 and Table 12: Connector J12 Flying Lead Sets 3&4.

The MultiLINX cable set is a peripheral hardware product from Xilinx.

For additional information on the MultiLINX cable set, go to the following site:

Xilinx MultiLINX cable

FPGA Readback and Partial reconfiguration

Using Comm-port3

Readback and partial reconfiguration are enabled by a specific design for the CPLD, **not provided as a standard feature of the CPLD** but that can be purchased from Sundance. Contrary to the original design, the CPLD is dedicated to control the FPGA and does not provide a communication channel to user logic residing on the FPGA anymore. The CPLD is connected to Comport number 3 of the SMT398 connector, which cannot be used anymore by the FPGA to transfer data.

Therefore, the CPLD controller can configure, readback, partially reconfigure the Virtex II and capture.

Using MultiLINX /Parallel cable III or IV

The JTAG and the MultiLINX SelectMAP headers are also provided to enable application debugging via suitable software. Typically, this will be Xilinx ChipScope ILA (Integrated Logic Analyzer).

The ChipScope Analyzer supports both the Xilinx MultiLINX™ and Parallel Cable III download cables for communication between the PC and FPGA(s). The MultiLINX cable supports both USB (Windows 98 and Windows 2000) and RS-232 serial communication from the PC. The Parallel Cable III supports only parallel port communication from the PC to the Boundary Scan chain.

Memory

Pipelined ZBTRAM

Up to 16Mbytes of pipeline ZBT memory is provided with direct access by the FPGA.

The ZBTRAM is designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.

This device is well suited for SDR applications that experience frequent bus turnarounds, need to operate on small data chunks (especially one-word chunks), and need to operate at higher frequencies than permitted by the flow-through version.

The memory is split into 2 to 4 independent 16-bit-wide Banks depending on the configuration you select.(in Basic configuration or in Full configuration)

All three chip enables are available on each bank for simple depth expansion with no data contention.

Each bank is composed of one chip, available in 4 different sizes as presented in Table 2: ZBTRAM sizes.

The memory is expected to be clocked at 166 MHz (speed grade is: -16)

For more complete information, please read:

General Information on how to choose your memory type according to your application

For the parts datasheet please read:

ZBTRAM datasheets

Chips parts and densities are shown in the table below.

ZBTRAM part number	Size in bits	Size in Bytes	Actual Memory size	Amount of memory per board
K7N401801A	4Mb	512kBytes	256kx18	2 MBytes
K7N801801M	8Mb	1MBytes	512kx18	4 MBytes
K7N161801A	16Mb	2MBytes	1Mx18	8 MBytes
K7N321801M	32Mb	4MBytes	2Mx18	16 MBytes

Table 2: ZBTRAM sizes

The total available ZBT RAM on the board is therefore 2 MBytes, 4 MBytes, 8 MBytes, or 16 MBytes

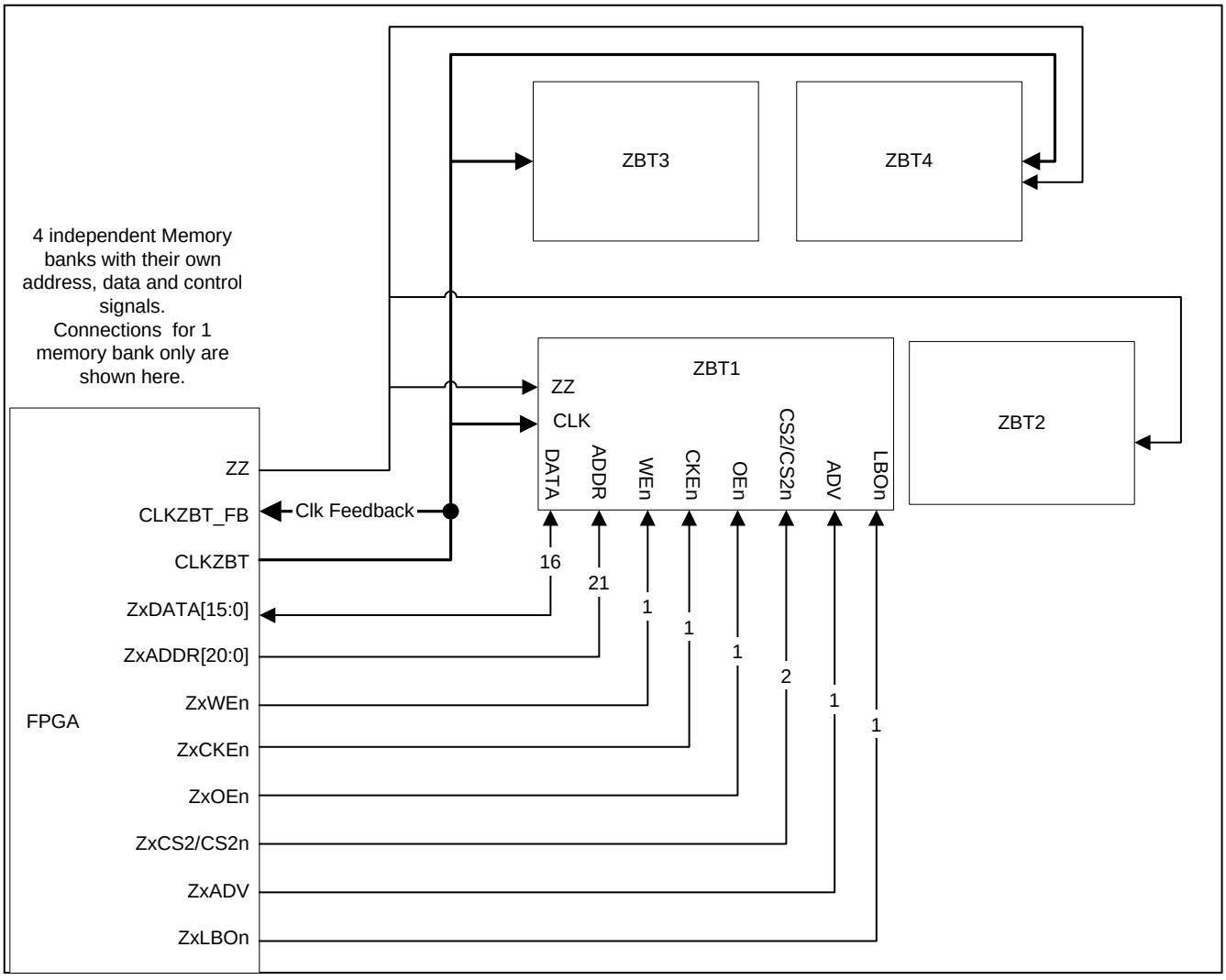


Figure 7:SMT398 ZBT Memory Banks arrangement

Constraints File Signal Names

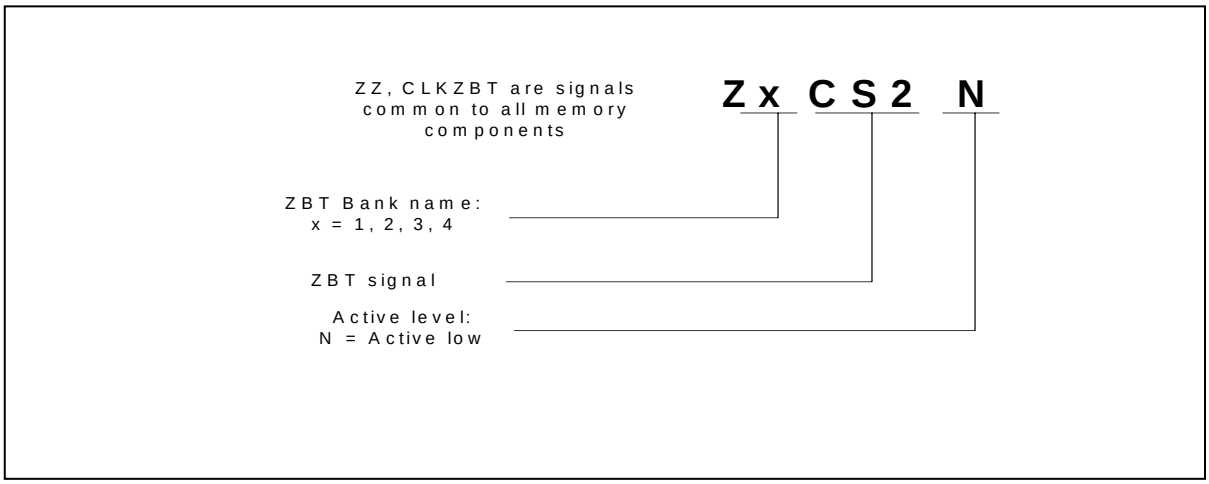


Figure 8: ZBT Constraints file signal names

QDR (Quad Data Rate)

Up to 8 Mbytes of QDR (Quad Data Rate) Synchronous Pipelined Burst SRAMs memory is provided with direct access to the FPGA. (Provision has been made to accommodate up to 64 Mbytes of QDR when the memory chips will be available)

The QDR operation is possible by supporting DDR (Double Data Rate) read and writes operations through separate data output and input ports with the same cycle.

Memory bandwidth is maximized as data can be transferred into SRAM on every rising edge of the write clock, and transferred out of SRAM on every rising edge of the read clock. (Read clock is write clock shifted of 90 degrees)

And totally independent read and write ports eliminate the need for high-speed bus turn around. The memory is expected to be clocked at 166 MHz allowing a data throughput rate of 1.3 GBytes/s.

The memory bank of the SMT398 is composed of 2 devices added in parallel in width expansion architecture. The address bus, input clocks, R# and W# are common to both devices. The data buses are not common.

Each chip is available in 3 different sizes (up to 164Mbits chips are expected)

QDR part number	Size in bits	Size in Bytes	Actual Memory size	Amount of memory per board
CY7C1302V25	8Mb	1MBytes	512kx18	2 MBytes
k7q1636(18)52a	16Mb	2MBytes	1Mx18	4 MBytes
k7q3236(18)52m.pdf	32Mb	4MBytes	2Mx18	4 MBytes

Table 3: QDR RAM sizes

Due to a board layout issue the total available QDR RAM is 2 Mbytes or 4Mbytes with the 32Mb chips fitted.

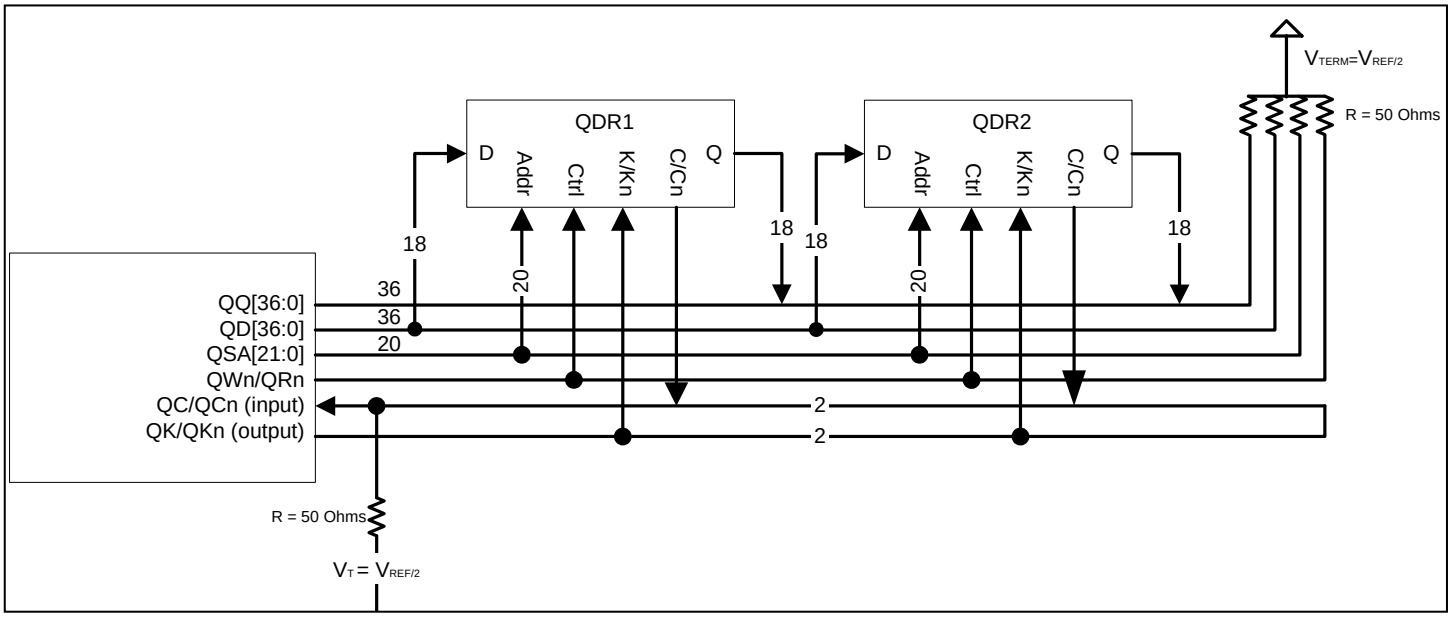


Figure 9:SMT398 QDR Width expansion arrangement.

Constraints File Signal Names

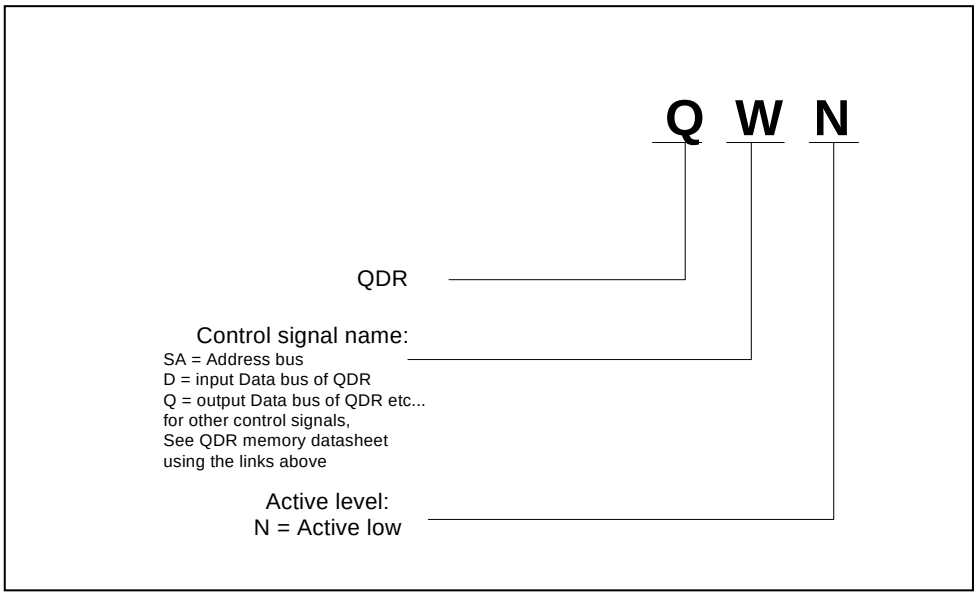


Figure 10: QDR Constraints file signal names

Comports

These communication links follow Texas Instrument C4x standard. They are 8-bit parallel inter-processor ports of the 'C4x processors.

The 398 follows the C40 TIM standard and as such provides 6 links. These are given the numbers 0, 1, 2, 3, 4 and 5. The following figure shows how the 2 configuration Comports (FPGA) are connected on the TIM.

They are guaranteed for a transfer rate of 20MB/s, which could lead, using the 6 Comports available to a 120MB/s transfer rate.

The Comport drives at 3.3v signal levels.

Additional information on the standard is available in the TMS320C4x User's Guide chapter 12: Communication ports and the Texas Instrument Module Specification.

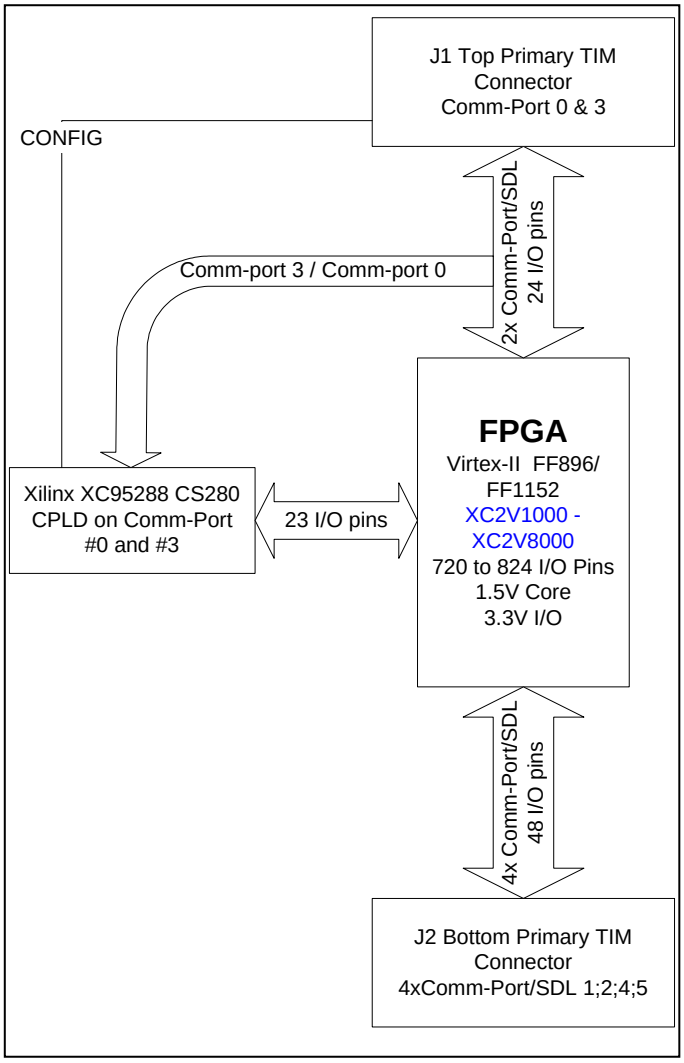


Figure 11:SMT398 Comports connections

Constraints File signal Names

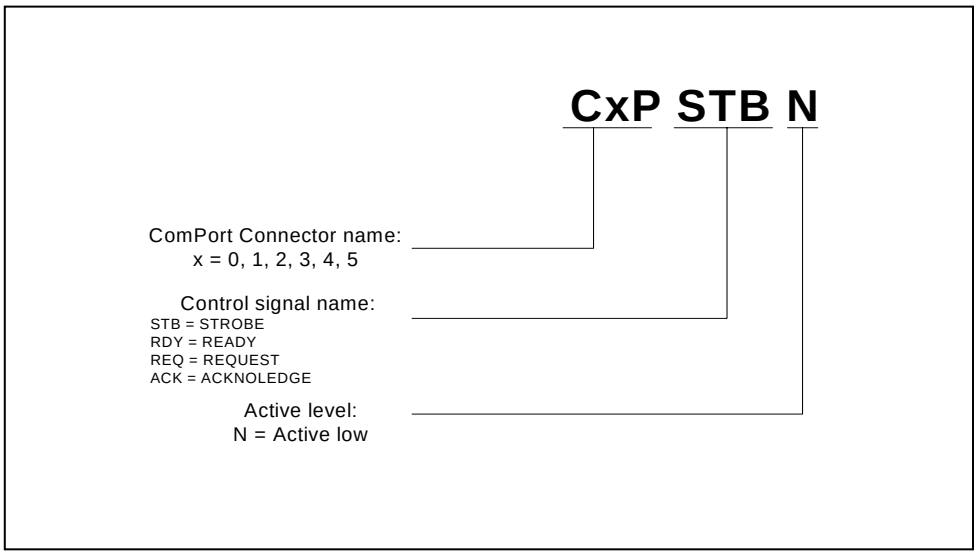


Figure 12: Comport Constraints file signal name

SHB

SHB Connector

The SMT398 includes 4 60-pin connectors to provide SHB communication to the outside world.

The connectors are referenced on the PCB by J8, J9, J10 and J11 (See Figure 19:SMT398 Components placement-Top view).

All 60 pins of a SHB connector are routed to a Virtex II 3000 and above in SMT398 Full configuration.

SMT398s with a smaller Virtex II (1000 to 2000) only provide access to 25 pins per SHB Connector in Basic configuration, which represents the minimum amount required to implement 1 Half Word Interface (Hw). (See SUNDANCE SHB specification and Sundance SDB specification.)

Basic configuration:

J8, J10: pin[1:24]

J9, J11: pin [37:60]

Full configuration:

J8, J9, J10, J11: Pin [1:60]

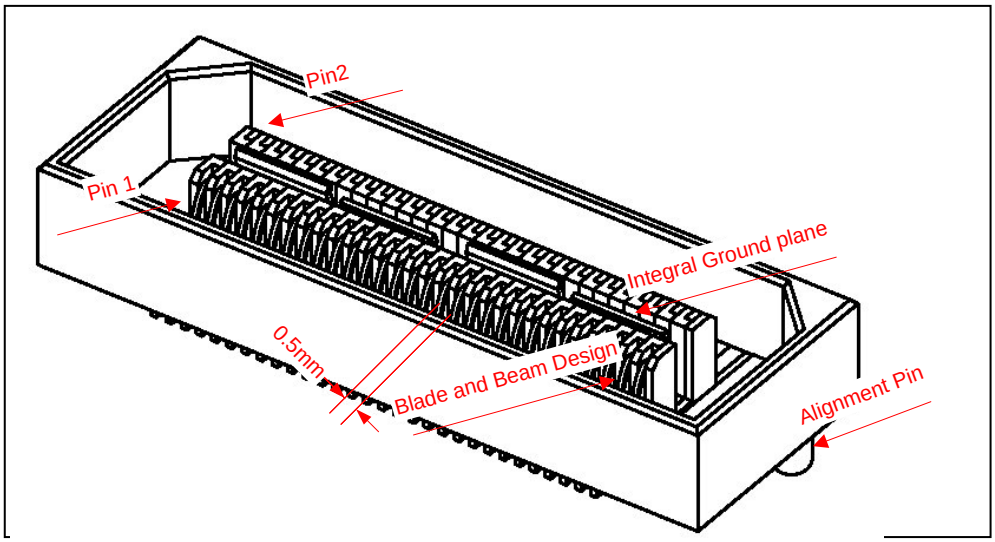


Figure 13: SHB Connector

The bigger the FPGA, the more pins from the SHB Connector become available

Features:

- High-speed socket strip: QSH-030-01-L-D-A-K on the SMT398, mates with QTH-030-01-L-D-A-K
- QTH are used for cable assembly or PCB connecting 2 TIMs.
- Centreline: 0.5mm (0.0197”)
- QSH Connector

An adapter is available for Agilent probes for the 16760A Logic Analyser.

The 2 probes supported are the E5378A 100-pin Single-ended Probe and the E5386A Half Channel Adapter with E5378A.

You can find information on the mechanical and electrical specifications of the probe in the User's Guide available from:

http://www.cos.agilent.com/manuals/pdf/16760705.PDF

Also see page 213 of the Help Volume for the 16760A for specifications:

http://www.cos.agilent.com/manuals/help25/help16760.pdf

SHB Cable Assembly

The cable is custom made by Precision Interconnect and a cable assembly solution builder can be found at: http://www.precisionint.com/tdibrsb/content/howtouse.asp

SHB Inter Modules solutions

High-speed data transfer can be achieved between TIM modules thanks to the use of a 60-way flat ribbon micro-coax cable or via PCB connections.

InterModule PCBs can be found at: Inter Module Connections

As a result, NO DIFFERENTIAL lines are required to transfer data on long distances and at speeds in excess of 100Mhz, which allows the full use of the SHB connector 60 pins.

Half Word Interface (16-bit SHB Interface)

The SHB connectors provide to the FPGA connections to the external world.

You can implement your own interface to transfer data over using these connectors, but if you want to communicate with other Sundance TIM modules, you can implement a Half Word (Hw) interface sitting on 25 pins of an SHB connector.

Then, the SHBs are parallel communication links for synchronous transmission.

An SHB interface is derived from the SDB interface which is a 16-bit wide synchronous communication interface.(SUNDANCE SDB specification)

The differences are:

- The SHB interface can be made Byte (8 bits), Half Word (16 bits) or Word (32 bits) wide.
- The transfer rate can be increased thanks to better quality interconnect.

As an example, let us consider the Half Word (Hw) SHB interface.

In

You can implement 2 x 16-bit SHB interfaces per SHB connector, as per **Table 9,** and have some spare signals for User defined functions. (no differential lines are needed thanks to our SHB cable assembly described in SHB Cable Assembly).

The SMT398 in Full configuration provides 8 Hw SHB interfaces on 4 connectors and can support data rates of 1.6Gbytes/s at 100Mhz

You must refer to the latest SUNDANCE SDB specification for technical information on how it works.

You must make sure to use the SMT6500 package V1.0 and above (which contains the VHDL for it).

Constraint File Signal Names

According to the SUNDANCE SHB specification, 5 Byte-interfaces (from 0 to 4) can be implemented on the 60 pins of a SHB connector. Each Byte interface has its own CLK, WEN, REQ and ACK.

I defined the signal names going from the FPGA to an SHB connector by assuming 2 Hw configurations per SHB connector: Hw0 and Hw1.

So, when in Half Word configuration:

- 16-bit data D(0 to 15)
- CLK0 is borrowed from Byte configuration 0, WEN1, REQ1 and ACK1 are borrowed from Byte configuration 1 to make configuration Hw0 control signals and
- CLK3 is borrowed from Byte configuration 3, WEN4, REQ4 ACK4 are borrowed from Byte configuration 4 to make configuration Hw1 control signals.

The connector names are A, B, C and D with J8 as A, J9 as B, J10 as C and J11 as D. (See Figure 19:SMT398 Components placement-Top view)

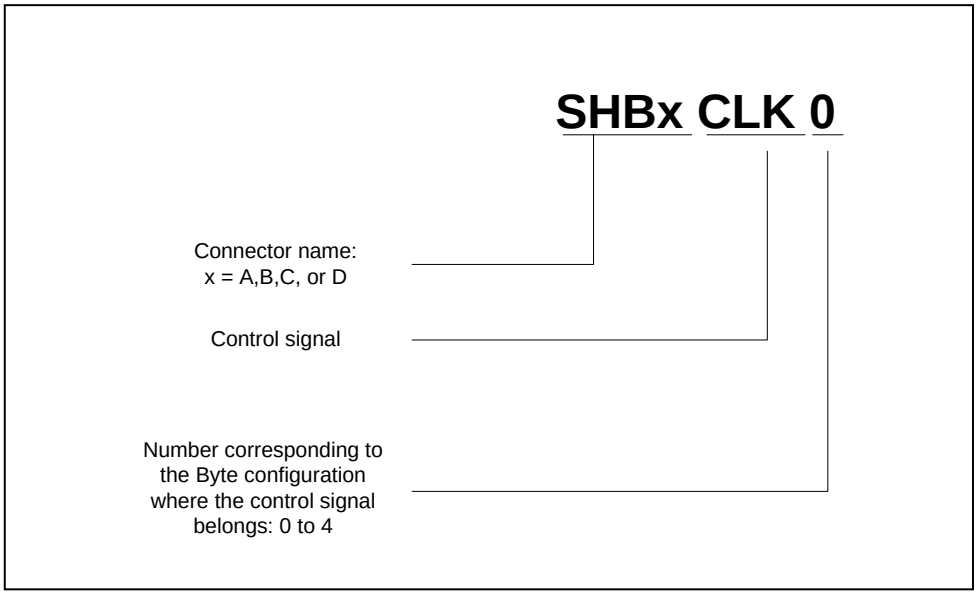


Figure 14: SHB constraints file control signals names.

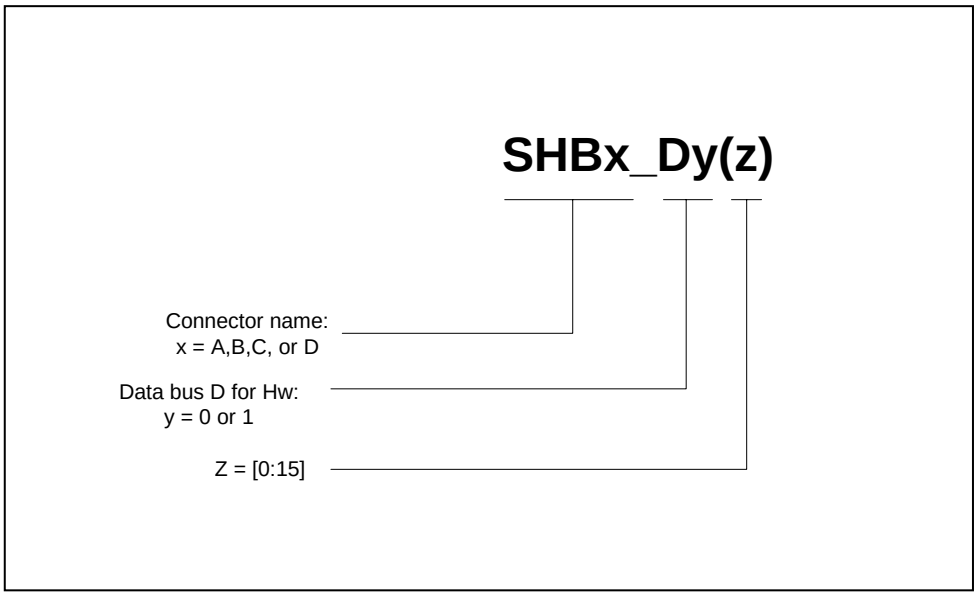


Figure 15: SHB constraints file data signals names

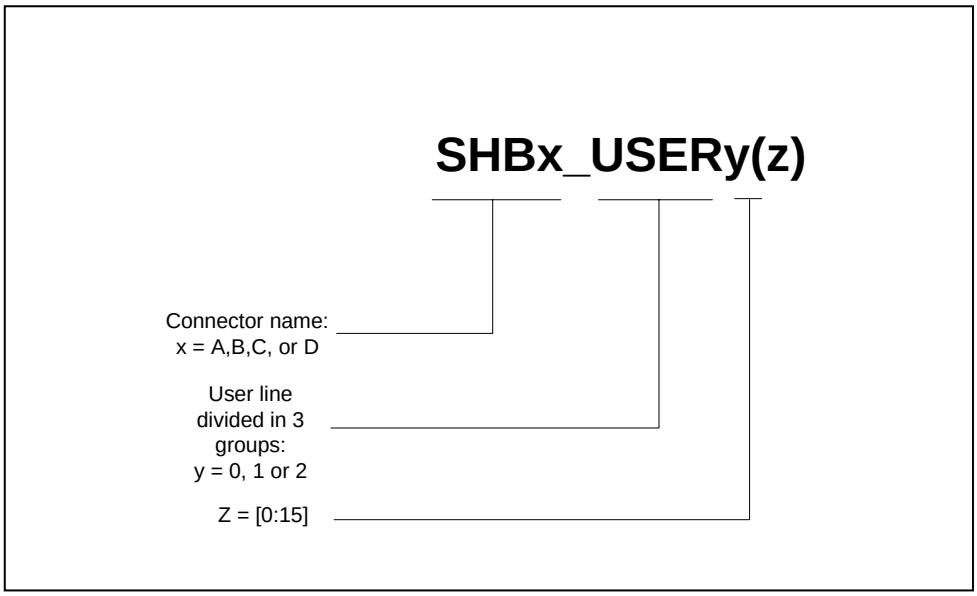


Figure 16: SHB constraints file User pins signals names

Please refer to SHB Header.

Global bus

The global bus is compatible with the TIM standard.

The Global Bus Interface is a memory Interface that follows Texas Instruments' TMS320C4x External Bus operation standard. Additional information on the standard is available in the TMS320C4x User's Guide chapter 9:

External Bus operation.

When Writing, the FPGA sends data across the global bus to the external device.

When Reading, the external device writes data across the global bus to the FPGA.

Constraints File Signals Names

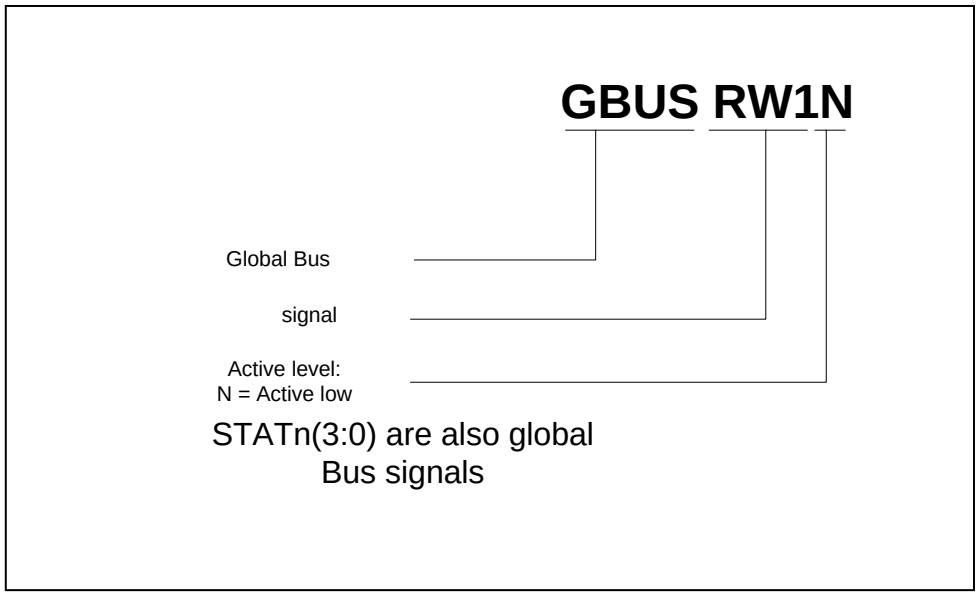


Figure 17: Global Bus constraints file signal names.

Clocks

An on-board oscillator provides a free running clock to the FPGA and CPLD. The default is a 50Mhz oscillator but other frequencies can be provided upon request to Sundance.

An external clock input/outptut is provided to the Virtex II FPGA via a 50 ohms MMBX coax-connector.

These clocks can be de-skewed by the FPGA DCMs or output to other TIMs to synchronise TIMs together.

Description	Specification			
	V input Low	**V output Low**	**V input High**	**V output High**
Maximum voltage	0.8	0.4	3.8	
Minimum voltage	-0.5		2.0	2.4
Impedance	50 Ohms			
Frequency	The Frequency limitations are the ones of the Virtex II part fitted on the SMT398.			

Table 4: External clock specification

Constraints file signal Names

BOARDCLK: On-board oscillator input to the FPGA.

EXT_CLK: External clock input to the FPGA.

Power Supplies

The PCI specifications state that the maximum power allowed for any PCI board is 25 Watts, and represents the total power drawn from all power rails provided at the connector (+5V, +3.3v, +VI/O,+12V,-12V, +3.3Vaux). The expansion board (in our case the TIM carrier board and the TIM modules) may optionally draw all this power from either the +5V or +3.3V rail.
Nevertheless, it is anticipated that many systems will not provide a full 25 Watts per connector for each power rail, because most boards will typically draw much less than this amount.

For this reason it is recommended that you analyse the total FPGA device power drawn by using Xilinx XPOWER before implementing your design in the FPGA.

This will tell you if you need to use the external power connector provided on our carrier boards. (Like the SMT310Q carrier board)

		CPLD XL95288CS280	FPGA XC2V	QDR	ZBT	Oscillator
Vccint/Vdd		3.3v	1.5v	2.5v	3.3v	3.3v
Vcco	LVTLL	3.3v	3.3v	N/A	3.3v	N/A
Vddq	HSTL I	N/A	1.5v	1.5v	N/A	N/A
Vref		N/A	0.75v	0.75v	N/A	N/A
Iref			10uA			

Table 5: powering the devices.

DC/DC converter
PC 3.3v
Voltage regulator

This module must have 5V supplied through the TIM connectors. In addition, a 3.3V supply is required and should be supplied through the TIM mounting holes. This is compatible with the SMT310Q, SMT327 and future Sundance TIM carrier boards.

Contained on the module are a linear regulator for the ‘QDRs and a DC/DC converter for the FPGA.

DC/DC Converter

This module is designed to provide up to 20A of low voltage supply to the FPGA from a single 5V input. The output voltage provided is a Vout of 1.5V.

Current limiting is provided if more than 20 A are drawn out of the DC\DC converter.

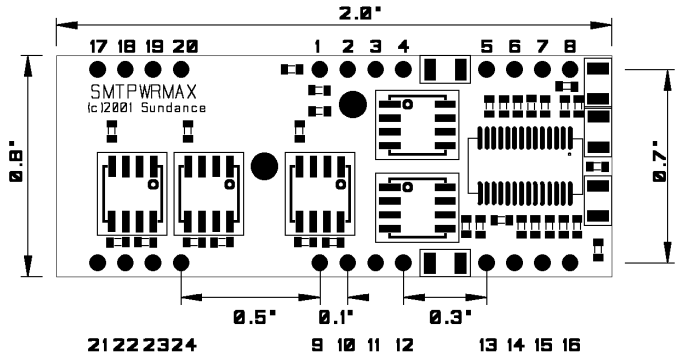


Figure 18: DC/DC converter dimensions (in inches)

Linear Voltage regulator

The QDR core voltage is provided through an adjustable linear voltage regulator from 3.3V.

Fan

A fan coupled with a heat sink can be mounted on the Virtex II to provide heat dissipation but a permanent airflow should always be maintained inbox to provide enough cooling for your system. Please ask Sundance when ordering.

Power Consumption

QDR: 2.5 Watts.

ZBT: 5.544 Watts.

CPLD: 0.2 Watts.

FPGA: depending on the implemented design, the power consumption can reach a maximum of 30 Watts.

Please consider connecting an external power supply to the carrier board. (see 0 for information

Verification Procedures

The specification (design requirements) will be tested using the following:

1) Power module test.
2) FPGA configuration using CPLD and/or JTAG connector.
3) Comport transfers between a SMT376 and the SMT398.
4) ZBT and QDR memory tests.
5) SHB connector Pins Test using SHB tester PCBs.
6) Global Bus transfers between SMT398 and SMT310Q onboard SRAM.(Not yet implemented)
7) External clock I/O tested with scope.

Review Procedures

Reviews will be carried out as indicated in design quality document QCF14 and in accordance with Sundance's ISO9000 procedures.

Validation Procedures

The validation procedure is happening during the verification procedure.

Test that all the memories are accessible by the FPGA as well as all the communication links.

FPGA Constraint File general Information

Because the Virtex FF896 and FF1152 packages are footprint and pinout compatible, the SMT398 offers a high level of flexibility in the choice of the FPGA fitted.

SMT398_896_in_1152_.xls is a spreadsheet showing ALL signal connections for ALL FPGAs that can be fitted on the SMT398.

You can see at a glance which signals are available or not for ALL FPGAs.

It also allows to sort pins automatically by names beginning with, or containing a string etc…using the drop down menus.

This file also shows a particular feature of the SMT398: some signals can be accessed from 2 different pin locations on the FPGA to allow an easier routing of your design. (The duplicate pin is indicated by "name_2"). See Table 6: Duplicate pins

For example, on a XC2V6000, you could use AL33 or W25 to access Z3CS1N.

ff1152	Bank	xc2v8000ff1152 xc2v6000ff1152 xc2v4000ff1152	xc2v3000ff1152	ff896	Bank	xc2v2000ff896	xc2v1500ff896	xc2v1000ff896
H19	0	shba_user0_2<19>/ IO_L83N_0	NOPAD	F17	0	shba_user0_2<19>/ IO_L92N_0	shba_user0_2<19>/ IO_L92N_0	shba_user0_2<19>/ IO_L92N_0
H18	0	shba_user0_2<18>/ IO_L83P_0	NOPAD	F16	0	shba_user0_2<18>/ IO_L92P_0	shba_user0_2<18>/ IO_L92P_0	shba_user0_2<18>/ IO_L92P_0
F11	1	shbb_user0_2<55>/ IO_L60N_1	NOPAD	D9	1	shbb_user0_2<55>/ IO_L52N_1	shbb_user0_2<55>/ IO_L52N_1	shbb_user0_2<55>/ IO_L52N_1
F12	1	shbb_user0_2<54>/ IO_L60P_1	NOPAD	D10	1	shbb_user0_2<54>/ IO_L52P_1	shbb_user0_2<54>/ IO_L52P_1	shbb_user0_2<54>/ IO_L52P_1
Y4	3	Z2CS1N_2/ IO_L83P_3	NOPAD	V2	3	Z2CS1N_2/ IO_L92P_3	Z2CS1N_2/ IO_L92P_3	Z2CS1N_2/ IO_L92P_3
AE16	4	shbd_user0_2<54>/ IO_L80N_4	NOPAD	AC14	4	shbd_user0_2<54>/ IO_L92N_4	shbd_user0_2<54>/ IO_L92N_4	shbd_user0_2<54>/ IO_L92N_4
AE17	4	shbd_user0_2<55>/ IO_L80P_4	NOPAD	AC15	4	shbd_user0_2<55>/ IO_L92P_4	shbd_user0_2<55>/ IO_L92P_4	shbd_user0_2<55>/ IO_L92P_4
AE18	5	shbc_user0_2<18>/ IO_L80N_5	NOPAD	AC16	5	shbc_user0_2<18>/ IO_L92N_5	shbc_user0_2<18>/ IO_L92N_5	shbc_user0_2<18>/ IO_L92N_5
AE19	5	shbc_user0_2<19>/ IO_L80P_5	NOPAD	AC17	5	shbc_user0_2<19>/ IO_L92P_5	shbc_user0_2<19>/ IO_L92P_5	shbc_user0_2<19>/ IO_L92P_5
W25	6	Z3CS1N_2/ IO_L82P_6	NOPAD	U23	6	Z3CS1N_2/ IO_L91P_6	Z3CS1N_2/ IO_L91P_6	Z3CS1N_2/ IO_L91P_6
F34	7	stat_2<0>/ IO_L28P_7	stat_2<0>/ IO_L28P_7	NA	7			
G34	7	stat_2<1>/ IO_L28N_7	stat_2<1>/ IO_L28N_7	NA	7			
F33	7	stat_2<2>/ IO_L22P_7	stat_2<2>/ IO_L22P_7	NA	7			
G33	7	stat_2<3>/ IO_L22N_7	stat_2<3>/ IO_L22N_7	NA	7			
D34	7	GBUS_2H1/ IO_L04P_7	GBUS_2H1/ IO_L04P_7	NA	7			
E34	7	GBUS_2RDY1N/ IO_L04N_7	GBUS_2RDY1N/ IO_L04N_7	NA	7			
D33	7	GBUS_2RW1N/ IO_L01P_7	GBUS_2RW1N/ IO_L01P_7	NA	7			

Table 6: Duplicate pins

The constraints also exist in ASCII files for each FPGA package.

- VII1000.ucf provides the constraints for the FF896 package chips: xc2v1000, xc2v1500 and xc2v2000.
- VII3000.ucf provides constraints for the FF1152 package, xc2v3000 chip
- VII4000.ucf ucf provides constraints for the FF1152 package xc2v6000 and xc2v8000 chips.

Ordering information:

Because the Virtex FF896 and FF1152 packages are footprint and pinout compatible, the SMT398 offers a high level of flexibility in the choice of the FPGA fitted.

The FPGA fitted will influence the amount of usable resources on the board and of course the price.

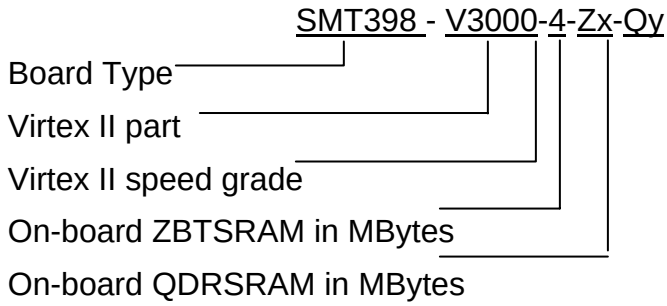
Currently, the SMT398 is available in 2 configurations: Full configuration and Basic configuration.

Full configuration

In the full configuration, a Virtex II 3000, 4000, 6000 or 8000 is used and allows interfacing to ALL the memories and ALL I/Os available on the SMT398.

The SMT398 comes in 3 main full configurations, highlighted in red in Table 7.

The other full configurations options are highlighted in blue in Table 7:



SMT398		Virtex II			
		XC2V3000	XC2V4000	XC2V6000	XC2V8000
ZBT-QDR	Z4-Q2	SMT398-V3000-4-Z4-Q2	SMT398-V4000-4-Z4-Q2	SMT398-V6000-4-Z4-Q2	SMT398-V8000-4-Z4-Q2
	Z4-Q4		SMT398-V4000-4-Z4-Q4	SMT398-V6000-4-Z4-Q4	SMT398-V8000-4-Z4-Q4

Table 7: Virtex II, ZBT/QDR combinations in FULL configuration

The ZBT RAM also comes as Z2, Z8 and Z16 on the board.

Basic configuration

In the basic configuration, a Virtex II 1000, 1500, or 2000 is used and allows interfacing to part of the memories and I/Os available on the SMT398.

Memories

- Only 2 Banks of ZBT RAM are available to the FPGA. The total amount of ZBT on board shown in Table 8 is to be divided amongst these 2 banks.
- No QDR available.

SHBs

- 25 I/Os per SHB connectors are available to allow the implementation of up to 4x16-bit SDB interfaces.

Comports

- 5 Comports are available with one (Comport 3) reserved for the FPGA configuration (remains not connected to the FPGA after configuration)

Global Bus

- 1 Global Bus

External Clock

- 1 External clock I/O.

SMT398		Virtex II		
		XC2V1000	XC2V1500	XC2V2000
ZBT	Z2	SMT398-V1000-4-Z2	SMT398-V1500-4-Z2	SMT398-V2000-4-Z2
	Z4	SMT398-V1000-4- Z4	SMT398-V1500-4- Z4	SMT398-V2000-4- Z4
	Z8	SMT398-V1000-4- Z8	SMT398-V1500-4- Z8	SMT398-V2000-4- Z8

Table 8: Virtex II, ZBT combinations in BASIC configuration

PCB Layout Details

Components placement

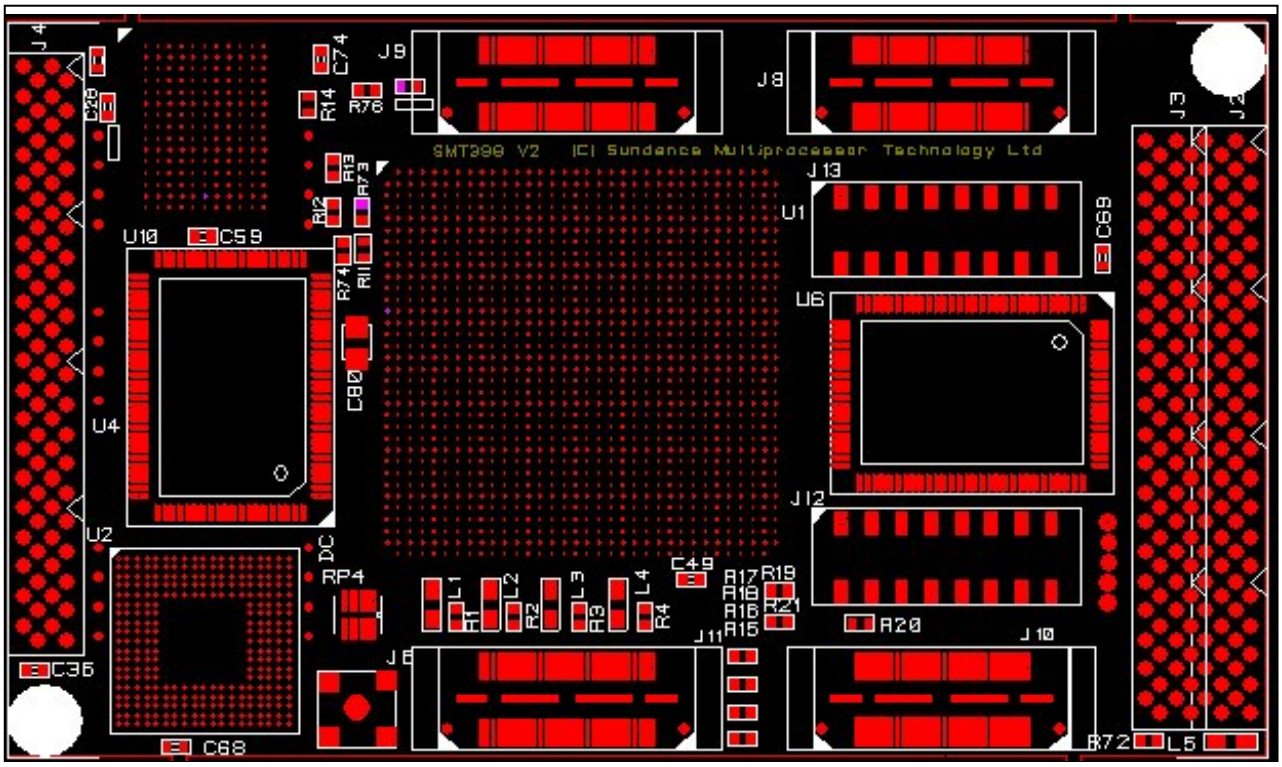


Figure 19:SMT398 Components placement-Top view

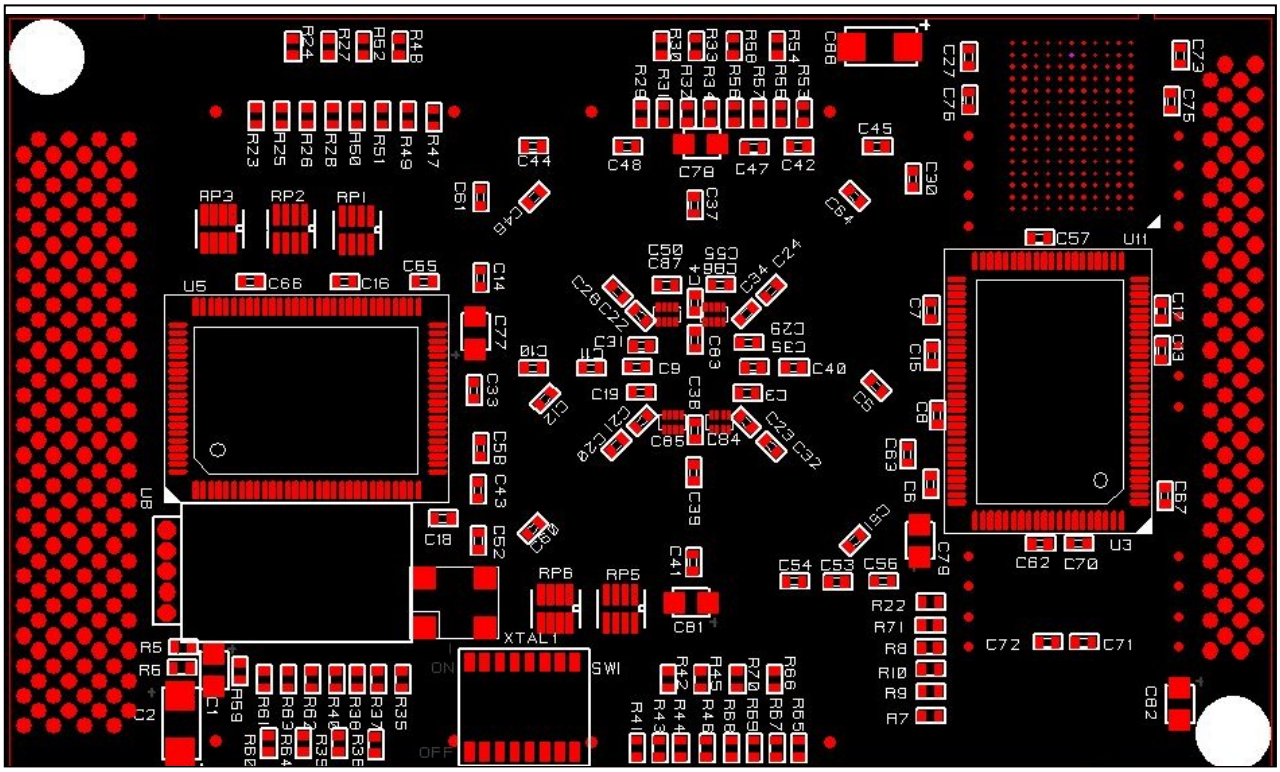


Figure 20: SMT398 Components placement-Bottom view

U1 : Xilinx FPGA

U2: Xilinx CPLD

U3: ZBTRAM Bank1

U4: ZBTRAM Bank2

U5: ZBTRAM Bank3

U6: ZBTRAM Bank4

U10: QDR Bank1

U11: QDR Bank2

XTAL1: Onboard oscillator

J6: (Top view, bottom left corner), External clock input connector

These 2 Banks share the same address lines (See

Figure 9:SMT398 QDR Width expansion arrangement.)

Headers Pinout

SHB Header

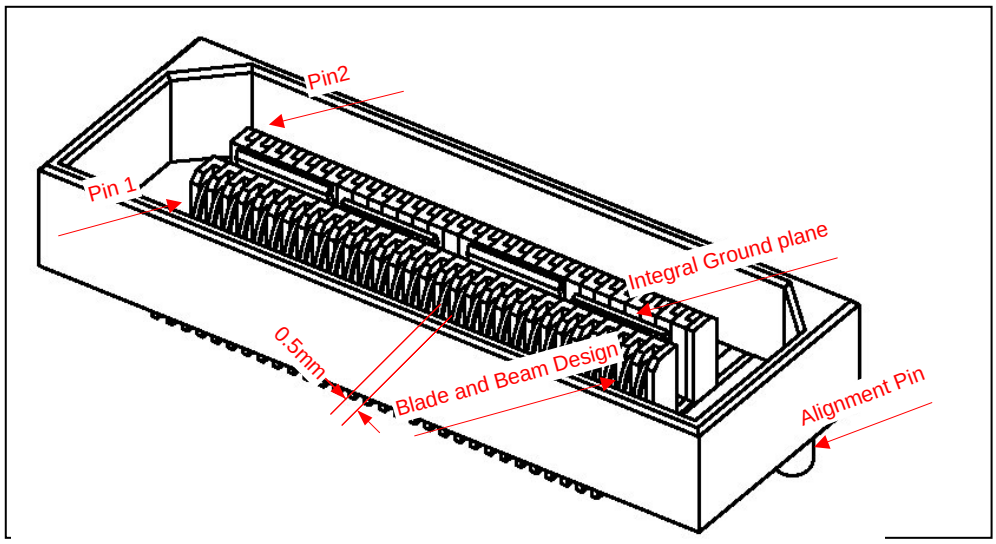


Figure 21: Top View QSH 30

SHB Pinout (LVTTL only).(J8-J9-J10-11)

In the constraints file provided for the SMT398 FPGA, the SHB signals have been named to match 2 16-bit SDB interfaces (or Hw SHB interface) pinout according to the SUNDANCE SHB specification Half Word configuration.

	Hw	QSH Pin number	QSH Pin number		Hw
Hw0	SHBxCLK0	1	2	Hw0	SHBxD0(0)
	SHBxD0(1)	3	4		SHBxD0(2)
	SHBxD0(3)	5	6		SHBxD0(4)
	SHBxD0(5)	7	8		SHBxD0(6)
	SHBxD0(7)	9	10		SHBxD0(8)
	SHBxD0(9)	11	12		SHBxD0(10)
	SHBxD0(11)	13	14		SHBxD0(12)
	SHBxD0(13)	15	16		SHBxD0(14)
	SHBxD0(15)	17	18		SHBxUSER0(16)
	SHBxUSER0(17)	19	20		SHBxUSER0(18)
	SHBxUSER0(19)	21	22		SHBxWEN1
	SHBxREQ1	23	24		SHBxACK1
	SHBxUSER1(23)	25	26		SHBxUSER1(24)
	SHBxUSER1(25)	27	28		SHBxUSER1(26)
	SHBxUSER1(27)	29	30		SHBxUSER1(28)
	SHBxUSER1(29)	31	32		SHBxUSER1(30)
	SHBxUSER1(31)	33	34		SHBxUSER1(32)
	SHBxUSER1(33)	35	36		SHBxUSER1(34)
Hw1	SHBxCLK3	37	38	Hw1	SHBxD1(0)
	SHBxD1(1)	39	40		SHBxD1(2)
	SHBxD1(3)	41	42		SHBxD1(4)
	SHBxD1(5)	43	44		SHBxD1(6)
	SHBxD1(7)	45	46		SHBxD1(8)
	SHBxD1(9)	47	48		SHBxD1(10)
	SHBxD1(11)	49	50		SHBxD1(12)
	SHBxD1(13)	51	52		SHBxD1(14)
	SHBxD1(15)	53	54		SHBxUSER2(52)
	SHBxUSER2(53)	55	56		SHBxUSER2(54)
	SHBxUSER2(55)	57	58		SHBxWEN4
	SHBxREQ4	59	60		SHBxACK4

Table 9: SHB interfaces table.

16-bit interface

JTAG/Multilinx headers

The JTAG/Multilinx headers have the following pinout:

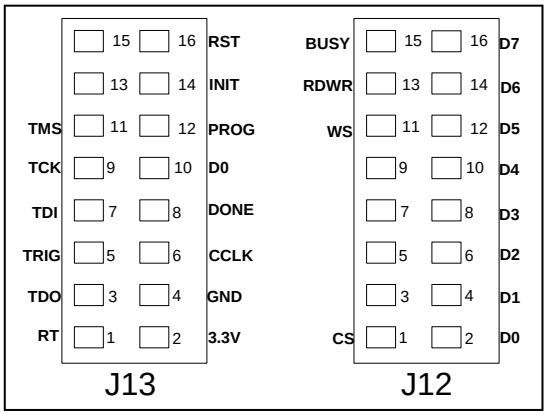


Figure 22: Top View of JTAG/Multilinx headers

JTAG/Boundary scan pinout (J13)

Name	Pin	Function	Connections
VCC	2	Power. Supplies VCC (3.3V, 10 mA, typically) to the cable.	To target system VCC
GND	4	Ground. Supplies ground reference to the cable.	To target system ground
TCK	9	Test Clock. This clock drives the test logic for all devices on boundary-scan chain.	Connect to system TCK pin.
TDO	3	Read Data. Read back data from the target system is read at this pin.	Connect to system TDO pin.
TDI	7	Test Data In. This signal is used to transmit serial test instructions and data.	Connect to system TDI pin.
TMS	11	Test Mode Select. This signal is decoded by the TAP controller to control test operations.	Connect to system TMS pin.

Table 10: Connector J13-JTAG Header

MultiLINX SelectMap Pin Descriptions (J12-J13)

Signal Name	Pin	Function
PWR	2	*Power.* Supplies VCC to cable (Works at multiple voltages 5V, 3.3V, and 2.5V).
GND	4	*Ground.* Supplies ground reference to cable.
CCLK	6	*Configuration Clock* is the configuration clock pin, and the default clock for readback operation.
DONE (D/P)	8	*Done/Program.* Indicates that configuration loading is complete, and that the start-up sequence is in progress.
PROG	12	*Program.* A Low indicates the device is clearing its configuration memory. Use the Active Low signal to initiate the configuration process.
INIT	14	*Initialize.* Initialization sequencing pin during configuration (indicates start of configuration). A logical zero on this pin during Configuration indicates a data error.

Table 11: Connector J13-Flying Lead Set #1

D0-D7	2,4,6,8 10,12, 14,16	*Data Bus* — This pin is used for Virtex SelectMAP Mode. An 8-bit data bus supporting the SelectMAP and Express configuration modes.
CS0 (CS)	1	*Chip Select* — CS on the Virtex. The CS0/CS pin represents a chip select to the target FPGA during configuration.
RS (RDWR)	13	*Read Select* — The RS pin represents Read Select control for the Asynchronous Peripheral configuration mode. *Read/Write* — The RDWR pin is used as an active high READ and an active low WRITE control signal to the Virtex FPGA.
RDY/BUSY	15	*Busy Pin* — Busy pin on the Virtex.

Table 12: Connector J12 Flying Lead Sets 3&4

Safety

This module presents no hazard to the user.

EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.