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Product Specification for SMT6058

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Revision History

Issue	Changes Made	Date	Initials
1.0	First release	03.12.08	SM
1.1	Added: RSL registers	03.02.09	SM

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1 Introduction

This document specifies the requirements for the SMT6058 software board support package.

The SMT6058 product will allow accessing the SMT148-FX60 carrier boards via its Gigabit Ethernet port (onboard RJ45 connector). The SMT6058 includes a software TCP/IP stack for the Gigabit Ethernet interface, a default firmware implementing a PowerPC core for the Virtex-4 FX60 FPGA device, the software functions to access the board resources (flash programming) and on-board modules via Rocket-IO Serial Links and/or Comport link from the gigabit Ethernet port (TCP/IP stack).

The SMT6058 is provided with a set of reference design examples, full documentation and user manual/help file.

2 Related Documents

2.1 Referenced Documents

SMT6048 help file

SMT6048 software package

SMT148-FX User Manual

2.2 Applicable Documents

3 Acronyms, Abbreviations and Definitions

3.1 Acronyms and Abbreviations

TIM Texas Instruments Module

3.2 Definitions

N/A

4 Functional Description

The SMT6058 allows to interface to the SMT148-FX60 standalone carrier board to a host computer via the Gigabit Ethernet port.

4.1 Block Diagram

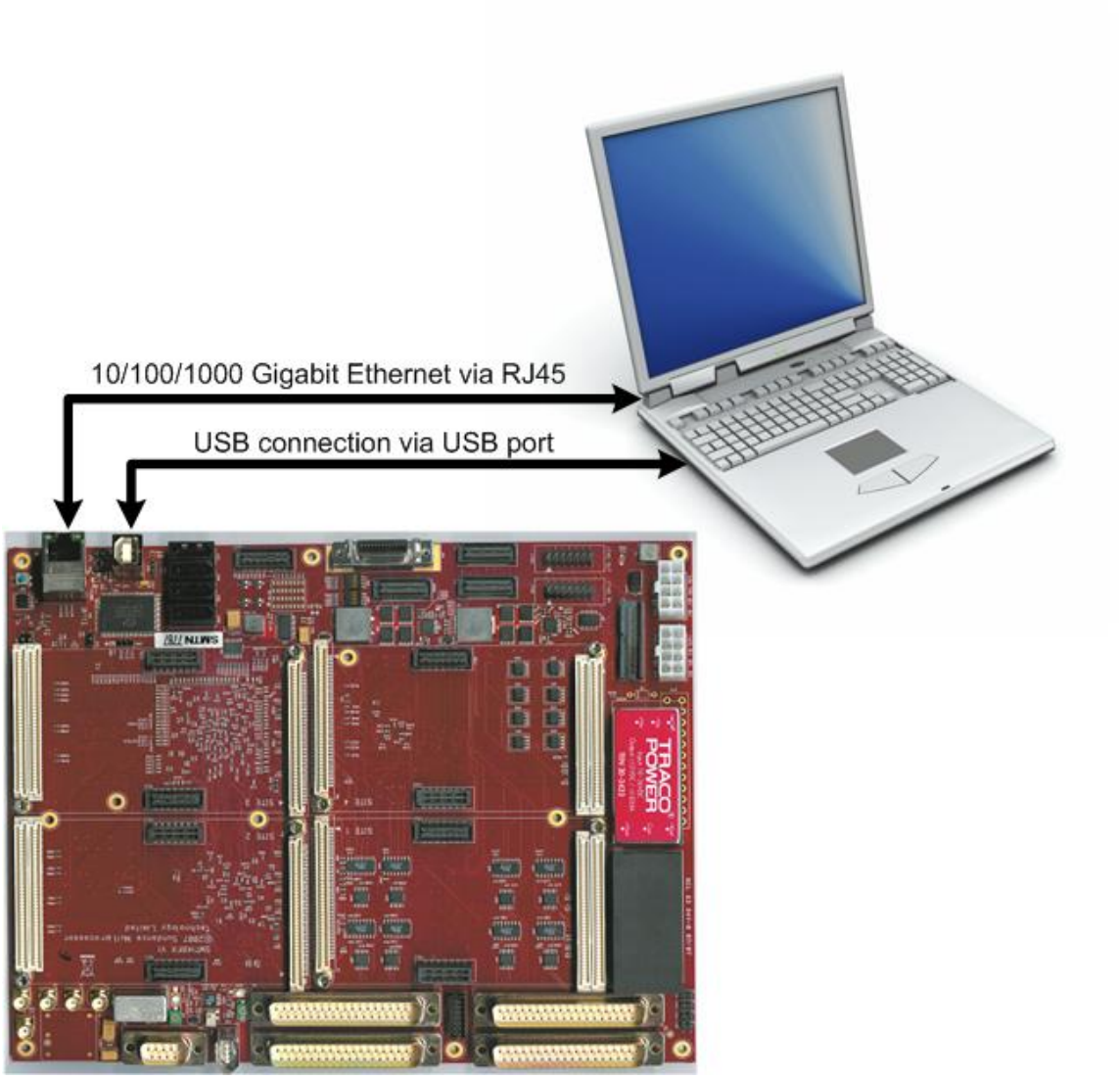

Figure 1: System architecture

A computer can be connected to the SMT148-FX60 standalone carrier board via:

- USB port using the SMT6048 software product,
- RJ45 port using the SMT6058 software product.

The software products allow to send/receive data between the SMT148-FX and a device/computer.

4.2 SMT6058 Description

The Gigabit Ethernet application will be implemented using Xilinx EDK 10.1 and the included FPGA IP cores. It should be possible to generate a bitstream file out of the EDK project which allows to do software debugging in the Virtex-4 FX60's embedded PowerPC processor core. It should be also possible to generate a 3L Diamond application from the project netlist.

The objective of the task is to be able to send and receive Ethernet packets through the Gigabit Ethernet interface in the SMT148-FX60 carrier board. The data is generated and received in the embedded PowerPC processor core. The application should allow to communicate from an external device/computer connected to the Ethernet port (RJ45 connector).

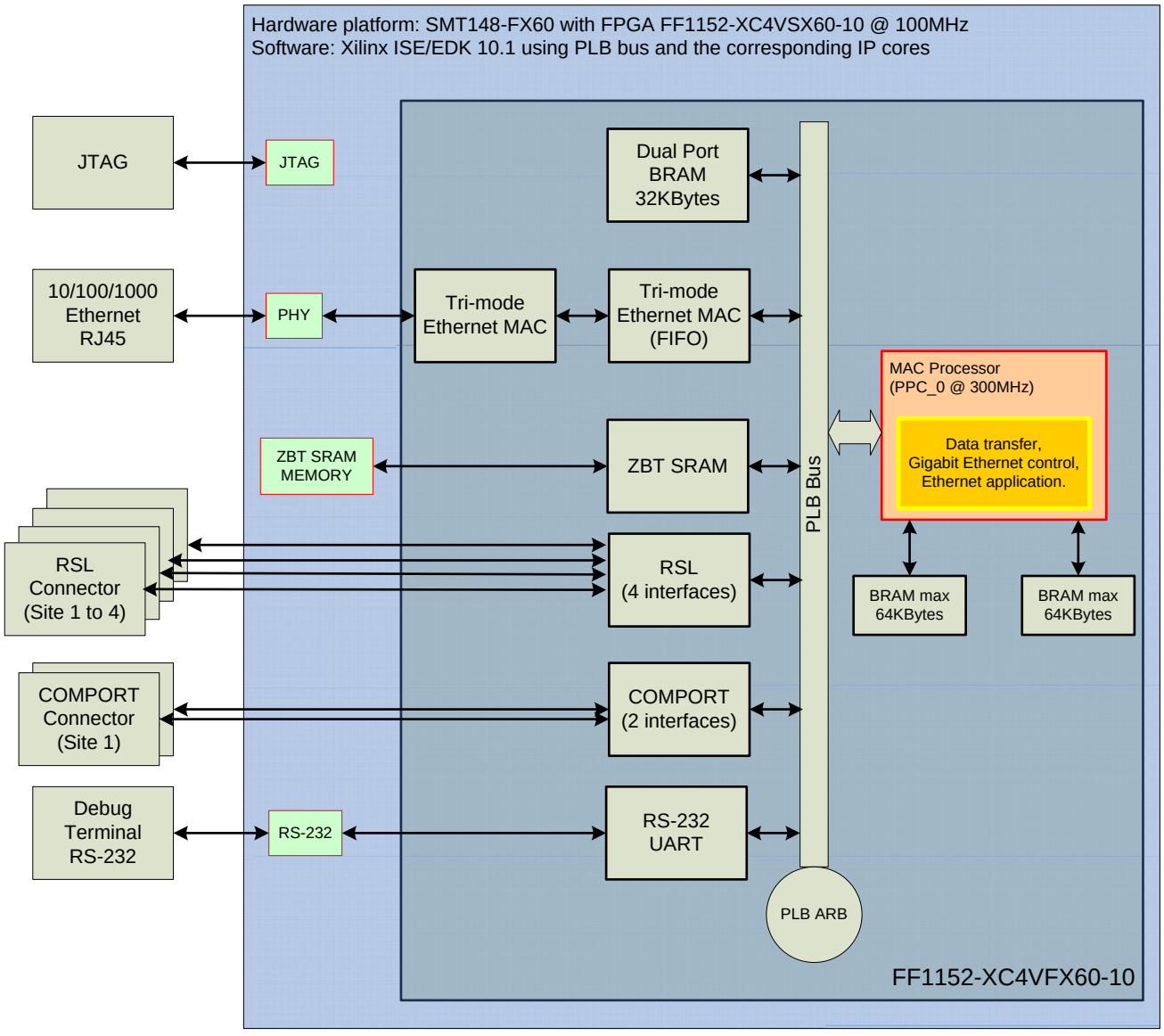

Figure 2: Task description

All required parameters to setup the Gigabit Ethernet interface including the register settings for the TMAC and MARVEL (88E1116-xx-NNC1C000) chipset should be configurable (accessible) from the software running on the PowerPC processor core. There should be an assumption on 'default' or 'after reset' settings to have the SMT148 FX60 board in a mode where the Gigabit Ethernet port is running.

The Gigabit Ethernet interface should work in the 1000Mbps mode, both half and full duplex. The Gigabit Ethernet should be accessible via a low-weight TCP/IP stack.

DMA engine facilities have to be planned to access the Ethernet.

4.3 Interface Description

4.3.1 Software Functions

All the SMT6048 software functionalities should be ported to the SMT6058 TCP/IP Stack. Refer to the SMT6048 Help File for more details.

4.3.2 Note about the Flash access

The on-board Flash memory located on the SMT148-FX60 shall be used to store the firmware for the PowerPC as well as a 'bootloader' built-into the canned netlist that can accept a program from:

- FLASH,
- Comport,
- Ethernet.

The SPANSION Flash memory (S29GL256N11TF or S29GL256M11TF) has a total capacity of 256Mbits.

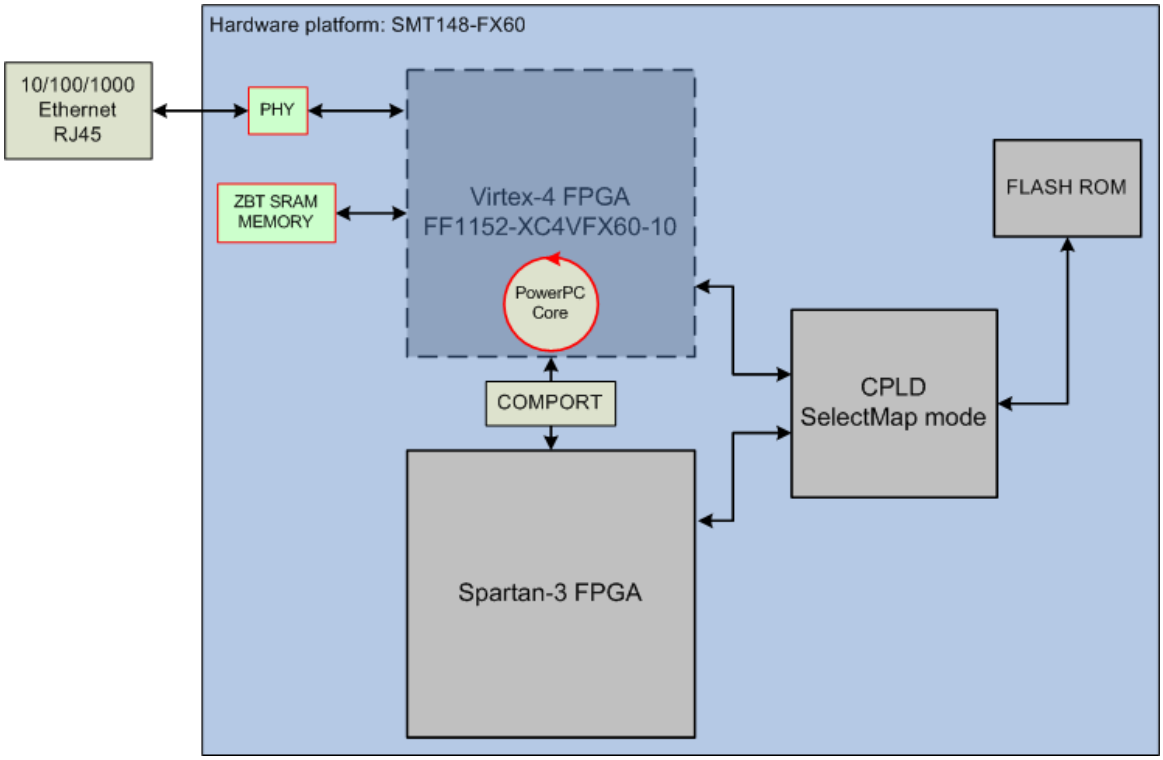

Figure 3: Flash access from the PowerPC (XC4VFX60)

The PowerPC should access the Flash memory to read or write some data into.

For a Write command, two control words should be sent:

- 1st word: address where will be located the data written in Flash memory and the control command 'Write'
- 2nd Word: send the Data to write into the Flash memory

For a Read command, one control word should be sent:

- Read at the correct address and then the data is available on the Comport. The Power PC needs to read the value stored in the Comport FIFO.

The Comport interface has many control flags that should be monitored like FULL and EMPTY FLAGS. Refer to the SMT6400 help file for the description.

4.3.3 Note about the ZBT SRAM

The ZBT SRAM (K7N321801M) is organised into two banks of 2Mx18-bit, offering a total capacity of 9Mbytes. Note that only 8Mbytes are available for the user. The memory controller provided by Xilinx MIG (Memory Interface Generator) is used.

The PowerPC should access the ZBT SRAM memory to read or write some data into.

For a Write command, two control words should be sent:

- 1st word: address where will be located the data written in ZBT SRAM memory and the control command 'Write'
- 2nd Word: send the Data to write into the ZBT SRAM memory

For a Read command, one control word should be sent:

- Read at the correct address and then the data is available on PLB bus. The Power PC needs to read the value from the PLB bus.

The ZBT SRAM memory is accessible from the address: TBB to the address: TBD

DMA engine facilities have to be planned to access the ZBT SRAM.

4.3.4 Note about the RSL and Comport interfaces

The SMT148-FX60 FPGA shall be accessed by its base address. The FPGA base address is the pointer to map all the communication resources and interfaces needed to a specific address. The SMT148-FX60 base address is: TBD.

The SMT148-FX60 offers 2 RSL links per module site on the SMT148-FX standalone carrier board. The RSL is a communication link sustaining 250Mbytes/s per link. The RSL are directly connected from the Virtex-4 FX60 FPGA to each of the module sites.

This table gives the offset address to add to the base address to access the RSL communication links:

Resource	Offset
RSL_CSR for RSL 0 (TIM site 1)	0x00108000
RSL_CSR for RSL 1 (TIM site 1)	0x00118000
RSL _CSR for RSL 3 (TIM site 2)	0x00138000
RSL _CSR for RSL 4 (TIM site 2)	0x00148000
RSL_CSR for RSL 5 (TIM site 3)	0x00158000
RSL_CSR for RSL 6 (TIM site 3)	0x00168000
RSL _CSR for RSL 8 (TIM site 4)	0x00188000
RSL _CSR for RSL 9 (TIM site 4)	0x00188000
RSL _DAT for RSL 0 (TIM site 1)	0x00100000
RSL _DAT for RSL 1 (TIM site 1)	0x00110000
RSL _DAT for RSL 3 (TIM site 2)	0x00130000
RSL _DAT for RSL 4 (TIM site 2)	0x00140000
RSL _DAT for RSL 5 (TIM site 3)	0x00150000
RSL _DAT for RSL 6 (TIM site 3)	0x00160000
RSL _DAT for RSL 8 (TIM site 4)	0x00180000
RSL _DAT for RSL 9 (TIM site 4)	0x00190000

Table 1: FPGA memory map for RSL communication links

Note: The layout of the RSL registers is the same as for the SDB registers. See the SMT6400 Help File for more details.

There are 3 Comports connected between the Spartan-3 and the Virtex-4 FX60. One is reserved to interface to the on-board Flash memory (via the Spartan-3 FPGA device), another one is used to interface the embedded PowerPC processor core to the SMT148 FX60 module site 1.

This table gives the offset address to add to the base address to access the Comport communication links:

Resource	Offset
CP_CSR for comport 0 (Flash access)	0x00004000
CP_CSR for comport 1 (Not used)	0x0000C000
CP_CSR for comport 3 (USB access)	0x0001C000
CP_CSR for comport 4 (TIM site 1)	0x00024000
CP_DAT for comport 0 (Flash access)	0x00000000
CP_DAT for comport 1 (Not used)	0x00008000
CP_DAT for comport 3 (USB access)	0x00018000
CP_DAT for comport 4 (TIM site 1)	0x00020000

Table 2: FPGA memory map for COMPORT communication links

Note: *Comports 0, 1 and 2 are transmitters at 'Reset' and Comports 3, 4 and 5 are receivers at 'Reset'.*

For a Write command, two control words should be sent:

- 1st word: address where will be located the data written in the RSL/Comport FIFO and the control command 'Write'
- 2nd Word: send the Data to write into the RSL/Comport FIFO

For a Read command, one control word should be sent:

Read at the correct address for the relevant data register when a FIFO flag not empty is triggered. The Power PC needs to read the value from the PLB bus.

DMA engine facilities have to be planned to access the RSL and Comport.

5 Verification Procedures

5.1.1 Performance

This test shall display the minimum, maximum and average speed rates reached by the communication link over the Gigabit Ethernet port for Read and Write accesses.

5.1.2 Web server

This test is the control board to access the SMT148 FX60 via the Gigabit Ethernet port. It allows to:

- Access the Flash (Read/Write),
- Read data packets from the Gigabit Ethernet port using the TCP/IP stack:
    - Read one single word,
    - Read a buffer of words.
- Write data packets to the Gigabit Ethernet port using the TCP/IP stack:
    - Write one single word,
    - Write a buffer of words.
- Access several carrier boards

Note: the Virtex-4 FX60 shall be first configured from Flash to have the adequate firmware with the PowerPC implementation running prior to using the Gigabit Ethernet port.

6 Review Procedures

TBD

7 Validation Procedures

TBD

8 Deliverables

The SMT6058 includes software functions and FPGA firmware delivered as a netlist.

9 Distribution

The SMT6058 is delivered to customers as an installer for Windows 32-bit version.

10 Warranty

90 days after purchase of the SMT6058 software package.

11 Support Packages

SMT6058 support package.