Unit / Module Description:	PXIe FPGA board
Unit / Module Number:	SMT700
Document Issue Number:	1.5
Issue Date:	20th November 2009
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Product Specification for SMT700

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Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	20/7/07	GKP
1.1	Minor updates.	1/8/07	GKP
1.2	Added RJ45.	4/9/07	GKP
1.3	Update of board layout diagrams.	17/3/08	GKP
1.4	Clarification of fibre module provision.	18/3/09	GKP
1.5	Correction of DDR speed.	20/11/09	GKP
1.6	Updated block diagram to add second SHB	7/6/10	CH

Table of Contents

1 Introduction

The SMT700 is a Virtex 5 based PXIe board.

Main features (maximum configuration):

- Xilinx Virtex 5 in an FF1136 package. Supports LX50T/LX85T/SX50T or LX110T/SX95T.
- FPGA configuration from 64MByte flash using a Xilinx Coolrunner CPLD.
- One 64-bit wide data bank of DDR2 memory. The bank uses 4 16-bit wide devices. Running this memory at 175MHz provides a maximum access speed of over 2.8Gbyte/s.
- Sundance LVDS Bus (SLB) connector.
- Front panel SATA connectors carrying Virtex5 serial interfaces.
- Front panel RJ45 for gigabit Ethernet.
- Front panel Fibre Optic modules carrying Virtex5 Serial interfaces.
- Sundance RSL connector with 4 serial interfaces.
- Front panel USB interface to allow re-programming of the flash memory.

2 Related Documents

Sundance RSL specification (hyperlink).

Xilinx Virtex5 datasheets (hyperlink).

3 Acronyms, Abbreviations and Definitions

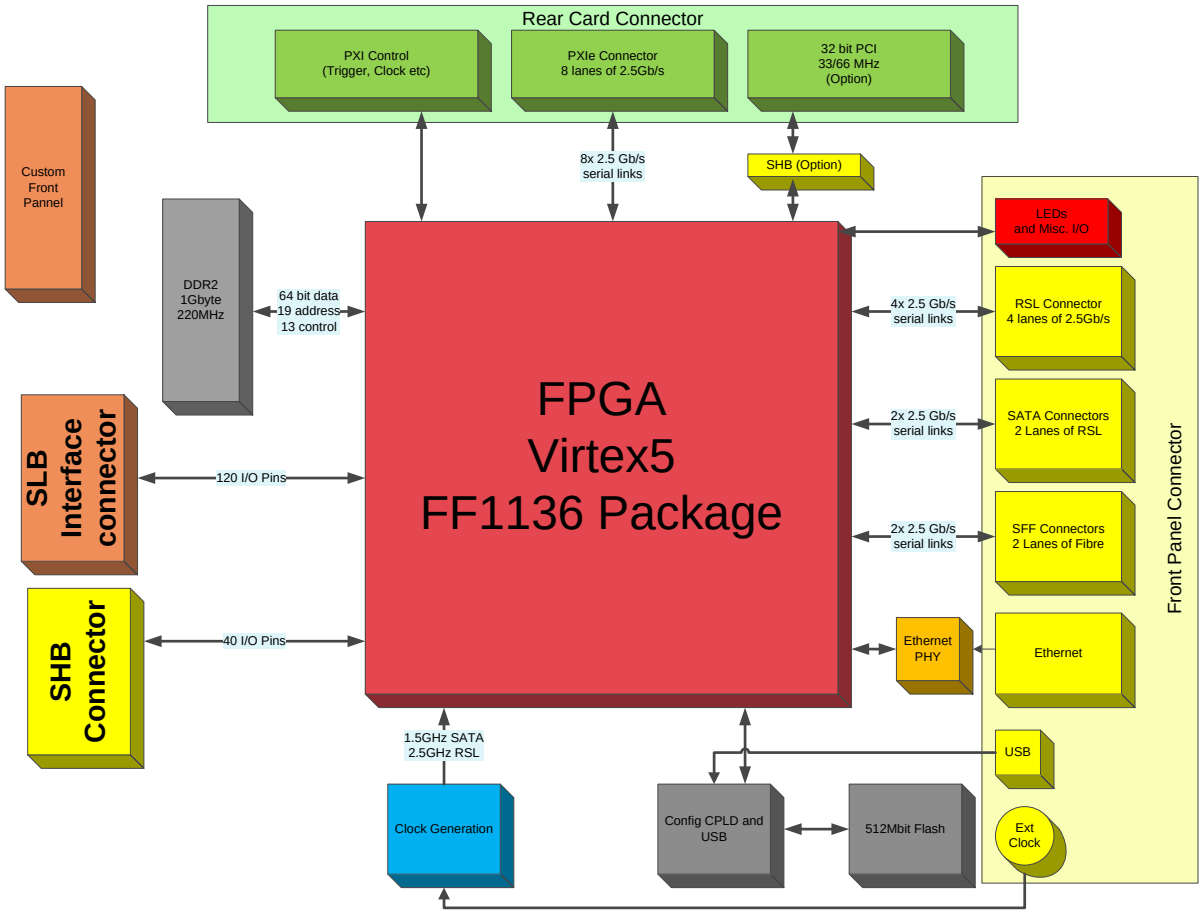
A list of acronyms etc (hyperlink).

MGT, GTP, RSL are all used (interchangeably) and refer to the FPGA's high speed serial links.

4 Functional Description

The major elements of the SMT700 are shown in the block diagram below.

4.1 Block Diagram



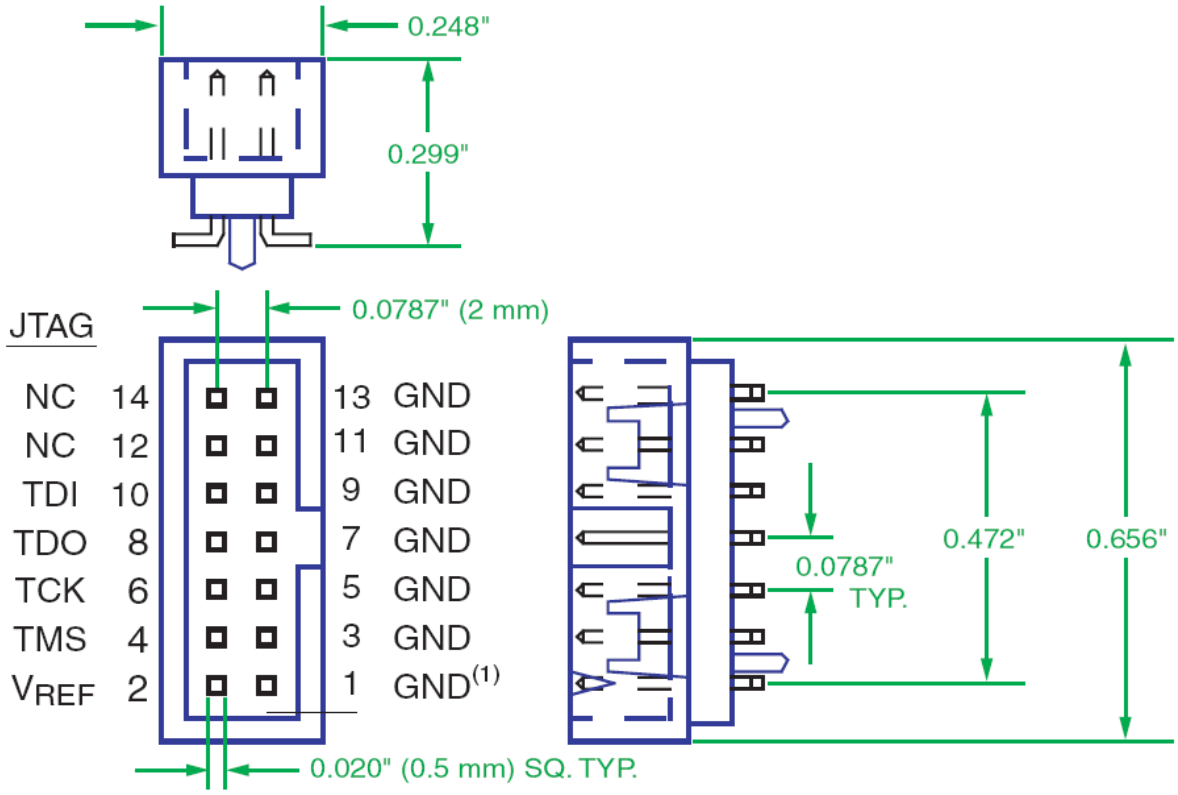
4.2 Module Description

4.2.1 FPGA

The SMT700 module uses a Xilinx Virtex 5 LXT or SXT to implement the interfaces the board provides.

Configuration of the FPGA is from one of two sources; on-board flash memory or Xilinx JTAG header.

A connector is specifically dedicated for FPGA and CPLD detection and programming. Both the CPLD and the FPGA are part of the JTAG chain. A 14-position (2x7) connector (2mm) is available and shows TDI, TDO, TCK and TMS lines, as well as a Ground and a reference voltage, as shown below:



This connector has been chosen because it can connect easily to a Xilinx Parallel IV cable using the ribbon cable provided by Xilinx.

The connector is a Molex part: Molex 87831-1428.

4.2.2 SLB Connector

An SLB connector provides a base for a wide range of Sundance analog modules.

This connector is mounted on the reverse side of the board. The SMT700 occupies two slots in a rack with the board itself residing on the central card guides (i.e. there will be a whole slot width for the FPGA, memory etc, and another slot with the SLB mezzanine. This approach will greatly improve thermal design issues, whilst still remaining within the relevant backplane specifications.

4.2.3 DDR2

Four devices are used to implement this memory.

A 175MHz 64-bit data bus is used to transfer data at over 2.8Gbyte/s. (Xilinx provides performances of a DDR2 interface as being: 200MHz for a -1 part, 267MHz for a -2 part and 333MHz for a -3 part.)

4.2.4 Front Panel Fibre Optic Modules

Two FPGA serial interfaces are presented here using Stratos Lightwave 568-LTK-LT12-H modules.

These interfaces support 2.5Gb/s operation.

Note that only one device is fitted as standard due to the fact that the second module fits on the reverse of the SMT700 PCB. Not all variations of the SMT7xx series can support two modules.

4.2.5 Front Panel RJ45 Connector (Ethernet)

A single RJ45 connector provides a 10/100/1000 Ethernet interface. The RJ45 connects directly to a Marvell 88E1116 PHY, which is interfaced to the FPGA.

4.2.6 Front Panel SATA Connectors

Two SATA-style connectors are provided on the front panel. Each connector carries a single FPGA serial interface. As standard, these interfaces do NOT provide SATA connectivity.

4.2.7 RSL

The LXT/SXT series devices from Xilinx provide up to 16 high speed (>3Gbps) serial links.

The SMT700 connects 8 links to the PXIe connector, 4 links to an RSL connector, two links to Fibre Modules sites, and two links to front panel SATA connectors.

For FPGAs with only 12 GTPs (high speed serial ports), no links are available on the RSL connector.

4.2.8 Flash

This 64Mbyte memory contains configuration code for the FPGA.

The flash contents may be programmed via the PXIe/PCI interface or via USB.

4.2.9 CPLD and FPGA Configuration

This Xilinx CPLD is capable of configuring the FPGA using data provided from the flash memory.

The CPLD also interfaces to a Cypress USB device. This interface allows easy upgrading of the FPGA configuration stored in flash.

The USB mechanism to re-program the flash is always present and does not rely on the FPGA being configured. This can be advantageous if the FPGA configuration has been updated with a non-working PCI interface.

4.2.10 SHB

Two Sundance SHB connectors are fitted as standard. Each connector has the ability to carry a 32-bit data bus with a data rate of 133MHz. A dual 16-bit interface option is also supported.

One SHB is connected directly to the FPGA. The second SHB shares the PCI interface signals. For this reason, this SHB interface and the PCI cannot be operated simultaneously.

4.2.11 LEDs

Two front panel LEDs are available and connected directly to the FPGA.

5 PXI Pinout

5.1 PXI Express Hybrid Connectors

The SMT700 is a PXI Express Hybrid Peripheral Module, a 3U card with 2 PXI connectors, XP4 and XP3 or P1. The following table shows their pinouts.

Pin	Z	A	B	C	D	E	F	
1	GND	GA4	GA3	GA2	GA1	GA0	GND	XP4 / XJ4 Connector
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND	
3	GND	12V	12V	GND	GND	GND	GND	
4	GND	GND	GND	3.3V	3.3V	3.3V	GND	
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND	
6	GND	PXI_TRIG2	GND	ATNLED	PXI_STAR	PXI_CLK10	GND	
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND	
8	GND	RSV	GND	RSV	PXI_LBL6	PXI_LBR6	GND	

Pin	A	B	ab	C	D	cd	E	F	ef	XP3 / XJ3 Connector
1	PXIe_CLK100+	PXIe_CLK100-	GND	PXIe_SYNC100+	PXIe_SYNC100-	GND	PXIe_DSTARC+	PXIe_DSTARC-	GND	
2	PRSNT#	PWREN#	GND	PXIe_DSTARB+	PXIe_DSTARB-	GND	PXIe_DSTARA+	PXIe_DSTARA-	GND	
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND	
4	MPWRGD	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND	
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND	
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND	
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND	
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND	
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND	
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND	

Pin	Z	A	B	C	D	E	F	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1 / J1 Connector
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND	
12–14	Key Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	

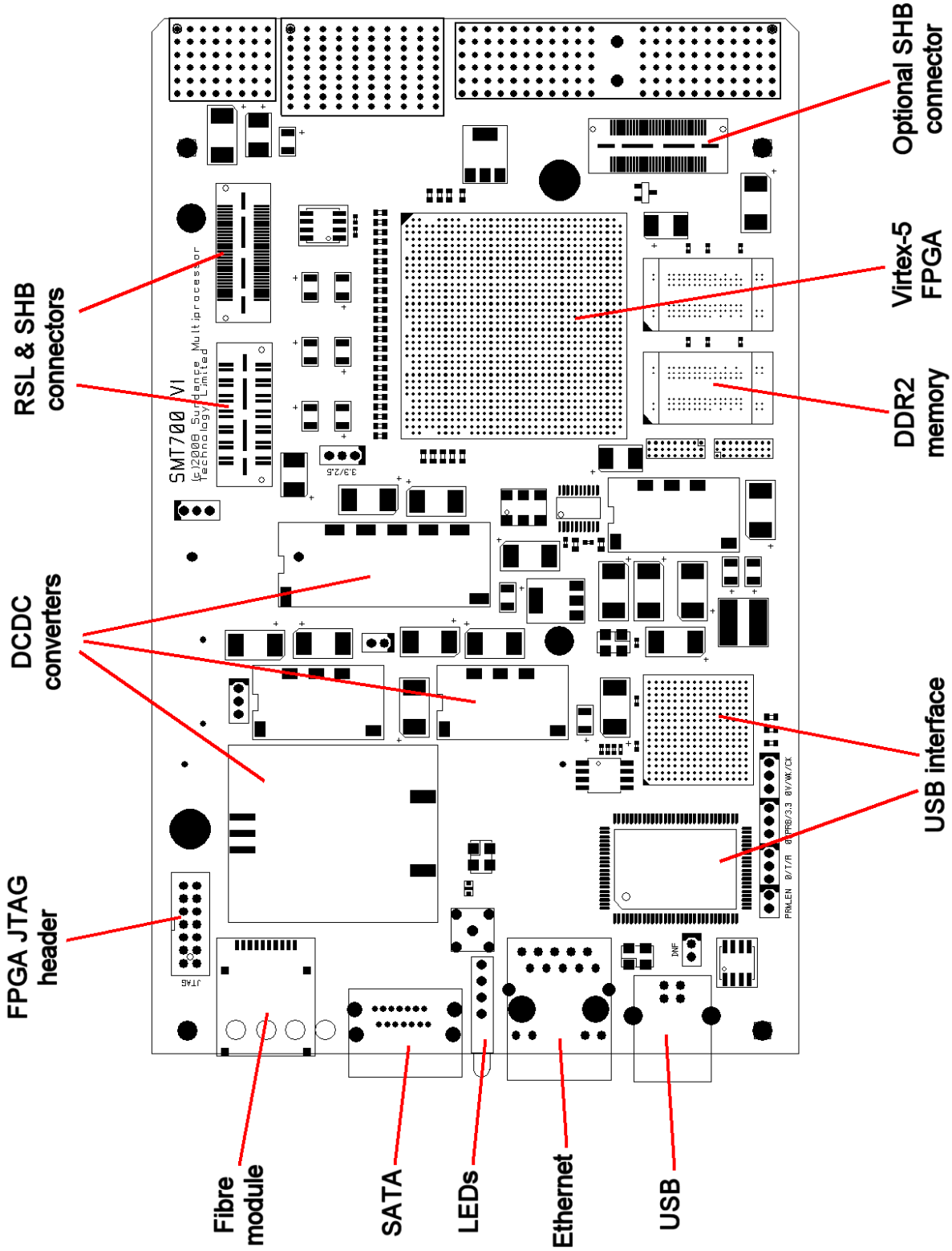
The SMT700 implements up to eight 2.5-Gigabit PCI Express lanes, allowing a maximum data transfer of 2 gigabytes per second. It also implements optionally a 32-bit, 33-MHz PCI interface.

6 FPGA Pin Allocation

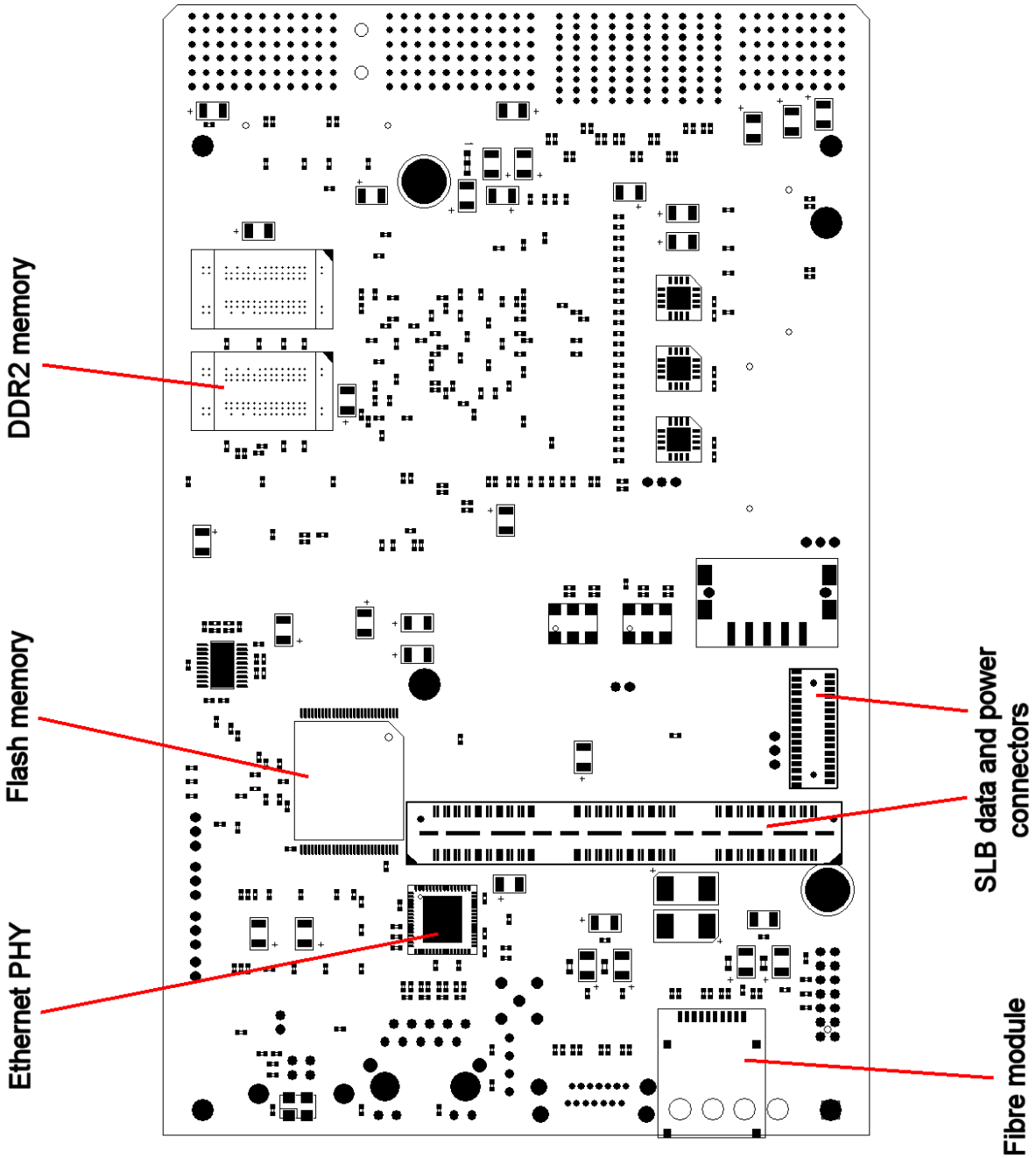
Sub-system	Pin count	Instances	Total
Clock	1	2	2
PXI	23	1	23
PXIe	18	1	18
PCI	52	1	52
DDR2	115	1	115
SLB			110
Ethernet	16	1	16
SHB	40	1	40
LEDs	4	1	4
CPLD	44	1	44
Clock distribution	6	1	6
TOTAL			430

7 Board Layout

7.1 Top side



7.2 Bottom side



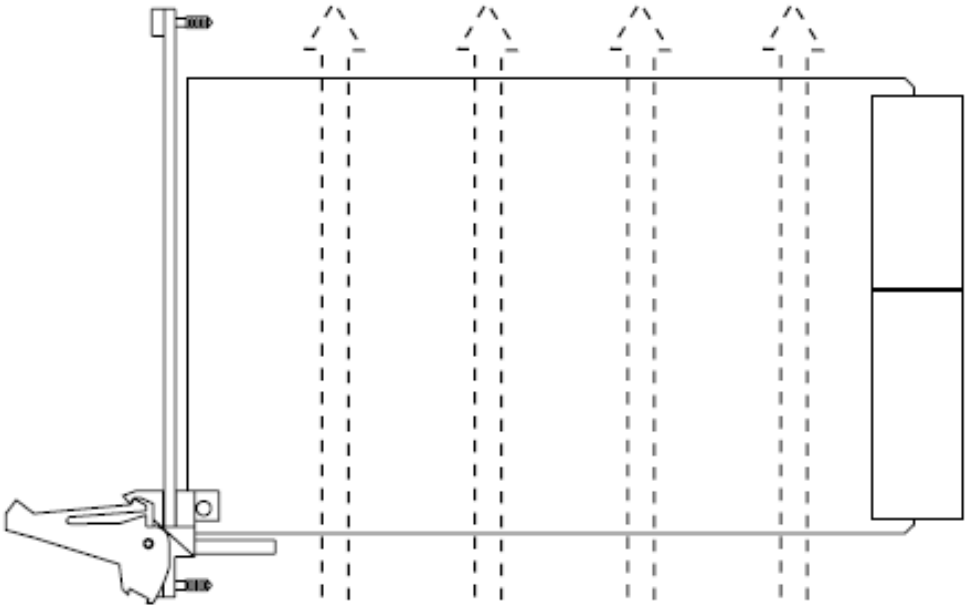
8 Power and Thermal

8.1 Power dissipation

The PXI Express chassis receiving the SMT700 module should provide enough forced air flow in order to dissipate the heat generated by the module. The air flow must be going against gravity or upwards, as specified in the PXI Specification.

It is also specified that a 3U PXI Express module should not dissipate more than 30 Watts of heat.

The following picture shows the direction of the forced air flow across a 3U PXI Express module:



The estimated maximum power consumption of the Virtex5 FPGA is 22W. This assumes a design running at 500MHz with all DSP slices used.

All of the devices on the SMT700 derive their power from the +12V PXI power rails.

It is strongly advised, as applications vary considerably, to use the Xilinx power estimator tools available from this link;

http://www.xilinx.com/products/design_resources/design_tool/grouping/power_tools.htm

9 Support Packages

TBD

10 Verification, Review & Validation Procedures

To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

11 Physical Properties

Dimensions		

Weight	

Voltage	Current
+12V	Estimated 2.5A
+5V	
+3.3V	
-5V	0
-12V	0

MTBF	

12 Safety

This module presents no hazard to the user when in normal use.

13 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

14 Ordering Information

Several variations of this product are available. Various FPGA types and speed grades are available. Please contact Sundance for further information.

Eg. SMT700-LX50-1	Fitted with an XC5VLX50T, 1Gbyte of memory, and a single fibre module..