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Product Specification for SMT702

Sundance Multiprocessor Technology Ltd, Chiltern House, Waterside, Chesham, Bucks. HP5 1PS.

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Revision History

Issue	Changes Made	Date	Initials
1	First Release	07/02/07	PhSR
2	Power consumptions detailed. Block diagrams updated. Virtex changed for a bigger part. Decision made for the clock chip. FPGA Block Diagram added.	23/02/07	PhSR
3	Layout added and registers (ADC and Frequency Synthesizer) added. Comport removed	22/03/07	PhSR
4	JTAG Connector placed on Layout – Front panel connectors are all SMA.	28/03/07	PhSR
5	DDR2 interface speed added, changed to hybrid PXI module	15/04/07	PhSR
6	Options PXIe/PXI clarified	19/04/07	PhSR
7	SHB Connector added for connection to SMT712 board. Diagrams updated.	15/05/07	PhSR
8	Layout updated	09/10/07	PhSR

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1 Introduction

The SMT702 is a PXI Express (opt. Hybrid) Peripheral Module (3U), which integrates two fast 8-bit ADCs, a clock circuitry, 2 banks of DDR2 Memory and a Virtex5 Xilinx FPGA, under the 3U format.

The PXIe specification integrates PCI Express signalling into the PXI standard for more backplane bandwidth. It also enhances PXI timing and synchronisation features by incorporating a 100MHz differential reference clock and triggers. The SMT702 can also integrate the standard 32-bit PXI signalling as an option.

Both ADC chips are identical and can produce 3 Giga-samples per second each, with an 8-bit resolution. The manufacturer is National Semiconductor and the part number is ADC083000. Analog-to-Digital converters are clocked by circuitry based on a PLL coupled with a VCO in order to generate a low-jitter signal. The ADC083000 is capable to achieve 7 bits of ENOB, 44dBs of SNR and 54dBs of SFDR. The full bandwidth is 3GHz. Each ADC integrates settings such as offset and scale factor, which makes the pair of ADC suitable to be combined together in order to make a 6GSPS single Analog to Digital converter. This will be subject to a specific application note.

An on-board PLL+VCO chip ensure a stable fixed sampling frequency (maximum rate), in order for the board to be used as digitiser without the need of external clock signal. The PLL will be able to lock the VCO either on the on-board 100MHz reference or the 100MHz PXI express reference (or 10MHz PXI reference depending on option) or on an external reference signal. The sampling clock for the converters can be either coming from the PLL+VCO chip or from an external source. The chip used is a National Semiconductor part: LMX2531LQ1500. The reference clock selected is also output on a connector in order to pass it to an other module.

The Virtex5 FPGA is responsible for controlling all interfaces, including PXI (32-bit) and PXIe (8 lanes allocated – depending on PXIe chassis, 4 or 8 lanes would be used), as well as routing samples. On the SMT702 the FPGA is an XC5VLX50T, which is footprint compatible with XC5VLX85T and XC5VLX110T. Note that all Virtex5s connect PXIe and only the XC5VLX110T will allow the full 32-bit PXI format

Two DDR2 memory banks are accessible by the FPGA in order to store data on the fly.

An SHB connector is available (XC5VLX110T only) in order to transfer data/samples to an other Sundance module.

All analog connectors on the front panel are SMA.

2 Related Documents

2.1 Referenced Documents

1 - National Semiconductor ADC083000:

http://www.national.com/pf/DC/ADC083000.html

2 – National Semiconductor LMX2531LQ1500:

http://www.national.com/pf/LM/LMX2531LQ1500E.html

3 - Virtex5 FPGA:

http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/index.htm

4 - PXIe specifications: http://www.pxisa.org/Spec/PXIEXPRESS_HW_SPEC_R1.PDF

5 – Micron 2Gigabit DDR2 chip MT47H128M16:

http://download.micron.com/pdf/datasheets/dram/ddr2/2gbddr2.pdf

3 Acronyms, Abbreviations and Definitions

3.1 Acronyms and Abbreviations

PXIe : PXI Express.

SNR: Signal-to-Noise Ratio. It is expressed in dBs. It is defined as the ratio of a signal power to the noise power corrupting the signal.

SINAD: Signal-to-Noise Ratio plus Distorsion. Same as SNR but includes harmonics too (no DC component).

ENOB: Effective Number Of Bits. This is an alternative way of defining the Signal-to-Noise Ratio and Distorsion Ratio (or SINAD). This means that the ADC is equivalent to a perfect ADC of ENOB number of bits.

SFDR: Spurious-Free Dynamic Range. It indicates in dB the ratio between the powers of the converted main signal and the greatest undesired spur.

3.2 Definitions

4 Functional Description

4.1 Block Diagram

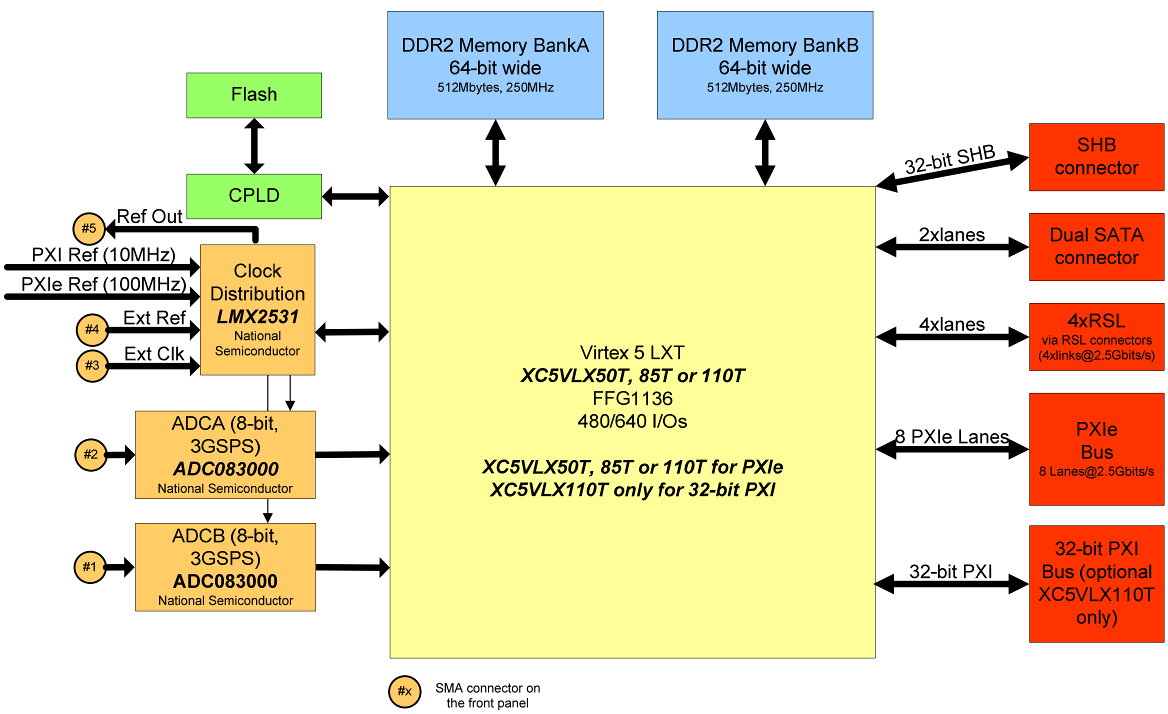


Figure 1 - SMT702 Block Diagram.

4.2 Block Diagram (Option PXIe)

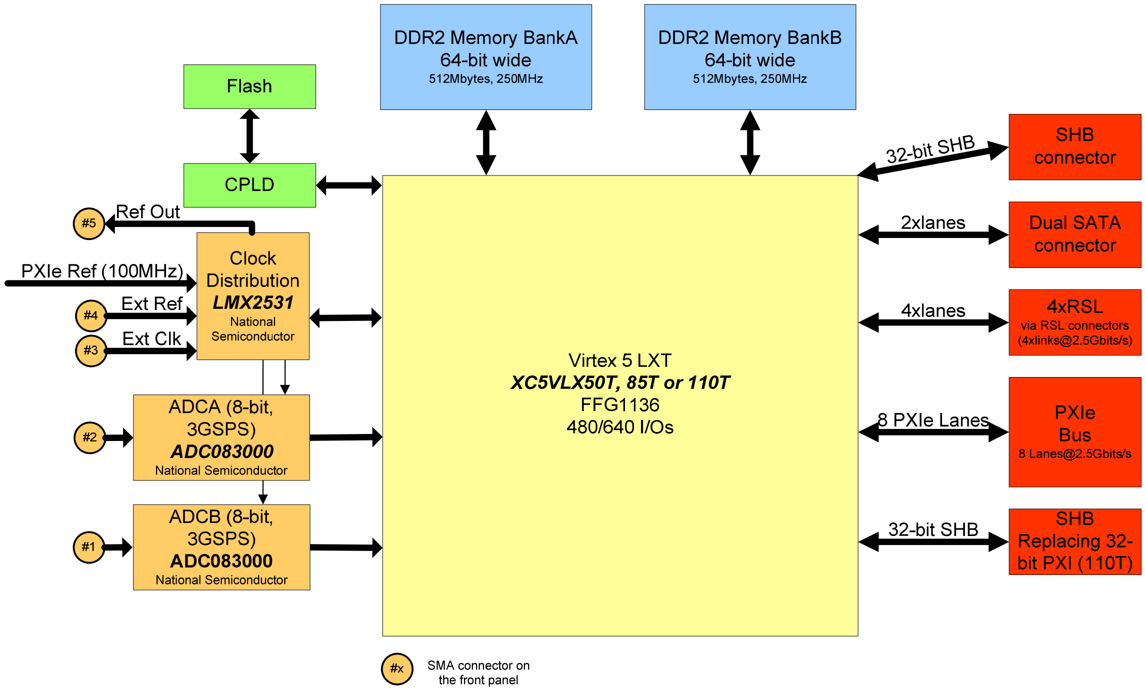


Figure 2 - SMT702 Block Diagram (option PXI Express)

4.3 Block Diagram (option 32-bit PXI)

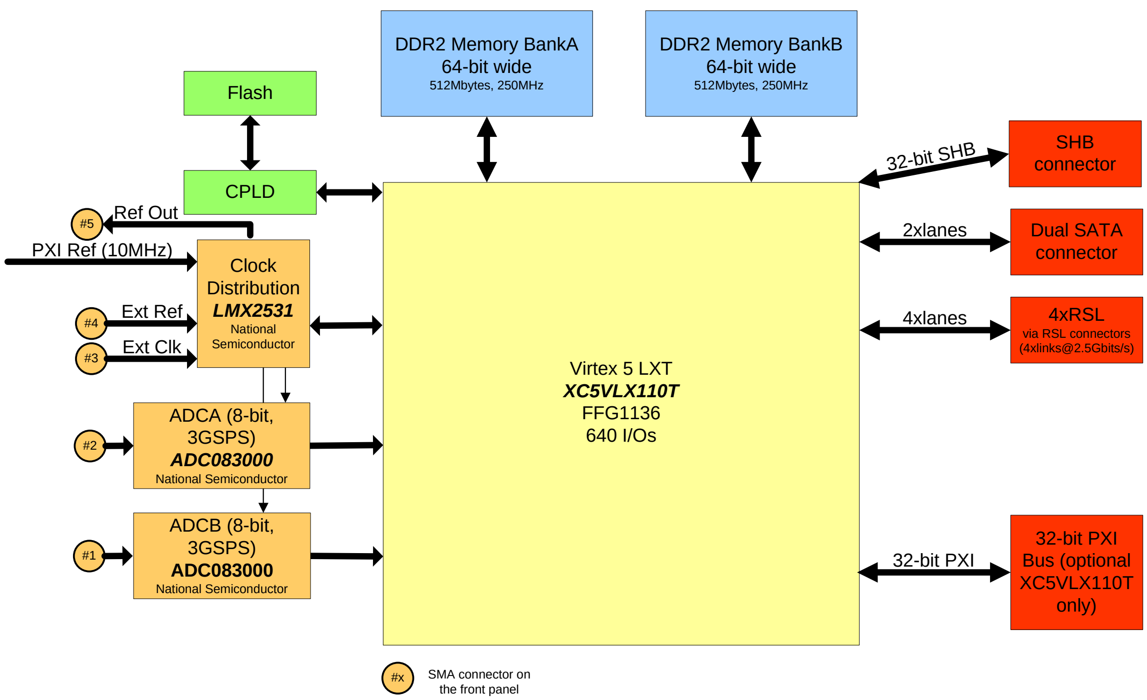


Figure 3 - SMT702 Block Diagram (32-bir PXI Option)

4.4 Module Description

4.4.1 ADCs

The ADCs are 8-bit parts from National Semiconductor (ADC083000). On the SMT702, each ADC can achieve up to 3 GSPS, in DDR mode.

Both ADCs are used in the extended mode. For more information, please refer to the ADC083000 datasheet (National Semiconductor). This implies that they are configured using a Serial Interface implemented in the FPGA.

The typical Bit Error Rate (BER) of the ADC083000 is 10^{-18}. The maximum achievable SNR is 44dBs and the maximum SFDR achievable is 54dBs. These are the manufacturer figures.

4.4.2 FPGA

The FPGA fitted as standard on the SMT702 is part of the Virtex5 LXT family: XC5VLX50T. The package used if FFG1136. It is footprint compatible with the XC5VLX85T and XC5VLX110T.

The FPGA should be at least a -2 speed grade, or -3 for an even faster FPGA.

The parts mentioned above are also footprint compatible with the SXT series: XC5VSX50T and XC5VSX95T. The SXT series implements a DSP48E core, which if used on the SMT702 may result power consumption problem such as exceeding the PXI Express Hybrid 3U Peripheral Module limits.

4.4.3 Configuration (CPLD+Flash)

The FPGA gets its configuration at power up from the Flash memory via a CPLD.

Once the FPGA configured, the contents of the flash can be dynamically changed. Words are received from the PXI Express bus and passed to the CPLD that writes them in the Flash memory. A control word will be dedicated for reconfiguring the FPGA without the need of powering off and back on the board.

This allows the SMT702 to be used as a development platform for signal processing algorithms implementation.

The following diagram show how the connection are made on the board between the CPLD, the Flash memory and the FPGA:

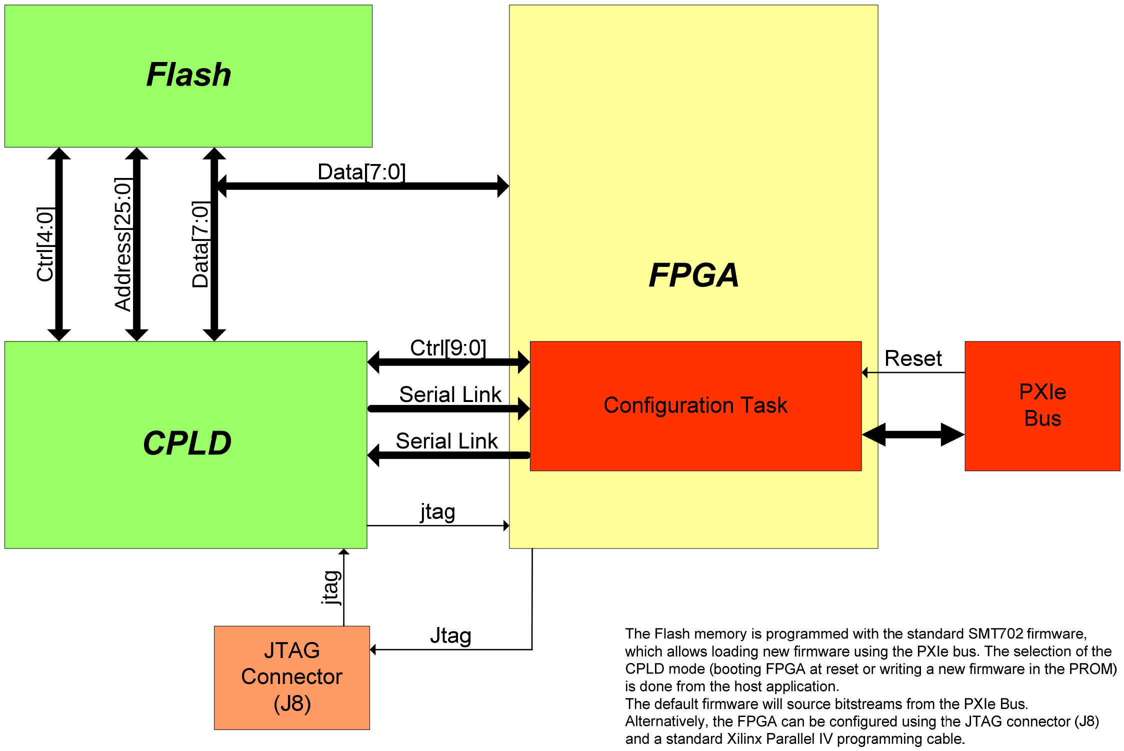


Figure 4 - Configuration (Flash).

4.4.4 DDR2 Memory

Two banks of DDR2 memory are available on the SMT702, directly connected to the FPGA. Interfaces are part of the FPGA design. Each bank is 64-bit wide and 64-Meg deep, so each bank can store up to 512 Mega samples. Each memory bank is dedicated to one ADC.

Xilinx provides performances of a DDR2 interface as being: 200MHz for a -1 part, 267MHz for a -2 part and 333MHz for a -3 part.

Memory burst read or write operations, in order to achieve storage real-time of the ADC samples, should be done under a minimum clock of 187.5 MHz. Clocking the memory interface at 250MHz would allow achieving this figure.

4.4.5 Clock circuitry

An on-board PLL+VCO chip ensure a stable fixed sampling frequency (maximum rate, i.e. 1500MHz), in order for the board to be used as digitiser without the need of external clock signal. The PLL will be able to lock the VCO either on the 10MHz PXI reference or the 100MHz PXI express reference or on an external reference signal. The sampling clock for the converters can be either coming from the PLL+VCO chip or from an external source. The chip used is a National Semiconductor part: LMX2531LQ1500.

The selection Internal/External clock is made via a bit in the control register. The same applies to the selection of the reference clock.

Note that the PLL+VCO chip also has the possibility to output half of the fixed VCO frequency, i.e. 1500/2=750MHz.

4.4.6 PXI Express Bus

As standard, the SMT702 is a 3U PXI Express peripheral module, which means it comes with two PXI Express connectors: XP4 (PXI timing and synchronisation signals) and XP3 (x8 PCI Express and additional synchronisation signals). The SMT702 dedicates 8 lanes to the PXI Express bus, which gives an effective bandwidth per direction of 16Gb/s. It also implies core and user clocks to be 250 MHz. Note that not all PXIe Express chassis can handle 8 lanes on peripheral modules.

The standard SMT702 can plug in any PXI Express Peripheral Slot or any PXI Express Hybrid Slot.

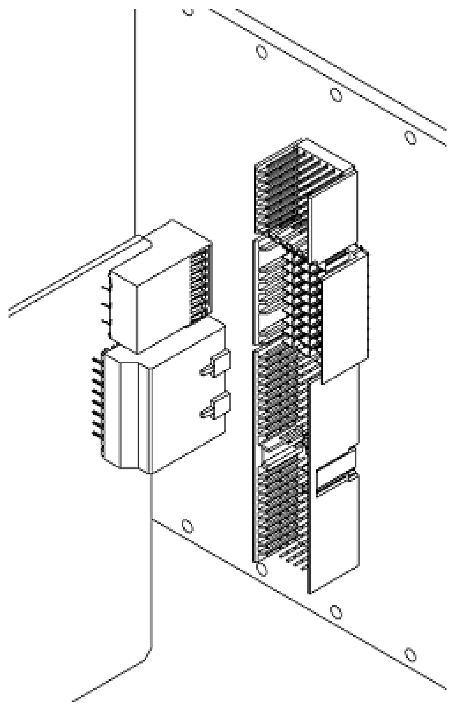


Figure 5 - Standard SMT702 - PXI Express Peripheral Module

Optionally, the module can be a 3U Hybrid Peripheral Slot Compatible PXI-1 Module, means it comes with two connectors: XP4 (PXI timing and synchronisation signals) and P1 (32-bit, 33MHz PCI Signals). This version of SMT702 can only plug in any PXI Express Hybrid Slot

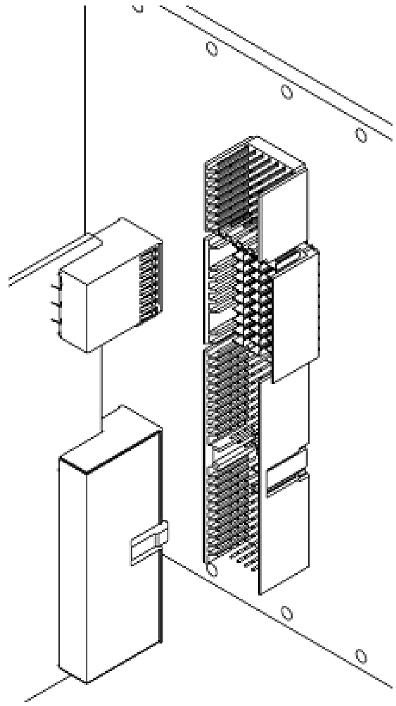


Figure 6 - SMT702 (opt.) - Hybrid Peripheral Slot Compatible PXI-1 Module

4.4.7 SHB Connector

An SHB Connector is available from the FPGA (only with XC5VLX110T). It maps 32 single-ended data lines and a set of control signals including a clock.

It can be used to transfer samples to an other Sundance module, for instance the SMT712.

4.4.8 Power Supply (PXI Express Chassis)

The PXI Express specifications defines the maximum power consumption of 3U PXI Express peripheral modules as:

- 12-Volt rail: 2 Amps maximum (**24 watts**),
- 3.3-Volt rail: 3 Amps maximum (**10 watts**),
- 5-Volt rail (5Vaux): 1 Amp maximum.

An optional external power connector is available for external sources of the above rails. This should be carefully assessed as the fact of using an external power source may not meet the PXI Express specifications requirements.

4.4.9 Power consumption

The FPGA and the DDR2 memory block will be powered from the 12-Volt PXI rail, whereas the ADCs and the clock circuitry will have their own supplies derived from the 3.3-Volt PXI rail.

Virtex5 FPGA (Worst case XC5VLX110T)(19.0 watts)

The XC5VLX50T is the part that will be fitted by default. Footprint compatible parts include XC5LX85T and XC5VLX110T (XC5VSX50T and XC5VSX95T). The following power estimation has been done using a Xilinx spreadsheet, targeting the XC5VLX110T, with 98%

of its LUTs and Flip-Flips used, an 8-lane PCI Express core, 128 DDR lines and the rest of the IOs set to standard LVTTL.

Note that in the case of the XC5VSX95T, using all 640 DSP slices would add an extra 2.7 watts to Vccint.

Vccint = 1.0 Volt / Estimated current = 11Amps [11 watts]

Vccaux = 2.5 Volts / Estimated current = 825mA [2.0 watts]

Vcco_18 = 1.8 Volts / Estimated current = 460mA [0.82 watt]

Vcco_33 = 3.3 Volts / Estimated current = 639mA [2.11 watt]

Vccmgt = 1 Volt / Estimated current = 294mA [0.294 watt]

Vccmgpll = 1.2 Volts / Estimated power = 198mA [0.238 watt]

Vtttx = 1.2 Volts / Estimated power = 390mA [0.468 watt]

Vttrx = 1.2 Volts / Estimated power = 72mA [0.086 watt]

The above figures stand as the worst case, where an XC5VLX110T is fitted with a chip full working at 500MHz. This will not be the case of the standard firmware provided with the board. In case the FPGA design gets to be modified, it is strongly recommended that an power consumption analysis is performed in order to check that 19 watt of total power is not exceeded.

Memory DDR2 – 2 banks of 1Gbytes (5 watts)

Vdd = Vddl = Vddq = 1.8V / Maximum current per chip = 355mA (8 chips – Micron MT47H128M16-37E - in total so 2.8 Amps). This does not include the termination resistors.

Vreference = Vddq/2 = 0.9V

Note that downsizing the memory capacity to 2 banks of 512Mbytes (MT47H64M16-37E) would reduce the current consumption per chip of 25mA (330mA) and would reduce power consumption down to 4.7 watts.

Note that downsizing the memory capacity to 2 banks of 256Mbytes (MT47H32M16-37E) would reduce the current consumption per chip of 15mA (340mA) and would reduce power consumption down to 4.9 watts.

ADCs (5.6 Watts)

Va = Vdr = 1.9 Volts / Maximum current per ADC = 945mA

Clock chip

Vccdig = Vccbuf = Vccvco = Vccvco = 3.0 Volts / maximum current = 46mA

4.4.10 Power dissipation

The PXI Express chassis receiving the SMT702 module should provide enough forced air flow in order to dissipate the heat generated by the module. The air flow must be going against gravity or upwards, as specified in the PXI Specification.

It is also specified that a 3U PXI Express module should not dissipate more than 30 Watts of heat.

The following picture shows the direction of the forced air flow across a 3U PXI Express module:

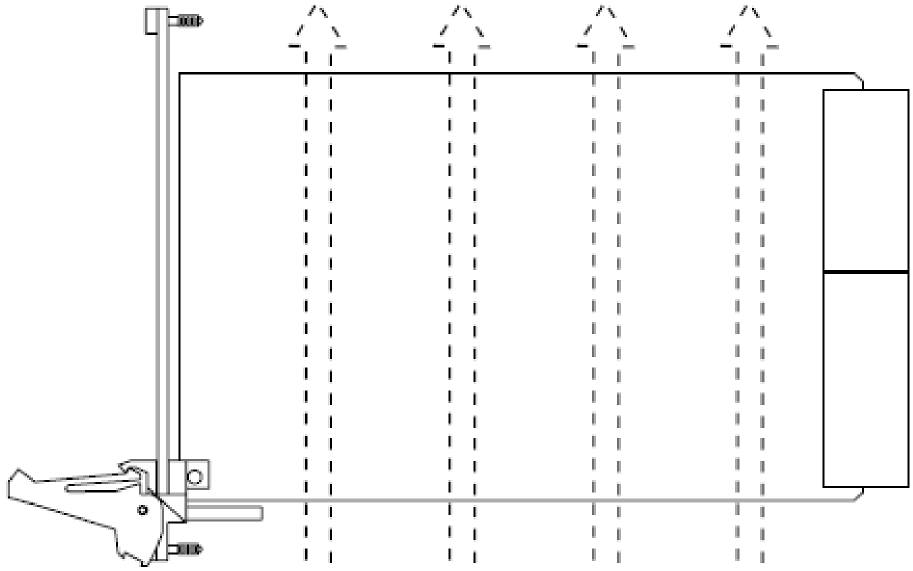
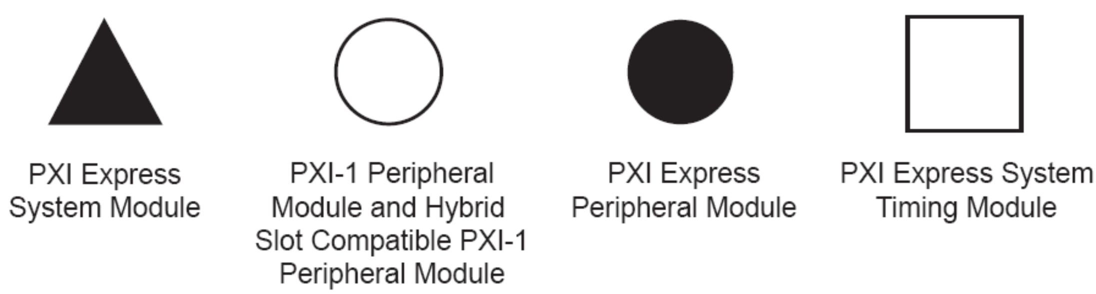


Figure 7 - Forced airflow for a 3U module.

A PXI Express rack has a capacity of dissipating 30 watts of heat per slot using forced air-cooling system via typically two 110-cfm fans with filter.

4.4.11 PXI Express Glyph



4.4.12 External Reset Button

Tbd.

4.4.13 JTAG

A connector (J8) is specifically dedicated for FPGA and CPLD detection and programming. Both the CPLD and the FPGA are part of the JTAG chain. A 14-position (2x7) connector (2mm) is available and shows TDI, TDO, TCK and TMS lines, as well as a Ground and a reference voltage, as shown below:

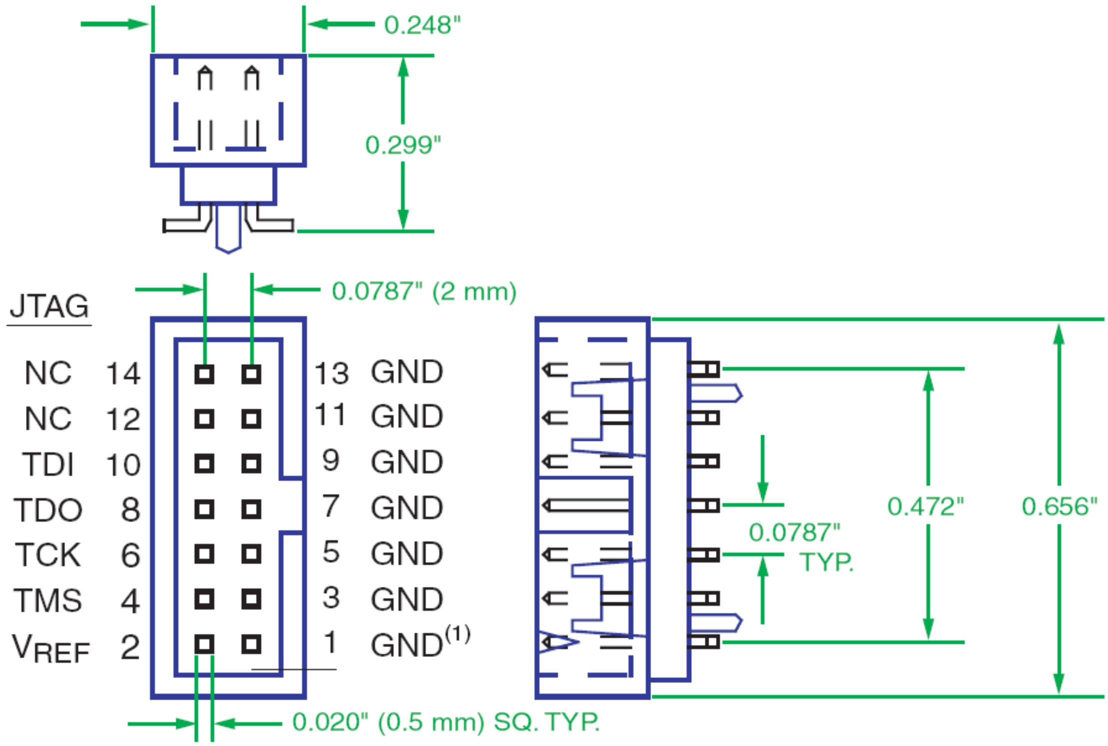


Figure 8 - JTAG Connector.

It can connect directly to a Xilinx Parallel IV cable using the ribbon cable provided by Xilinx. The connector is a Molex part: Molex 87831-1428.

Figure 9 - Photo of a Xilinx Parallel IV cable and its ribbon cable for JTAG connection

4.4.14 PXI Express Hybrid Connectors

As being a PXI Express Hybrid Peripheral Module, the SMT702 is a 3U card with 2 PXI connectors, XP4 and XP3 or P1. The following table shows their pinouts.

PIn	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND
5	GND	PXI TRIG3	PXI TRIG4	PXI TRIG5	GND	PXI TRIG6	GND
6	GND	PXI TRIG2	GND	ATNLED	PXI STAR	PXI CLK10	GND
7	GND	PXI TRIG1	PXI TRIG0	ATNSW#	GND	PXI TRIG7	GND
8	GND	RSV	GND	RSV	PXI LBL6	PXI LBR6	GND

XP4 / XJ4 Connector

PIn	A	B	ab	C	D	cd	E	F	ef
1	PXIe CLK100+	PXIe CLK100-	GND	PXIe SYNC100+	PXIe SYNC100-	GND	PXIe DSTARC+	PXIe DSTARC-	GND
2	PRSNT#	PWREN#	GND	PXIe DSTARB+	PXIe DSTARB-	GND	PXIe DSTARA+	PXIe DSTARA-	GND
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND
4	MPWRGD	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND

XP3 / XJ3 Connector

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12–14				Key Area			
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

P1 / J1 Connector

The SMT702 implements up to eight 2.5-Gigabit PCI Express lanes, allowing a maximum data transfer of 2 gigabytes per second. It also implements optionally a 32-bit, 33-MHz PCI interface.

4.5 FPGA Design

The following block diagram shows how the default FPGA design is organised.

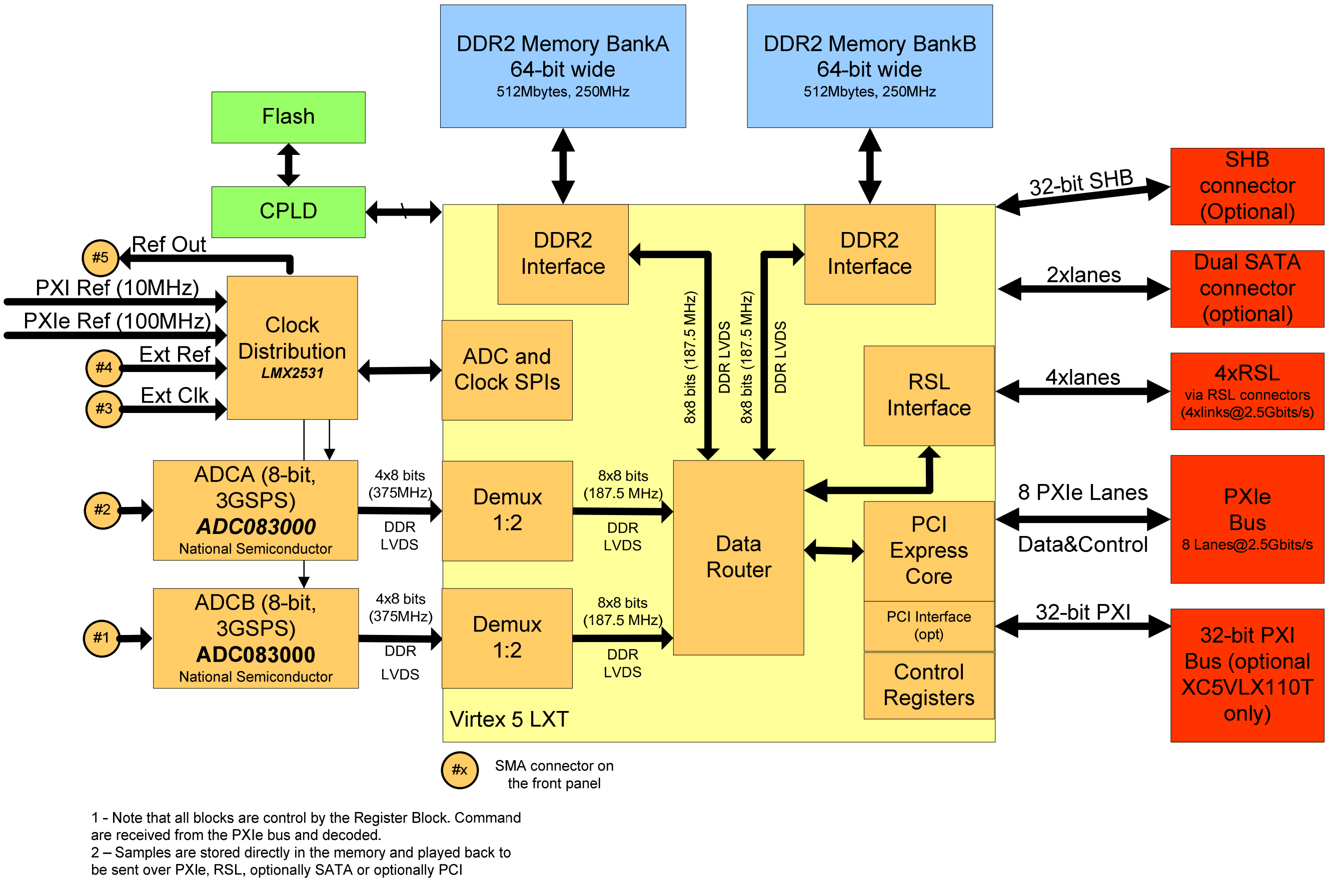


Figure 10 - Block Diagram - FPGA Design (standard Firmware).

4.5.1 Control Registers

The Control Registers drive the complete functionality of the SMT702. They are setup via the PXIe bus (standard firmware provided). The settings of the ADCs, triggers, clocks and the configuration of the RSL/PXI interfaces (optional SATA) and the internal FPGA data path settings can be configured.

The data passed on to the SMT702 over the PXIe bus must conform to a certain packet structure. Only valid packets will be accepted and only after acceptance of a packet will the appropriate settings be implemented. Each packet will start with a command (2 bits – 0x1 for a write operation – 0x2 for a read operation) information, followed by a register address (6 bits – see table), followed by a 24-bit data. This structure is illustrated in the following figure:

	Byte Content							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
3	Command 1	Command 0	Address 5	Address 4	Address 3	Address 2	Address 1	Address 0
2	Data 23	Data 22	Data 21	Data 20	Data 19	Data 18	Data 17	Data 16
1	Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0

Figure 11 – Setup Packet Structure.

4.5.1.1 Memory Map

The write packets must contain the address where the data must be written to and the read packets must contain the address where the required data must be read. The following figure shows the memory map for the writable and readable Control Registers on the SMT702:

Address	Writable Registers	Readable Registers
0x00	Reset Register.	Reserved.
0x01	Test Register.	Test Register.
0x02	Update and Read-back command Register	Firmware Version and Status bits.
0x03		
0x11	ADCA (ADC083000) Register 0x1.	Read-back (FPGA Register) ADCA (ADC083000) Register 0x1.
0x12	ADCA (ADC083000) Register 0x2.	Read-back (FPGA Register) ADCA (ADC083000) Register 0x2.
0x13	ADCA (ADC083000) Register 0x3.	Read-back (FPGA Register) ADCA (ADC083000) Register 0x3.
0x1D	ADCA (ADC083000) Register 0xD.	Read-back (FPGA Register) ADCA (ADC083000) Register 0xD.
0x1E	ADCA (ADC083000) Register 0xE.	Read-back (FPGA Register) ADCA (ADC083000) Register 0x2 E.
0x1F	ADCA (ADC083000) Register 0xF.	Read-back (FPGA Register) ADCA (ADC083000) Register 0xF.
0x21	ADCB (ADC083000) Register 0x1.	Read-back (FPGA Register) ADCB (ADC083000) Register 0x1.
0x22	ADCB (ADC083000) Register 0x2.	Read-back (FPGA Register) ADCB (ADC083000) Register 0x2.
0x23	ADCB (ADC083000) Register 0x3.	Read-back (FPGA Register) ADCB (ADC083000) Register 0x3.
0x2D	ADCB (ADC083000) Register 0xD.	Read-back (FPGA Register) ADCB (ADC083000) Register 0xD.
0x2E	ADCB (ADC083000) Register 0xE.	Read-back (FPGA Register) ADCB (ADC083000) Register 0x2 E.
0x2F	ADCB (ADC083000) Register 0xF.	Read-back (FPGA Register) ADCB (ADC083000) Register 0xF.
0x30	Frequency Synthesizer (LMX2531) register R0	Read-back (FPGA register) Frequency Synthesizer (LMX2531) register R0
0x31	Frequency Synthesizer (LMX2531) register R1	Read-back (FPGA register) Frequency Synthesizer (LMX2531) register R1
0x32	Frequency Synthesizer (LMX2531) register R2	Read-back (FPGA register) Frequency Synthesizer (LMX2531) register R2
0x33	Frequency Synthesizer (LMX2531) register R3	Read-back (FPGA register) Frequency Synthesizer (LMX2531) register R3
0x34	Frequency Synthesizer (LMX2531) register R4	Read-back (FPGA register) Frequency Synthesizer (LMX2531) register R4
0x35	Frequency Synthesizer (LMX2531) register R5	Read-back (FPGA register) Frequency Synthesizer (LMX2531) register R5
0x36	Frequency Synthesizer (LMX2531) register R6	Read-back (FPGA register) Frequency Synthesizer (LMX2531) register R6
0x37	Frequency Synthesizer (LMX2531) register R7	Read-back (FPGA register) Frequency Synthesizer (LMX2531) register R7
0x38	Frequency Synthesizer (LMX2531) register R8	Read-back (FPGA register) Frequency Synthesizer

		(LMX2531) register R8
0x39	Frequency Synthesizer (LMX2531) register R9	Read-back (FPGA register) Frequency Synthesizer (LMX2531) register R9
0x3A	Frequency Synthesizer (LMX2531) register R12	Read-back (FPGA register) Frequency Synthesizer (LMX2531) register R12

Figure 12 – Register Memory Map.

Note that all ADC registers are write-only, which means that the contents of the ADC registers can't be read-back from the ADC itself but can from the FPGA.

4.5.1.2 Register Descriptions

Reset Register – 0x0.

	Reset Register – 0x0						
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved	Reserved	Reserved	Reserved		Reserved	Reserved	Reserved
Default	'0'	'0'	'0'	'0'		'0'	'0'	'0'

	Reset Register – 0x0	
Setting	**Bit 0**	**Description**
0	0	tbd
1	1	tbd
Setting	**Bit 1**	**Description**
0	0	tbd
1	1	tbd

4.5.1.2.1 ADCA (ADC083000) Register 0x1 – Configuration Register.

	ADCA (ADC083000) Register 0x1 – Configuration Register							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved	DRE	RTD	DCS	DCP	nDE	OV	OE
Default	'1'	'0'	'0'	'1'	'0'	'0'	'1'	'1'
0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'

	ADCA (ADC083000) Register 0x1 – Configuration Register	
Setting	**Bit 14**	**Description (DRE – Differential Reset Enable)**
0	0	Single-ended Reset enabled.
1	1	Differential Reset enabled.
Setting	**Bit 13**	**Description (RTD – resistor Trim Disable)**
0	0	Normal Operation.
1	1	Input termination resistor is not trimmed during calibration cycle.
Setting	**Bit 12**	**Description (DCS – Duty Cycle Stabilizer)**
0	0	Stabilisation circuit disabled.
1	1	Duty Cycle Stabilizer applied to the sampling clock.
Setting	**Bit 11**	**Description (DCP – DDR Clock Phase – DDR Mode only)**

0	0	0° phase – ADC output clock time-aligned with data.
1	1	90° phase – ADc output clock placed in the middle of data.
Setting	**Bit 10**	**Description (nDE – DDR Enable)**
0	0	DDr Mode.
1	1	SRD Mode.
Setting	**Bit 9**	**Description (OV – LVDS Output Voltage amplitude)**
0	0	Reduced output amplitude – 510mV.
1	1	Standard output amplitude – 710mV.
Setting	**Bit 8**	**Description (OE –Output Edge)**
0	0	1:4 Demux Mode (DDR Mode must be Selected).
1	1	1:2 Demux Mode (DDR Mode must be selected).

4.5.1.2.2 ADCA (ADC083000) Register 0x2 – Offset Adjust.

	ADCA (ADC083000) Register 0x2 – Offset Adjust							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Offset Value							
Default	"00000000"							
0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'

	ADCA (ADC083000) Register 0x2 – Offset Adjust	
Setting	**Bit 8-15**	**Description (Offset Adjust)**
0	0	8-bit value - 0.176mV per bit – 0x0 is 0mv and 0xFF is 45mV.
Setting	**Bit 7**	**Description (Offset sign)**
0	0	Positive offset.
1	1	Negative offset.

4.5.1.2.3 ADCA (ADC083000) Register 0x3 – Full Scale Voltage Adjust.

	ADCA (ADC083000) Register 0x3 – Full Scale Voltage Adjust							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Adjust Value							
Default	"10000000"							
0	Adjust Value	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	'0'	'1'	'1'	'1'	'1'	'1'	'1'	'1'

	ADCA (ADC083000) Register 0x3 – Full Scale Voltage Adjust	
Setting	**Bit 7-15**	**Description (Full Scale Voltage Adjust)**
0	0	9-bit value – 20% adjustment around the nominal 700mVpp differential value – 0x0 is 560mVp-p and 0x1FF is 840mVp-p.

4.5.1.2.4 ADCA (ADC083000) Register 0xD – Extended Clock Phase Adjust Fine.

	ADCA (ADC083000) Register 0xD – Extended Clock Phase Adjust Fine							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Phase Adjust (Fine)							
Default	“00000000”							
0	Phase Adjust	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	‘0’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’

	ADCA (ADC083000) Register 0xD – Extended Clock Phase Adjust Fine	
Setting	**Bit 7-15**	**Description (Fine Adjust Magnitude)**
0	0	9-bit value – With all bits set, adjust=110ps.

4.5.1.2.5 ADCA (ADC083000) Register 0xE – Extended Clock Phase Adjust Coarse.

	ADCA (ADC083000) Register 0xE – Extended Clock Phase Adjust Coarse							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	ENA	Phase Adjust (Coarse)				LFS	Reserved	Reserved
Default	‘0’					‘0’	‘1’	‘1’
0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’

	ADCA (ADC083000) Register 0xE – Extended Clock Phase Adjust Coarse	
Setting	**Bit 10**	**Description (LFS – Low Frequency Sample Clock)**
0	0	Sample Clock above 900MHz.
1	1	Sample Clock below 900MHz.
Setting	**Bit 11-14**	**Description (Coarse Adjust Magnitude)**
0	0	4-bit value – Each LSB adds approximately 70ps of Clock Adjust.
Setting	**Bit 15**	**Description (ENA - enable)**
0	0	Disabled.
1	1	Enabled.

4.5.1.2.6 ADCA (ADC083000) Register 0xF – Test Pattern register.

	ADCA (ADC083000) Register 0xF – Test Pattern Register							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved	Reserved	Reserved	Reserved	TPO	Reserved	Reserved	Reserved
Default	‘1’	‘1’	‘1’	‘1’	‘0’	‘1’	‘1’	‘1’
0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’

	ADCA (ADC083000) Register 0xF – Test Pattern Register	
Setting	**Bit 11**	**Description (TPO – Test Pattern Output Enable)**
0	0	Normal mode of Operation.
1	1	All ADC outputs in Test Pattern mode.

4.5.1.2.7 ADCB (ADC083000) Register 0x1 – Configuration Register.

	ADCB (ADC083000) Register 0x1 – Configuration Register							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved	DRE	RTD	DCS	DCP	nDE	OV	OE
Default	‘1’	‘0’	‘0’	‘1’	‘0’	‘0’	‘1’	‘1’
0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’

	ADCB (ADC083000) Register 0x1 – Configuration Register	
Setting	**Bit 14**	**Description (DRE – Differential Reset Enable)**
0	0	Single-ended Reset enabled.
1	1	Differential Reset enabled.
Setting	**Bit 13**	**Description (RTD – resistor Trim Disable)**
0	0	Normal Operation.
1	1	Input termination resistor is not trimmed during calibration cycle.
Setting	**Bit 12**	**Description (DCS – Duty Cycle Stabilizer)**
0	0	Stabilisation circuit disabled.
1	1	Duty Cycle Stabilizer applied to the sampling clock.
Setting	**Bit 11**	**Description (DCP – DDR Clock Phase – DDR Mode only)**
0	0	0° phase – ADC output clock time-aligned with data.
1	1	90° phase – ADc output clock placed in the middle of data.
Setting	**Bit 10**	**Description (nDE – DDR Enable)**
0	0	DDr Mode.
1	1	SRD Mode.
Setting	**Bit 9**	**Description (OV – LVDS Output Voltage amplitude)**
0	0	Reduced output amplitude – 510mV.
1	1	Standard output amplitude – 710mV.
Setting	**Bit 8**	**Description (OE –Output Edge)**
0	0	1:4 Demux Mode (DDR Mode must be Selected).
1	1	1:2 Demux Mode (DDR Mode must be selected).

4.5.1.2.8 ADCB (ADC083000) Register 0x2 – Offset Adjust.

	ADCB (ADC083000) Register 0x2 – Offset Adjust							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Offset Value							
Default	“00000000”							

0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'

	ADCB (ADC083000) Register 0x2 – Offset Adjust	
Setting	**Bit 8-15**	**Description (Offset Adjust)**
0	0	8-bit value - 0.176mV per bit – 0x0 is 0mv and 0xFF is 45mV.
Setting	**Bit 7**	**Description (Offset sign)**
0	0	Positive offset.
1	1	Negative offset.

4.5.1.2.9 ADCB (ADC083000) Register 0x3 – Full Scale Voltage Adjust.

	ADCB (ADC083000) Register 0x3 – Full Scale Voltage Adjust							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Adjust Value							
Default	"10000000"							
0	Adjust Value	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	'0'	'1'	'1'	'1'	'1'	'1'	'1'	'1'

	ADCB (ADC083000) Register 0x3 – Full Scale Voltage Adjust	
Setting	**Bit 7-15**	**Description (Full Scale Voltage Adjust)**
0	0	9-bit value – 20% adjustment around the nominal 700mVpp differential value – 0x0 is 560mVp-p and 0x1FF is 840mVp-p.

4.5.1.2.10 ADCB (ADC083000) Register 0xD – Extended Clock Phase Adjust Fine.

	ADCB (ADC083000) Register 0xD – Extended Clock Phase Adjust Fine							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Phase Adjust (Fine)							
Default	"00000000"							
0	Phase Adjust	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	'0'	'1'	'1'	'1'	'1'	'1'	'1'	'1'

	ADCB (ADC083000) Register 0xD – Extended Clock Phase Adjust Fine	
Setting	**Bit 7-15**	**Description (Fine Adjust Magnitude)**
0	0	9-bit value – With all bits set, adjust=110ps.

4.5.1.2.11 ADCB (ADC083000) Register 0xE – Extended Clock Phase Adjust Coarse.

	ADCB (ADC083000) Register 0xE – Extended Clock Phase Adjust Coarse							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	ENA	Phase Adjust (Coarse)				LFS	Reserved	Reserved
Default	‘0’					‘0’	‘1’	‘1’
0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’

	ADCB (ADC083000) Register 0xE – Extended Clock Phase Adjust Coarse	
Setting	**Bit 10**	**Description (LFS – Low Frequency Sample Clock)**
0	0	Sample Clock above 900MHz.
1	1	Sample Clock below 900MHz.
Setting	**Bit 11-14**	**Description (Coarse Adjust Magnitude)**
0	0	4-bit value – Each LSB adds approximately 70ps of Clock Adjust.
Setting	**Bit 15**	**Description (ENA - enable)**
0	0	Disabled.
1	1	Enabled.

4.5.1.2.12 ADCB (ADC083000) Register 0xF – Test Pattern register.

	ADCB (ADC083000) Register 0xF – Test Pattern Register							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved	Reserved	Reserved	Reserved	TPO	Reserved	Reserved	Reserved
Default	‘1’	‘1’	‘1’	‘1’	‘0’	‘1’	‘1’	‘1’
0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’

	ADCB (ADC083000) Register 0xF – Test Pattern Register	
Setting	**Bit 11**	**Description (TPO – Test Pattern Output Enable)**
0	0	Normal mode of Operation.
1	1	All ADC outputs in Test Pattern mode.

4.5.1.2.13 Frequency Synthesizer (LMX2531) Register R0.

	Frequency Synthesizer (LMX2531) Register R0							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved				N[7:4]			
Default	‘0000’				‘0000’			
1	N[3:0]				NUM[11:8]			
Default	‘0000’				‘0000’			
0	NUM[7:0]							
Default	‘00000000’							

	Frequency Synthesizer (LMX2531) Register R0	
Setting	**Bit 11-0**	**Fractional numerator (NUM[11:0])**
0	0	Value between 0 (all 0s) and 4194303 (all 1s)
Setting	**Bit 21-12**	**N Counter (N[7:0])**
0	0	Value between 0 (0x0) and 2039 (0x3F7)

4.5.1.2.14 Frequency Synthesizer (LMX2531) Register R1.

	Frequency Synthesizer (LMX2531) Register R1							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved						Reserved	ICP[4]
Default	'000000'						'1'	'0'
1	ICP[3:0]			N[10:8]			NUM[21:20]	
Default	'000'			'000'			'00'	
0	NUM[19:12]							
Default	'00000000'							

	Frequency Synthesizer (LMX2531) Register R1	
Setting	**Bit 9-0**	**Fractional numerator (NUM[21:12])**
0	0	Value between 0 (all 0s) and 4194303 (all 1s)
Setting	**Bit 12-10**	**N Counter (N[10:8])**
0	0	Value between 0 (0x0) and 2039 (0x3F7)
Setting	**Bit 16-13**	**Charge Pump Current**
0	0	0x0 corresponds to 90uA (state 1x) and 0xF (State 16x) to 1440uA (90uA per state)

4.5.1.2.15 Frequency Synthesizer (LMX2531) Register R2.

	Frequency Synthesizer (LMX2531) Register R2							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved					Reserved	DEN[11:0}	
Default	'00000'					'1'	'00'	
1	DEN[11:0]							
Default	'00000000'							
0	DEN[11:0]		R[5:0}					
Default	'00'		'000000'					

	Frequency Synthesizer (LMX2531) Register R2	
Setting	**Bit 5-0**	**R Counter Value (R[5:0])**
0	0	R Country Value – These bits determine the phase detector frequency. Only possible values are 1, 2, 4, 8, 16 or 32
Setting	**Bit 17-6**	**Fractional Denominator DEN[11:0]**
0	0	Value between 0 (all 0s) and 4194303 (all 1s)

4.5.1.2.16 Frequency Synthesizer (LMX2531) Register R3.

	Frequency Synthesizer (LMX2531) Register R3							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved				DIV2	FDM	DITHER[1:0]	
Default	'0000'				'0'	'0'	'00'	
1	ORDER[1:0]		FoLD[3:0]				DEN[21:12]	
Default	'00'		'0000'				'00'	
0	DEN[21:12]							
Default	'00000000'							

	Frequency Synthesizer (LMX2531) Register R3	
Setting	**Bit 9-0**	**Fractional Denominator DEN[21:12]**
0	0	Value between 0 (all 0s) and 4194303 (all 1s)
Setting	**Bit 13-10**	**Multiplexed Output for Ftest/LD pin FoLD[3:0]**
0	0x0	Disabled (high impedance)
1	0x1	Logical High State (push pull)
2	0x2	Logical Low State (push pull)
3	0x3	Digital Lock Detect (push pull)
4	0x5	N Counter Output divided by 2 (push pull)
5	0x6	Analog Lock Detect (open drain)
6	0x7	Analog Lock Detect (push pull)
7	0xE	R counter output (push pull)
Setting	**Bit 15-14**	**Order of Delta Sigma modulator ORDER[1:0]**
0	0x0	Fourth
1	0x1	Reset Modulator (all fractions are ignored)
2	0x2	Second
3	0x3	Third
Setting	**Bit 17-16**	**Dithering DITHER[1:0]**
0	0x0	Weak dithering
1	0x1	Reserved
2	0x2	Strong Dithering
3	0x3	Dithering Disabled
Setting	**Bit 18**	**Fractional Denominator Mode FDM**
0	0x0	Only 12 LSBs of the fractional numerator and denominator are considered
1	0x1	Only the 10 MSBs of the fractional numerator and denominator are considered
Setting	**Bit 19**	**Divide By 2 option DIV2**
0	0x0	VCO output frequency not divided by 2
1	0x1	VCO output frequency divided by 2

4.5.1.2.17 Frequency Synthesizer (LMX2531) Register R4.

	Frequency Synthesizer (LMX2531) Register R4							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved						ICPFL[3:0]	
Default	'000000'						'00'	

1	ICPFL[3:0]	TOC[13:0]
Default	‘00’	‘000000’
0	TOC[13:0]	
Default	‘00000000’	

	Frequency Synthesizer (LMX2531) Register R4	
Setting	**Bit 13-0**	**Timeout Counter for fastlock (TOC[13:0])**
0	0	0x0 Timeout 0 – 0x1 Timeout always enable – 0x2 – timeout 0 – 0x3 timeout 0 – 0x4 timeout 4x2 phase detector - … - 0x3FFF 16383x2 phase detector
Setting	**Bit 17-14**	**Charge Pump Current for fastlock ICPFL[3:0]**
0	0	0x0 corresponds to 90uA (state 1x) and 0xF (State 16x) to 1440uA (90uA per state)

4.5.1.2.18 Frequency Synthesizer (LMX2531) Register R5.

	Frequency Synthesizer (LMX2531) Register R5							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved						ICPFL[3:0]	
Default	‘000000’						‘00’	
1	ICPFL[3:0]		TOC[13:0]					
Default	‘00’		‘000000’					
0	Reserved	EN_DIGLOD	EN_PLLLDO2	EN_PLLLDO1	EN_VCOLD	EN_OSC	EN_VCO	EN_PLL
Default	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’

	Frequency Synthesizer (LMX2531) Register R5	
Setting	**Bit 0**	**Enable bit for pll – EN_PLL**
0	0	PLL powered off
1	1	PLL powered on
Setting	**Bit 1**	**Enable bit for vco – EN_VCO**
0	0	VCO powered off
1	1	VCO powered on
Setting	**Bit 2**	**Enable bit for Oscillator inverter – EN_OSC**
0	0	Reference Oscillator powered off
1	1	Reference Oscillator powered on
Setting	**Bit 3**	**Enable bit for VCO LDO – EN_VCOLDO**
0	0	LDO powered off
1	1	LDO powered on
Setting	**Bit 4**	**Enable bit for PLL LDO1 – EN_PLLLDO1**
0	0	LDO powered off
1	1	LDO powered on
Setting	**Bit 5**	**Enable bit for PLL LDO2 – EN_PLLLDO2**
0	0	LDO powered off
1	1	LDO powered on
Setting	**Bit 6**	**Enable bit for Digital LDO – EN_DIGLDO**
0	0	PLL powered off
1	1	PLL powered on

Setting	Bit 14	Reset all register REG_RST
0	0	Normal Operation
1	1	All register set to the default values

4.5.1.2.19 *Frequency Synthesizer (LMX2531) Register R6.*

	Frequency Synthesizer (LMX2531) Register R6							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved					XTLSEL[2:0]		
Default	‘00000’					‘000’		
1	VCO_ACI_SEL[3:0]				EN_LPF LTR	R4_ADJ[1:0]		R4_ADJ_FL[1:0]
Default	‘0000’				‘0’	‘00’		‘00’
0	R4_ADJ_FL[1:0]	R3_ADJ[1:0]		R3_ADJ_FL[1:0]		C3_4_ADJ[2:0]		
Default	‘00’	‘00’		‘00’		‘000’		

	Frequency Synthesizer (LMX2531) Register R6	
Setting	**Bit 2-0**	**Value for C3 and C4 in the internal loop filter – C3_4_ADJ[2:0]**
0	0x0	C3=50pF and C4=50pF
1	0x1	C3=50pF and C4=100pF
2	0x2	C3=50pF and C4=150pF
3	0x3	C3=100pF and C4=50pF
4	0x4	C3=150pF and C4=50pF
5	0x5	C3=100pF and C4=100pF
6	0x6	C3=50pF and C4=150pF
7	0x7	C3=50pF and C4=150pF
Setting	**Bit 4-3**	**Value for internal loop filter resistor R3 during fastlock – R3_ADJ_FL[1:0]**
0	0x0	10 kΩ
1	0x1	20 kΩ
2	0x2	30 kΩ
3	0x3	40 kΩ
Setting	**Bit 6-5**	**Value for internal loop filter resistor R3 – R3_ADJ[1:0]**
0	0x0	10 kΩ
1	0x1	20 kΩ
2	0x2	30 kΩ
3	0x3	40 kΩ
Setting	**Bit 8-7**	**Value for internal loop filter resistor R4 during fastlock – R3_ADJ_FL[1:0]**
0	0x0	10 kΩ
1	0x1	20 kΩ
2	0x2	30 kΩ
3	0x3	40 kΩ
Setting	**Bit 10-9**	**Value for internal loop filter resistor R4 – R4_ADJ[1:0]**
0	0x0	10 kΩ
1	0x1	20 kΩ

2	0x2	30 kΩ
3	0x3	40 kΩ
Setting	**Bit 11**	**Enable for partially integrated internal loop filter – EN_LPFLTR**
0	0	Disabled (R3 and R4=0R and C3+C4=200pF)
1	1	Enabled
Setting	**Bit 15-12**	**Optimisation of VCO Phase noise – VCO_ACI_SEL**
0	0	Should always be set to 8
Setting	**Bit 18-16**	**Crystal Selection – XTLSEL[2:0]**
0	0x0	<25MHz
1	0x1	25-50MHz
2	0x2	50-70MHz
3	0x3	>70MHz
4	0x4	Manual mode
5	0x5	Reserved
6	0x6	Reserved
7	0x7	Reserved

4.5.1.2.20 Frequency Synthesizer (LMX2531) Register R7.

	Frequency Synthesizer (LMX2531) Register R7							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved						XTLMAN[11:0]	
Default	‘00000’						‘000000000000’	
1	XTLMAN[11:0]							
Default	‘000000000000’							
0	XTLMAN[11:0]		XTLDIV[1:0]		Reserved			
Default	‘000000000000’		‘00’		‘0000’			

	Frequency Synthesizer (LMX2531) Register R7	
Setting	**Bit 5-4**	**Division Ratio for the Crystal Frequency –** XTLDIV[1:0]
0	0x0	Reserved
1	0x1	Divide by 2 - <20Mhz
2	0x2	Divide by 4 – 20-40Mhz
3	0x3	Divide by 8 - >40Mhz
Setting	**Bit 17-6**	**Manual Crystal Mode – XTLMAN[11:0]**
0	0x0	To be programmed with 0s

4.5.1.2.21 Frequency Synthesizer (LMX2531) Register R8.

	Frequency Synthesizer (LMX2531) Register R8							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2	Reserved							
Default	‘00000000’							
1	Reserved							
Default	‘00000000’							

0	Reserved	XTLMAN 2
Default	‘0000000’	‘0’

	Frequency Synthesizer (LMX2531) Register R8	
Setting	Bit 0	**Manual crystal mode second adjustment** – XTLMAN2
0	0x0	To be programmed with 0s

4.5.1.2.22 Frequency Synthesizer (LMX2531) Register R9.

	Frequency Synthesizer (LMX2531) Register R9							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2	Reserved							
Default	‘00000000’							
1	Reserved							
Default	‘00000000’							
0	Reserved							
Default	‘10111010’							

	Frequency Synthesizer (LMX2531) Register R9	
Setting		
0	0x0	Should be programmed as above

4.5.1.2.23 Frequency Synthesizer (LMX2531) Register R12.

	Frequency Synthesizer (LMX2531) Register R12							
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2	Reserved							
Default	‘00000000’							
1	Reserved							
Default	‘00010000’							
0	Reserved							
Default	‘01001000’							

	Frequency Synthesizer (LMX2531) Register R12	
Setting		
0	0x0	Should be programmed as above

4.5.2 External Signal characteristics

The main characteristics of all external signals of the SMT702 are gathered into the following table.

Analogue Inputs (TBC)	
Input voltage range	**AC coupled option**. 600 or 800mV - AC coupled via RF transformer. **DC coupled option**. 600 or 800mV depending on the Full scale setting. Straight connection to the ADC.
Impedance	50Ω.
Bandwidth	ADC bandwidth: 3 Ghz.
External Reference Input (TBC)	
Input Voltage Level	0.5 – 3.3 Volts peak-to-peak (AC-coupled)
Input Impedance	50-Ohm (Termination implemented at the connector)
Frequency Range	0 – 100 MHz.
External Reference Output (TBC)	
Output Voltage Level	1.6 Volts peak-to-peak (AC-coupled)
Output Impedance	50-Ohm (Termination implemented at the connector)
External Sampling Clock Input (TBC)	
Input Voltage Level	0.5 – 3.3 Volts peak-to-peak (AC-coupled)
Input Format	Single-ended or differential on option (3.3V LVPECL).
Frequency range	500-1500 MHz
External Trigger Inputs (TBC)	
Input Voltage Level	1.5-3.3 Volts peak-to-peak.
Format	DC-coupled and Single-ended (Termination implemented at the connector). Differential on option (3.3 V PECL).
Impedance	50-Ohm.
Frequency range	62.5 MHz maximum
***ADCs* Output**	
Output Data Width	8-Bits
Data Format	Offset Binary
SFDR	54dBs maximum (manufacturer)
SNR	44dBs maximum (manufacturer)
Minimum Sampling Clock	500 MHz
Maximum Sampling Frequency	1500 MHz

Figure 13 – Main Characteristics.

4.6 Interface Description

4.6.1 Mechanical Interface

4.6.2 Electrical Interface

5 Verification Procedures

5.1 CPLD and FPGA detection

This, using the JTAG connector and a Xilinx parallel cable IV.

5.2 ADC connections

Each ADC has a Pattern Mode. This mode will be used to verify connections between the converters and the FPGA.

5.3 ADC Distribution

Once the connections are validated, a capture to verify the distribution with no input connected will be done.

5.4 ADC Performance

This will be done at frequency used in the ADC083000 datasheet to qualify the ADC and in order to compare the performance of the board with the performance of the ADC.

6 Review Procedures

7 Validation Procedures

8 Timing Diagrams

9 Circuit Description / Diagrams

10 Board Layout

10.1 Top View

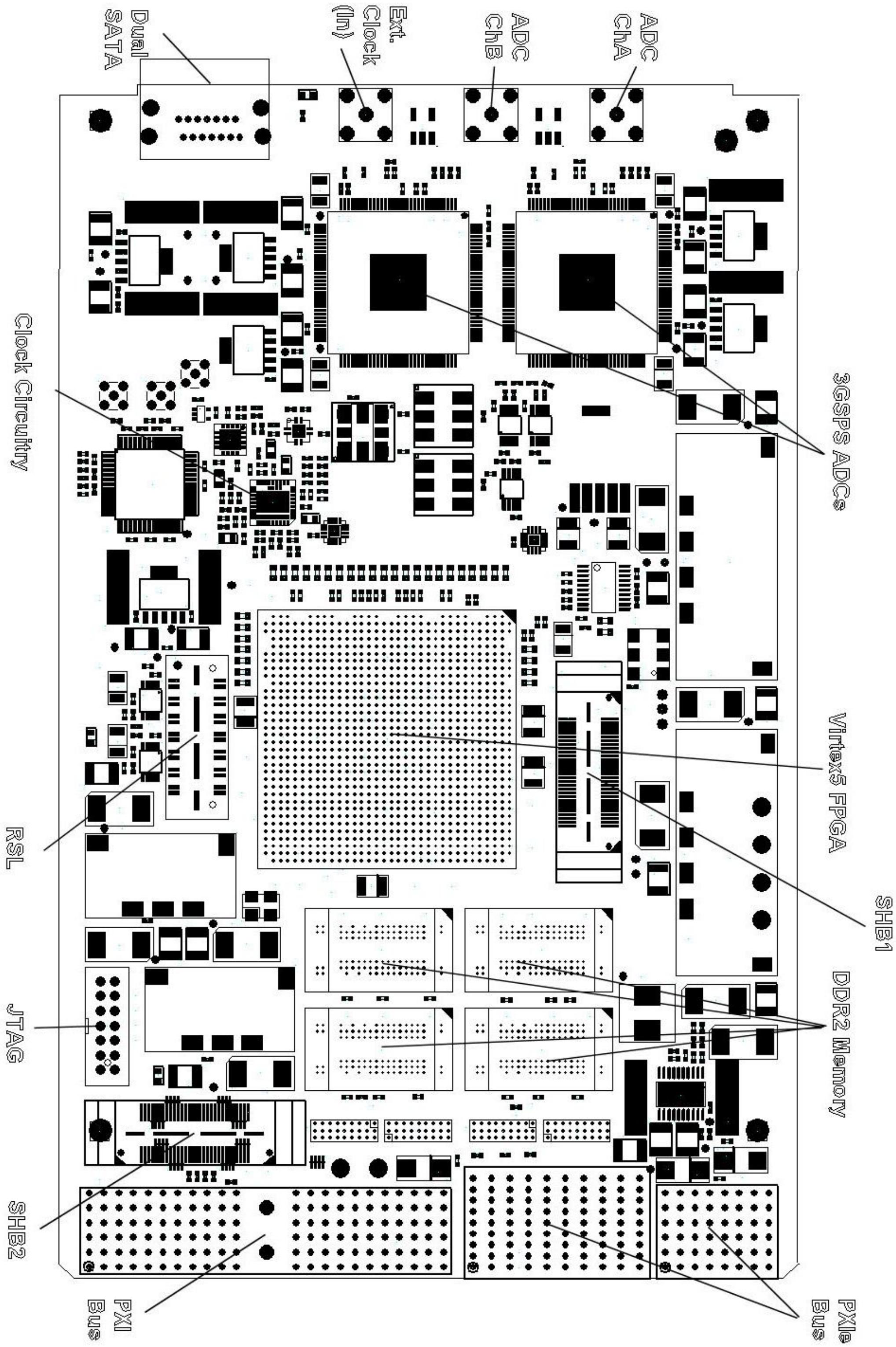


Figure 14 - Board Layout (Top View)

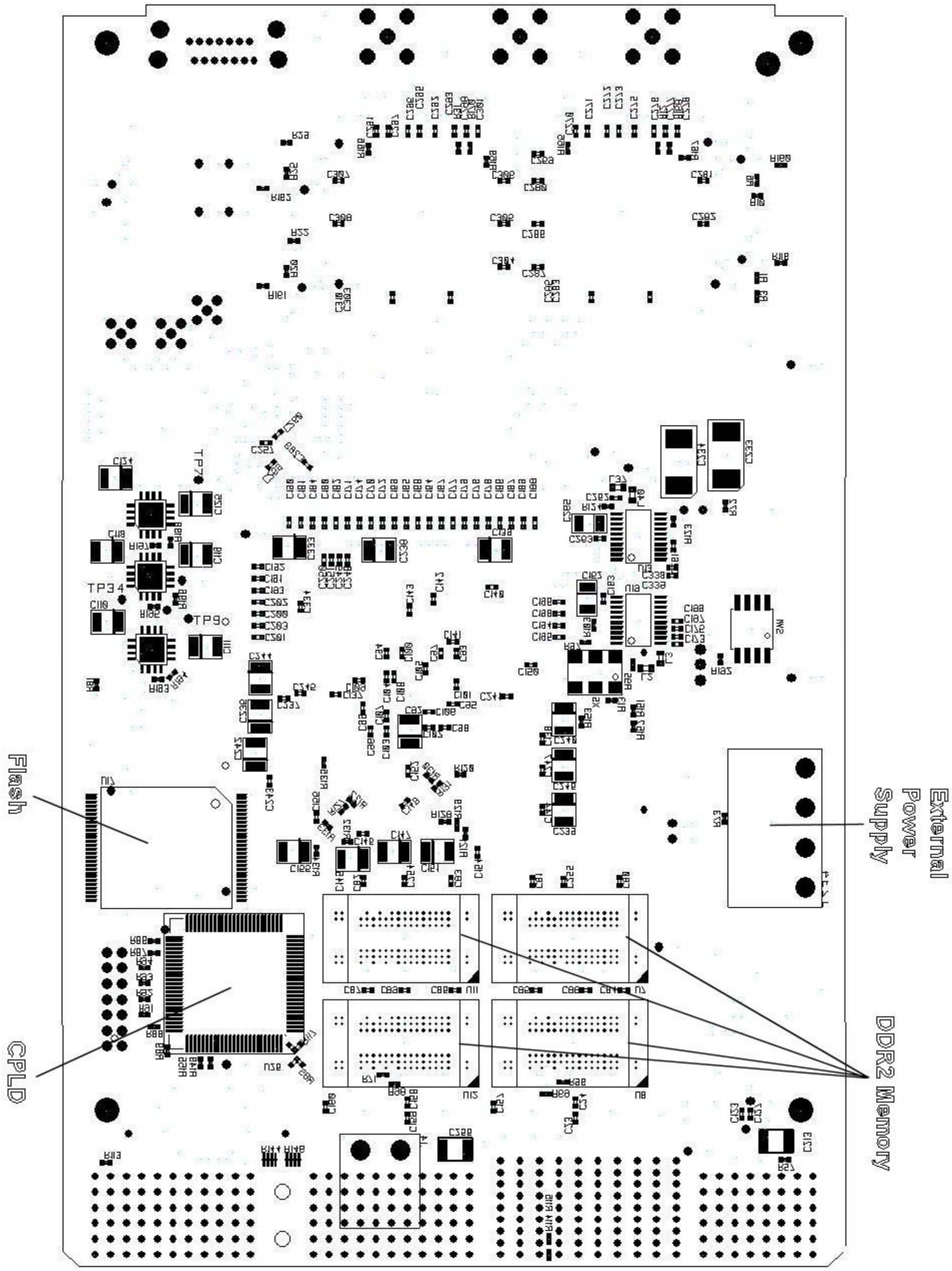


Figure 15 - Board Layout (Bottom View)

11 Pinout

12 Support Packages

13 Physical Properties

Dimensions	PXI Express 3U	
Weight		
Supply Voltages		
Supply Current	+12V	Est. 2 amps
	+5V	N/A
	+3.3V	Est. 3 amps
	-5V	N/A
	-12V	N/A
MTBF		

14 Safety

This module presents no hazard to the user when in normal use.

15 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

16 Ordering Information

Two variations of this product are available :

1 – Board Fitted with an FPGA XC5VLX50T or XC5VLX110T and works as a PXI Express Peripheral Module.

2 – Board Fitted with an FPGA XC5VLX110T and works as a PXI Express Hybrid Peripheral Module (PXI P1 connector).