SUNDANCE

SMT8101

User Manual

Revision History

Date	Comments	Engineer	Version
20/05/2005	Original Document	PSR	1.0
23/08/2005	More exhaustive description of connections added.	PSR	1.1
14/09/2005	Parts list added, block diagram corrected, photo 3L application added.	PSR	1.2
20/10/2005	Updated pictures of the system. Added table of figures.	JPA	1.3

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Contacting Sundance.

You can contact Sundance for additional information by sending email to support@sundance.com.

Notes.

- SHB stands for **S**undance **H**igh-speed **B**us.
- RSL stands for **R**ocket **S**erial **L**ink.
- Comport denotes an 8-bit communication port following the TI C4x standards.
- *SMT8101* is a PCI system to be plugged in a PC. The only software requirement is to have 3L Diamond server installed.

Precautions

In order to guarantee that Sundance's boards function correctly and to protect the module from damage, the following precautions should be taken:

- They are static sensitive products and should be handled accordingly. Always place the modules in a static protective bag during storage and transition.
- When operated in a closed environment make sure that the heat generated by the system is extracted e.g. a fan extracting heat or blowing cool air. Sundance recommends and uses PAPST 12-Volt fans (Series 8300) producing an air flow of 54 cubic meters per hour (equivalent to 31.8 CFM). Fans are placed so they blow across the PCI bus.

Outline description.

The *SMT8101* is PCI based and stands as an evaluation/development platform for Multi-carrier / Multi-standard cellular systems, High Direct-IF infrastructures, Test Equipment, etc

This system is built around 4 main boards: C64xx-based module (*SMT395-VP*) combined with a dual-channel high-speed ADC module (*SMT391-VP*) and a dual-channel high-speed DAC (*SMT381-VP*), all plugged on a PCI carrier board (*SMT310Q*).

Main Modules description.

Three modules are described below. For more details, please refer to www.sundance.com.

SMT395-VP characteristics:

- ⇒ TMS320C6416T processor running at 1GHz
- ⇒ Virtex II Pro FPGA
- ⇒ 8MByte Flash ROM for boot code and FPGA programming
- ⇒ 256MB of SDRAM (133MHz)
- ⇒ Global expansion connector
- ⇒ Six 20MB/s communication ports (comports)
- ⇒ High bandwidth data I/O via 2 **S**undance **H**igh-speed **B**uses (SHB)
- ⇒ Eight 2.5Gbit/sec **R**ocket **S**erial **L**inks (RSL)

SMT381-VP characteristics:

- ⇒ Dual-channel 14-bit DAC (Fujitsu MB86064) sampling at 1GHz
- ⇒ Xilinx Virtex-II FPGA XC2VP30-6
- ⇒ Low-jitter on-board system clock
- ⇒ Two 20MB/s communication ports (comports)
- ⇒ High bandwidth data I/O via 2 **S**undance **H**igh-speed **B**uses (SHB)
- ⇒ Eight 2.5Gbit/sec **R**ocket **S**erial **L**inks (RSL)
- ⇒ Low-jitter on-board system clock

⇒ 50-Ohm terminated analogue outputs via MMBX (Huber and Suhner) connectors

⇒ External Triggers and Clocks via MMBX

SMT391-VP characteristics:

⇒ Dual-channel 8-bit ADC (Atmel AT84AD001) sampling at 1GHz

⇒ Xilinx Virtex-II FPGA XC2VP30-6

⇒ Low-jitter on-board system clock

⇒ Two 20MB/s communication ports (comports)

⇒ High bandwidth data I/O via 2 **S**undance **H**igh-speed **B**uses (SHB)

⇒ Eight 2.5Gbit/sec **R**ocket **S**erial **L**inks (RSL)

⇒ Low-jitter on-board system clock

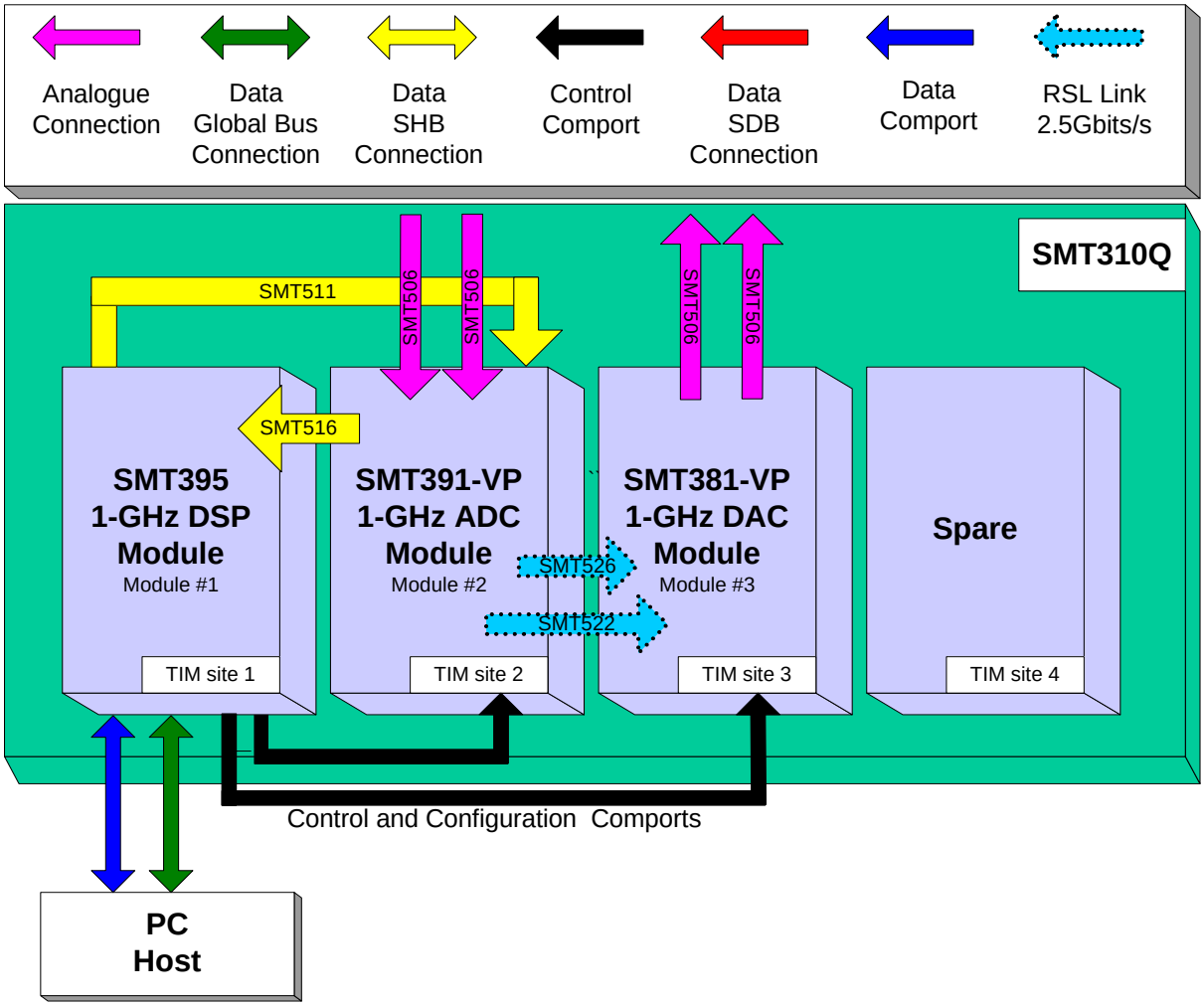
⇒ 50-Ohm terminated analogue inputs via MMBX (Huber and Suhner) connectors

⇒ External Triggers and Clocks via MMBX

Documentation and source files are installed by the way of the *SMT6600* package, which is the Sundance DAQ package. ***Source and application files provided are to be run by the way of 3L Diamond Server only***.

Architecture.

The following diagram shows the architecture of the *SMT8101* system:



The *SMT395-VP* is the module that controls all operations of the system, starting from configuring *SMT391-VP* and *SMT381-VP* FPGAs (Xilinx Virtex-II Pro VP30-6) using configuration ports (Comports).

The data path is clearly as follows: Analog inputs are fed into the ADC module that converts it into digital samples. The data flow is then passed onto the DAC module via RSL links (2.5 Gbits/s – *SMT526* and *SMT522*)) that transforms into Analog signals. Data streams go through 2 FPGAs where processing can be added.

Samples are originally coded on 8-bits by the ADCs, sent over the RSLs and converted into a 14-bit format samples to match the DAC data input as follow:

$$Sample\_DAC\_14\_bits = Sample\_ADC\_8\_bit \ \&\ "100000"$$

The *SMT391-VP* has an on-board VCO that is used to generate a 1GHz clock, which is passed to the *SMT381-VP* so ADC and DAC channels are receiving the same

sampling clock. It also makes the system stand alone with ADC and DAC channels synchronised.

As *SMT381-VP* and *SMT391-VP* have both Virtex-II Pro FPGAs (XC2VP30-6), processing can be added on the way.

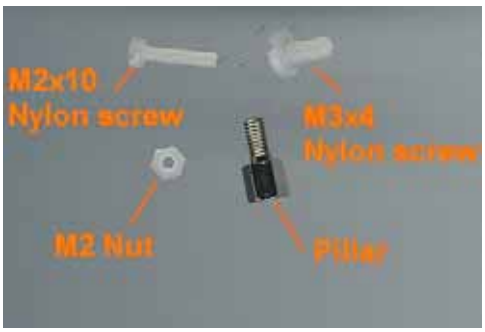
The DSP can also be report information through Comports (bidirectional) such as the temperature monitoring of both DAQ modules (*SMT391-VP* and *SMT381-VP*) or to capture blocks of data via the SHB Bus (*SMT511* and *SMT516*) to the DSP.

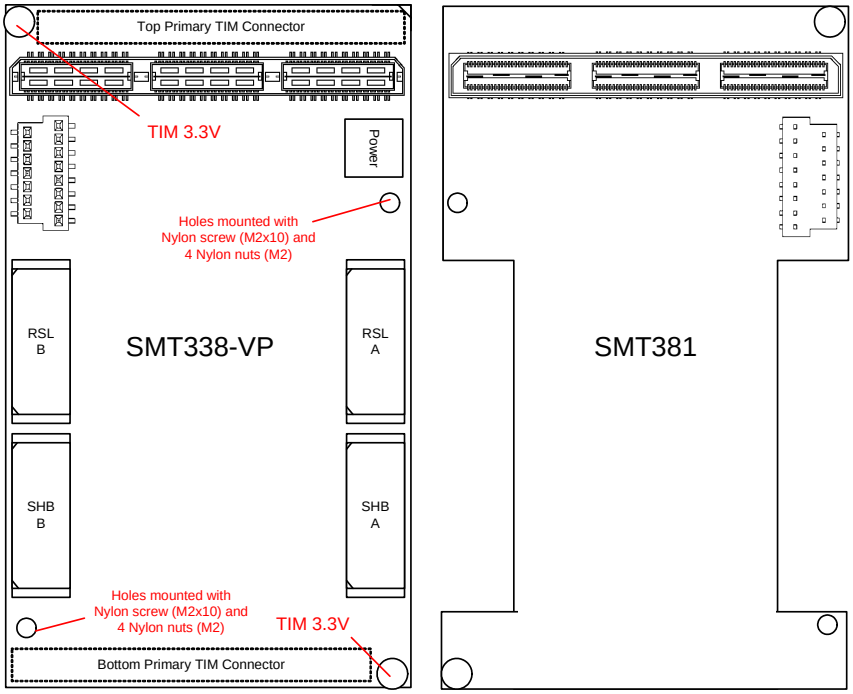
Hardware installation.

Here are the basic steps to follow to install an SLB module with its mezzanine. As an example, the *SMT381-VP* (the *SMT391-VP* follows the same procedure), which is the combination of the *SMT338-VP30-6* (SLB Base Module) and the *SMT381* (Mezzanine Module). Please note that photographs don't necessarily match exactly with the *SMT8101* systems but refer to similar products.

1 – Place the *SMT395-VP* on TIM site 1 of the carrier board (*SMT310Q*).

2 – The following are then required to mount *SMT338-VP30-6+SMT381* on the *SMT310Q*:

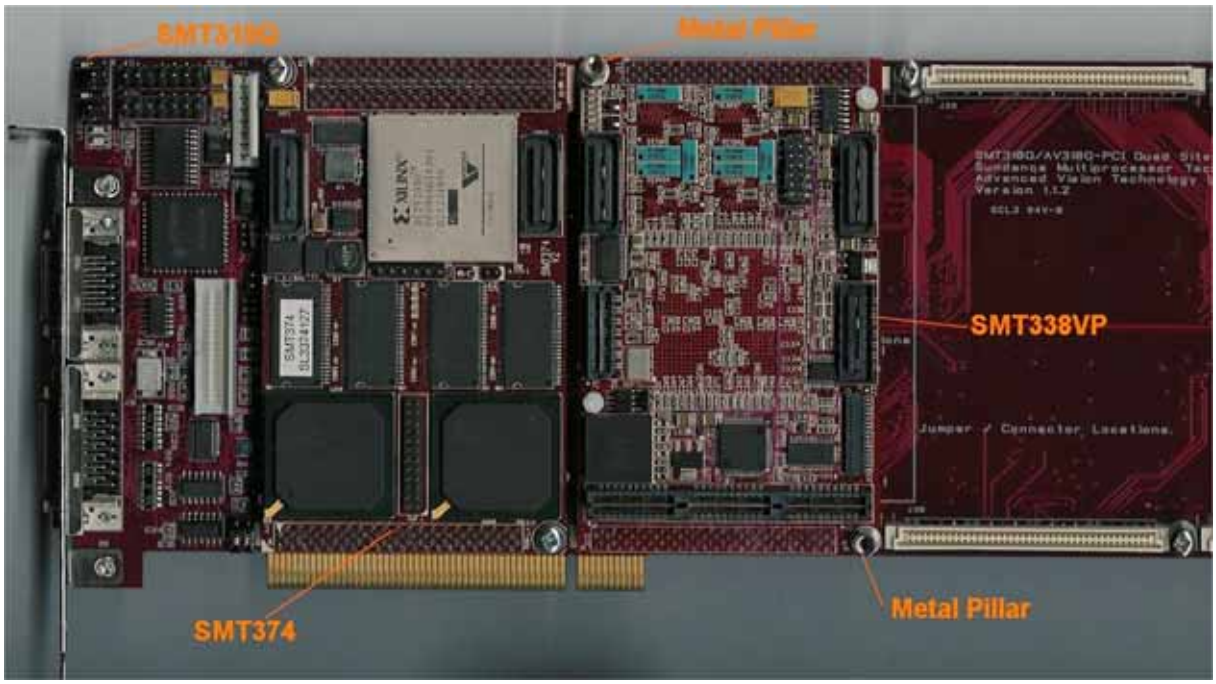




a – First, fit two Nylon screws (M2x10), pointing out (the head of the screws on bottom side).

b – Then fit four M2 nuts on each screw.

c – Place the *SMT338-VP* on the second site (*SMT395-VP* already on first site) on the *SMT310Q* and fit two metal pillars (3.3 Volts).



d – Place the *SMT381* on top of the *SMT338-VP*. Make sure that both modules fit firmly.

e – Fit two M2 nuts on the Nylon screws and two M3x4 screws in the 3.3V pillars.

3 – Connect CommPort 1 of the *SMT395-VP* to CommPort 3 of the *SMT338-VP* (**T1C1** to **T2C3**) via an FMS cable at the back of the *SMT310Q*. Also make the connection **T1C2** to **T3C3**)

4 – Connect SHBA on the *SMT395-VP* to SHBA on the *SMT338-VP* via the *SMT516*.

5 – Connect SHBB on the *SMT395-VP* to SHBB on the *SMT338-VP* via the *SMT511 (SHB to SHB cable)*.

6 – Connect J2 and J3 (*SMT381-VP*) to an oscilloscope or other system of display via MMBX-BNC cables.

7 – Place the carrier board in the host system and power up the PC and a fan to cool down the system.

8 – Connect a signal (0.36 Volts peak-to-peak) to J1 and J2 (*SMT391-VP*).

The following pictures show how connections are made at the top of the system:

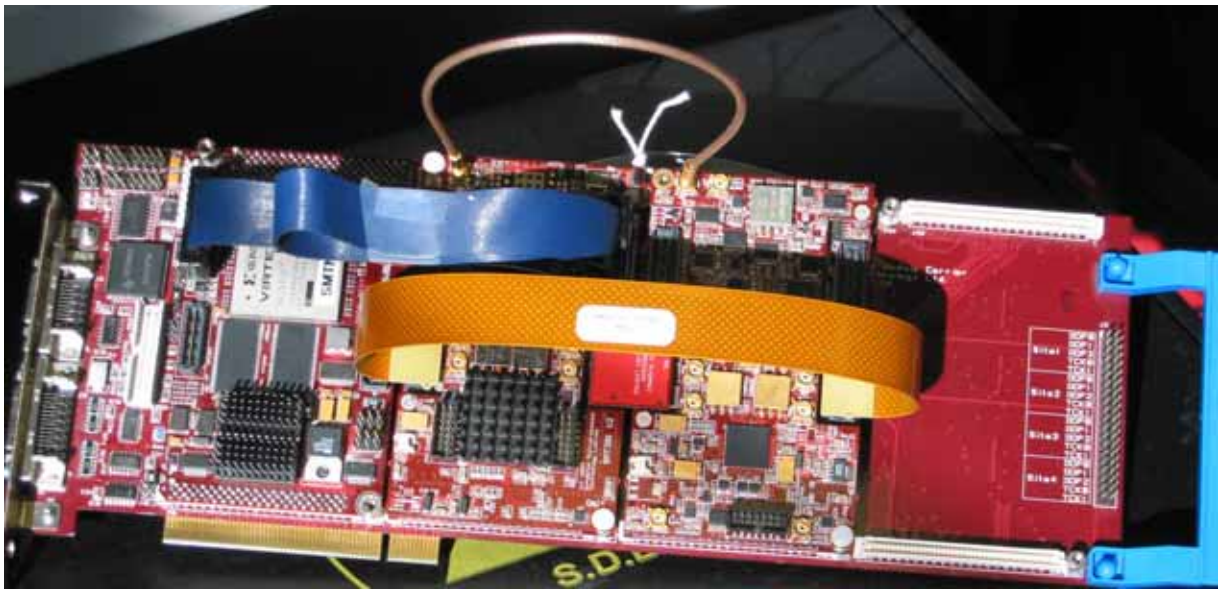


Figure 1: top view of the SMT8101

Figure 2: the cable connections of the SMT8101 system

The following picture shows the CommPort connection at the back of the SMT310Q. Note that the FMS are ‘twisted’, i.e. one end should be blue and the other should show silver pins. (**T1C1** to **T2C3** and **T1C2** to **T3C3**).

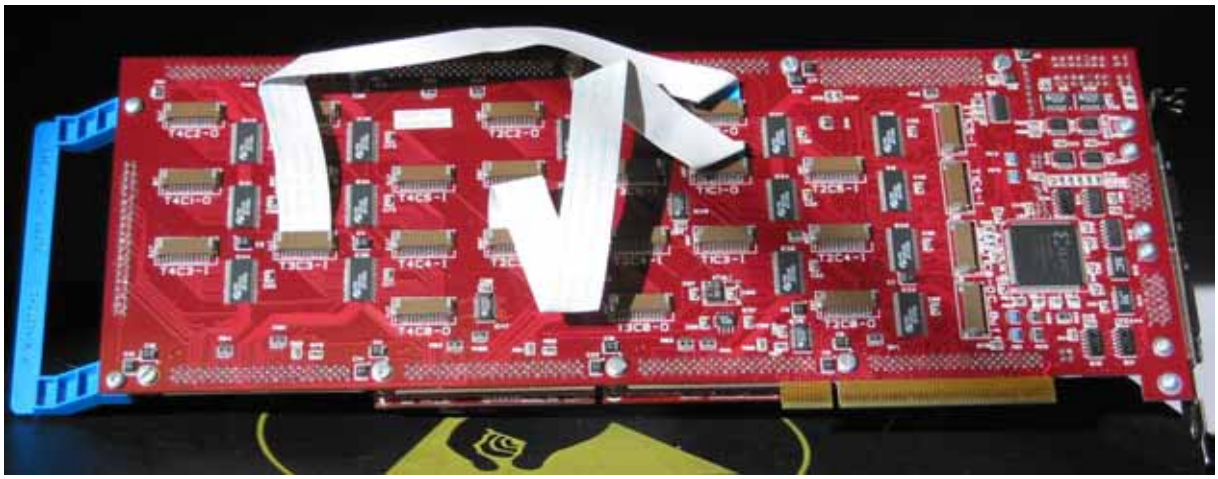


Figure 3: comport connections

Hardware Connections.

Below are listed the connection to be checked before plugging the system in the PC:

FMS connections:

- T1C1 to T2C3,
- T1C2 to T3C3.

SHB connections:

- *SMT395-VP* (SHBA) to *SMT391-VP* (SHBB) using *SMT516*,
- *SMT395-VP* (SHBB) to *SMT391-VP* (SHBA) using *SMT511*.

RSL connections:

- *SMT391-VP* (RSLA) to *SMT381-VP* (RSLB) using *SMT526*,
- *SMT391-VP* (RSLB) to *SMT381-VP* (RSLA) using *SMT522*.

Clock Connection:

- Use an MMBX to MMBX cable to link J8 (*SMT391-VP*) to J5 (*SMT381-VP*). This is to pass the 1GHz clock to the DAC module.

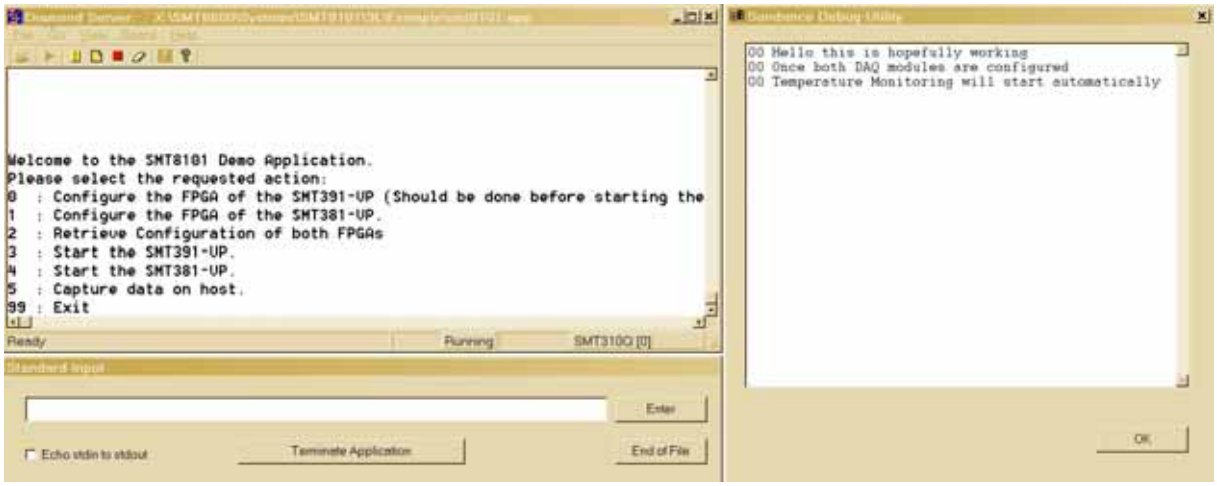
Software applications.

3L application.

In a sub-folder labelled 3L (directory SMT6600\Systems\SMT8101), you will find a C (*SMT8101.c*), a configuration (*SMT8101.cfg*) and a make (*nmake*) files.

In a DOS prompt window, simply type *nmake* to generate the 3L application file, which can be loaded into the *SMT395-VP30* by using the 3L Server (3L Diamond needs to be installed first).

This application allows the user to execute simple commands such as configuring the ADC (output format and scale), the clock synthesizers, clock routing, capturing data, etc.



Description of the functions in the test software menu.

The 3L application provided with the system allows the following option. Some will prompt for a value.

"Configure the FPGA of the SMT391-VP*"*

This command is used to reprogram the *SMT338-VP* (second TIM site - *SMT391-VP*) FPGA with a different/new bitstream.

*"*Configure the FPGA of the SMT381-VP*"*

This command is used to reprogram the second *SMT338-VP* (second TIM site - *SMT381-VP*) FPGA with a different/new bitstream.

"Retrieve configuration of both FPGAs"

This command is used once the FPGAs have already been configured and a reset has occurred. It sends an 'END KEY' (please refer to *SMT338-VP* User Guide) to retrieve the FPGA configurations previously loaded.

This command MUST be executed before using the system.

“Start the SMT391-VP”

This command sends all setting necessary to the *SMT391-VP*.

“Start the SMT381-VP”

This command sends all setting necessary to the *SMT381-VP*.

“Capture Data on HOST”

This command captures data from both SHBs (coming from ADCs) and stores them into files.

What is provided in the *SMT8101* system?

When purchasing an *SMT8101* system, you will get the following (unless stated on order/invoice):

- SMT395-VP30-6,
- SMT310Q,
- *SMT381-VP30-6* (SMT338-VP30-6 and SMT381),
- *SMT391-VP30-6* (SMT338-VP30-6 and SMT391) – Note that the *SMT391* needs to be modified in order to pass its on-board VCO clock to the *SMT381*,
- *Two FMS cable (SMT502),*
- SMT516 (SHB PCB),
- SMT511-320 (SHB Cable 320mm long),
- SMT520-04 (MMBX to BNC cables),
- SMT509-100 (100mm MMBX to MMBX - to feed the SMT391 on-board VCO clock to the *SMT381*),
- SMT526-RSL-IC1 (RSL PCB).
- SMT522-RSL10 (RSL flexi cable – 10 inches long).