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Application Note for SMT911

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Revision History

Issue	Changes Made	Date	Initials
1.0	First Release	26/01/10	C.G.

Table of Contents

1 Introduction

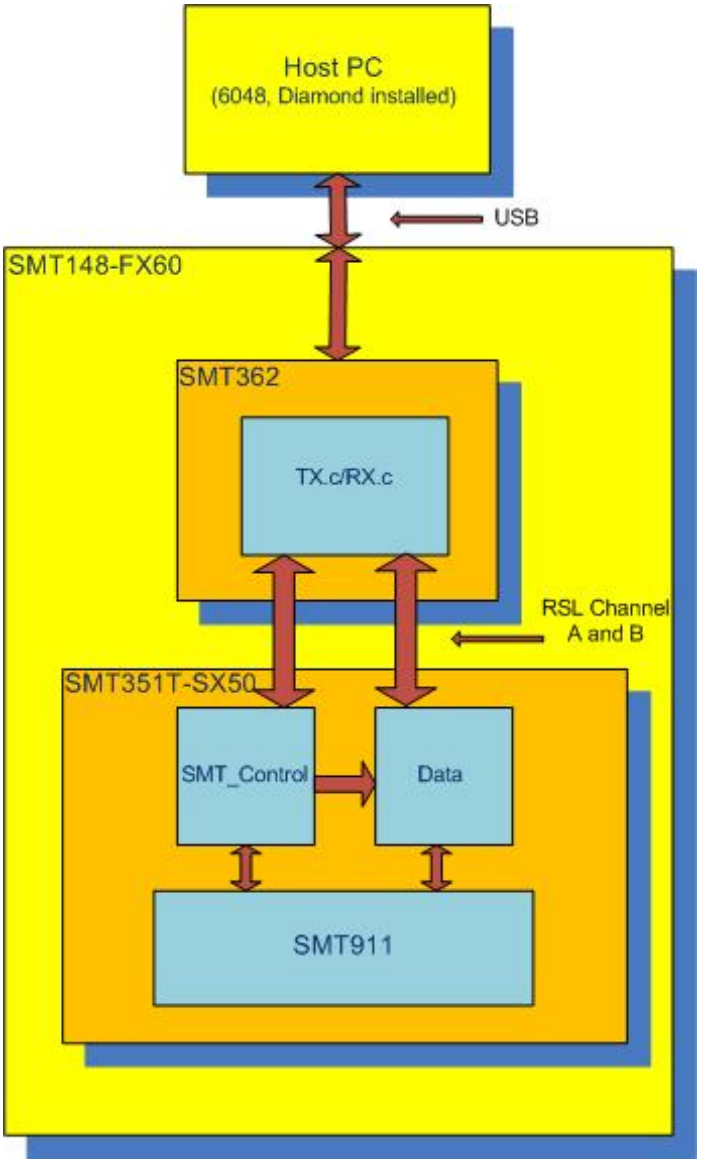
This document describes the SMT911 demo package that comes with the MIMO board.

The purpose of the demo is to check that the board is operating correctly and to give the user a kick-start for building their own application using the SMT911.

This application note describes the SMT911 demo control for a system using one SMT362 + SMT351T on a SMT148-FX.

2 SMT911 System

The major sub-systems and flow of information within the demo described in this application note is depicted in the following diagram:



2.1 Run Time Environment

For this application note, the demo is running on the following system configuration:

(1) Standard PC running Windows XP 32-bit OS with USB connection to

(2) SMT148 populated with an

(3) SMT362 on TIM site 1 and an

(3) SMT351T-SX50 on TIM site 4 attached to an

(4) SMT911 Sundance Local Bus mezzanine module.

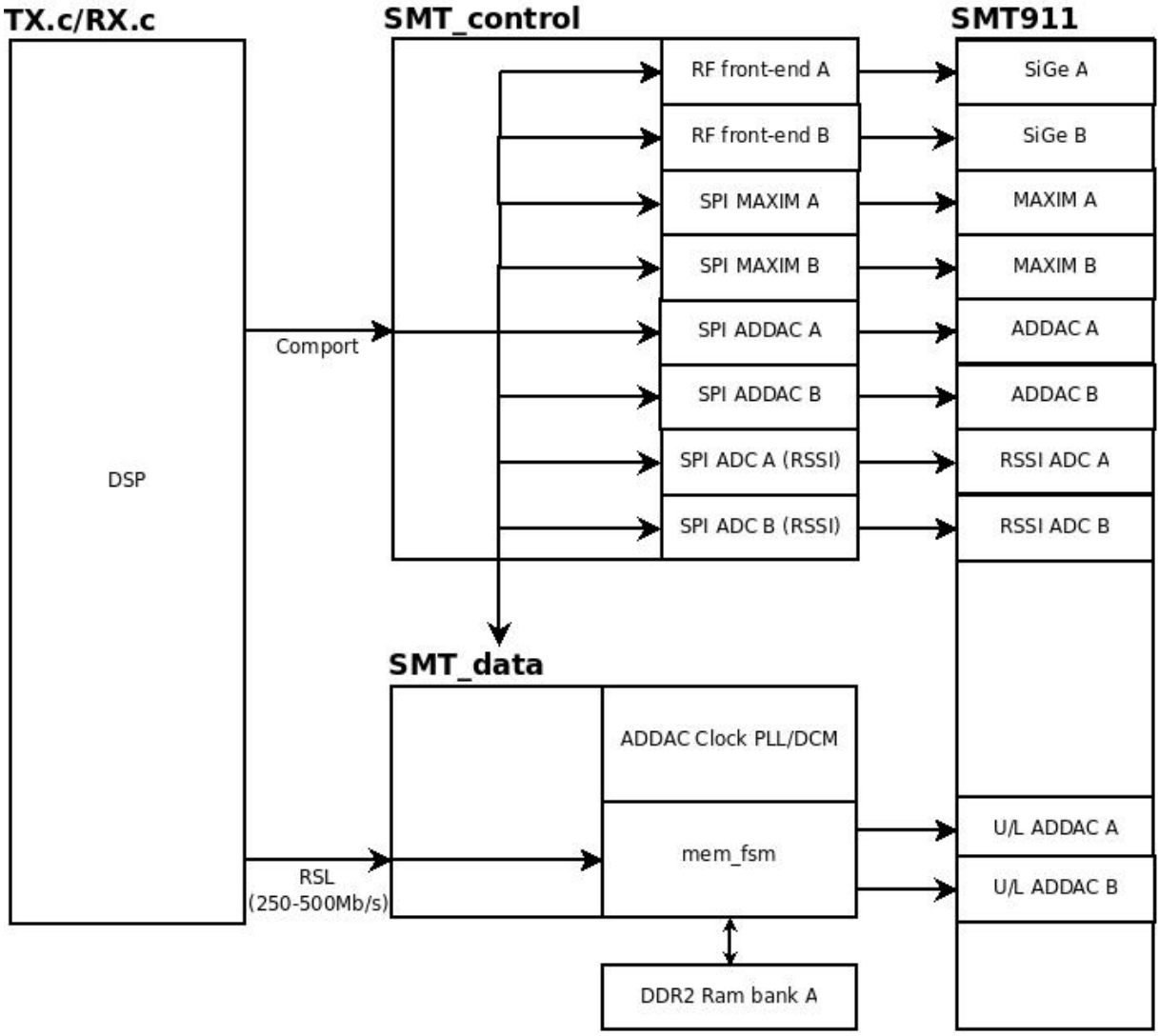
Launching the demo application requires 3L's Diamond software suite to be installed, at the very least the server.

The comport configuration for this SMT148-FX setup is the 'default anti-clockwise'. The latest SMT6048 needs to be installed to connect to the SMT148-FX, and the SMT6002 will be needed if the comport configuration of the carrier needs to be changed. If 'default clockwise' is instead loaded on the carrier, then the SMT351T-SX50 + SMT911 can be alternately moved to TIM site 2, keeping the SMT362 in the same position. (only T1C0 – T4C3 is used)

2.2 Development environment

The demo is provided with all necessary source code to allow you to begin developing your own application right away. It is not meant to demonstrate the full capability of the system, but to provide an example use of the device and example setup for configuration and control. The development environment of choice for this demo is Diamond 3.2.2 and the Diamond IDE. Diamond allows the easy management of multiple tasks in C or VHDL between the DSP's and FPGA's in the system. The use of Diamond to develop applications requires the PC to also have installed TI's Code Composer 3.3 and Xilinx ISE 10.3, although these are not necessary to run the application.

3 Firmware



3.1 Functional Overview

"SMT_control" is an NGC block for receiving instructions from a Sundance DSP module, and passing on these control words to the SMT911 board. Some modules which are integrated in this block are:

· Control Comport: receive instruction words, and send back register contents to DSP.
· Switching Controller: run switching (TX, RX, Standby, etc.) of SMT911 board.
· SPI: send SPI signals to every corresponding chip on the SMT911 board.
· RSSI ADC: convert the RSSI and Power Detection information into register words.

"SMT_data" is a block for data transfer between the ADDAC data pins and a Sundance DSP module through an RSL interface. Using this RSL link, a sustained streaming speed of 250MB/s is possible, or burst transfers of 500MB/s (not taking overhead into consideration). It also receives direct control words from the DSP

module, by getting the forwarded control worlds from the “SMT_control” module. This block is supported by a DDR2 RAM interface available on the SMT351T board for continuous playback in TX mode or as a buffer in RX mode.

3.2 Control Registers

These registers control the complete functionality of the SMT911 transceiver mezzanine. They are set up via Comport 3 of the base module.

3.2.1 Control Packet Structure

The data passed to the FPGA over the Comports must conform to a certain packet structure. Only after a valid packet is accepted and an update command sent will the specified settings be applied. The packet structure is illustrated in the following table.

Packet structure for writing (Byte 0 = 0x10)

	Byte Content							
Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	“0”	“0”	“0”	“1”	“0”	“0”	“0”	“0”
1	Address7	Address6	Address5	Address4	Address3	Address2	Address1	Address0
2	Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8
3	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0

Packet structure for reading (Byte 0 = 0x20)

	Byte Content							
Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	“0”	“0”	“1”	“0”	“0”	“0”	“0”	“0”
1	Address7	Address6	Address5	Address4	Address3	Address2	Address1	Address0
2	Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8
3	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0

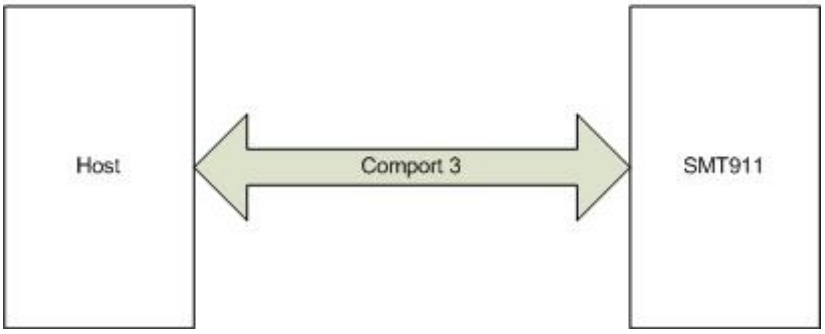
Byte 0 of a packet must be 0x10 (for writing register) or 0x20 (for reading register). This byte indicates the start of a packet and is required to synchronize communication. Byte 1 denotes the register address to be accessed. Byte 2 is the upper 8 bits of the data to the written or read, and Byte 3 is the lower 8 bits of the data to be written or read, creating 16-bit data words.

3.2.2 Reading and Writing Registers

Control packets are sent to the base module over Comport 3. This Comport is a 32-bit bi-directional interface, so all four control bytes are written and read as one word.

Packet Structure

Byte 0	Command Sequence
Byte 1	Read/Write Address
Byte 2	Read/Write Data
Byte 3	Read/Write Data



3.2.3 Register Map

Greater detail on each register can be found in the Appendix.

Address	Register Definition	Read/Write	Address	Register Definition	Read/Write
0x00	Reset Register	W	0x1B	ADDAC A Register 2	R/W
0x01	Test Register	R/W	0x1C	ADDAC A Register 3	R/W
0x02	Function Register 0	R/W	0x1D	ADDAC A Register 4	R/W
0x03	Function Register 1	R/W	0x1E	ADDAC A Register 5	R/W
0x04	Function Register 2	R/W	0x1F	ADDAC A Register 6	R/W
0x05	MAXIM A Register 0	R/W	0x20	ADDAC A Register 7	R/W
0x06	MAXIM A Register 1	R/W	0x21	ADDAC A Register 8	R/W
0x07	MAXIM A Register 2	R/W	0x22	ADDAC A Register 9	R/W
0x08	MAXIM A Register 3	R/W	0x23	ADDAC A Register 10	R/W
0x09	MAXIM A Register 4	R/W	0x24	ADDAC A Register 11	R/W
0x0A	MAXIM A Register 5	R/W	0x25	ADDAC B Register 0	R/W
0x0B	MAXIM A Register 6	R/W	0x26	ADDAC B Register 1	R/W
0x0C	MAXIM A Register 7	R/W	0x27	ADDAC B Register 2	R/W
0x0D	MAXIM A Register 8	R/W	0x28	ADDAC B Register 3	R/W
0x0E	MAXIM A Register 9	R/W	0x29	ADDAC B Register 4	R/W
0x0F	MAXIM B Register 0	R/W	0x2A	ADDAC B Register 5	R/W
0x10	MAXIM B Register 1	R/W	0x2B	ADDAC B Register 6	R/W
0x11	MAXIM B Register 2	R/W	0x2C	ADDAC B Register 7	R/W
0x12	MAXIM B Register 3	R/W	0x2D	ADDAC B Register 8	R/W
0x13	MAXIM B Register 4	R/W	0x2E	ADDAC B Register 9	R/W
0x14	MAXIM B Register 5	R/W	0x2E	ADDAC B Register 10	R/W
0x15	MAXIM B Register 6	R/W	0x30	ADDAC B Register 11	R/W
0x16	MAXIM B Register 7	R/W	0x31	Update Register	R=FW/W=SPI
0x17	MAXIM B Register 8	R/W	0x32	Update RSSI Register	W
0x18	MAXIM B Register 9	R/W	0x33	RSSI Channel A	R
0x19	ADDAC A Register 0	R/W	0x34	RSSI Channel B	R
0x1A	ADDAC A Register 1	R/W			

3.3 Running the Demo

The ‘SMT911_Control.ngc’ provides a ready to use interface for configuring the registers of the mezzanine and switching between various states. This should not need any modification when developing custom tasks, although new tasks or the ‘Data’ task can be modified any number of ways to create custom hardware processing.

In the DSP task is an array called ‘BlockofRegisters[]’ which has all the default register configuration settings loaded at start-up. Details on the registers and the structure for writing to specific fields can be found in the appendix. The datasheets for the AD9863 and the MAXIM 2829 will offer further detailed information on what each setting in these registers will do, and the format for writing to these registers can be found in the header file for this task.

The applications depend on a couple folders being available, so these must be set up first. On the ‘C’ drive, make a new folder called ‘SMT911 Data’, and in this folder create a folder called ‘Received Data’. The resulting path should be:

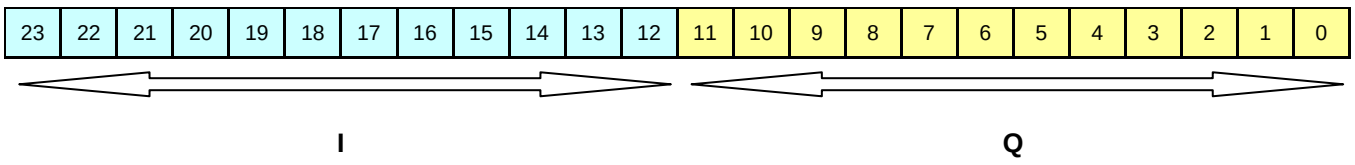
C:\SMT911 Data\Received Data\

Take the provided ‘SINE.dat’ file and place it within the ‘SMT911 Data’ folder. This is the sample data file which the DSP will look for when loading the DDR memory for transmit.

For both demo’s, leave the jumpers off of the mezzanine to choose the onboard crystal as the clock source, otherwise a larger system can be synchronized using an external clock.

3.3.1 System As Transmitter

The data file used when the module is configured as a transmitter must be formatted so that each line provides a concatenated I/Q pair for the dual DAC’s of each channel. Each line will be read into the DSP and passed to the FPGA as straight unsigned binary, with the first 12 bits corresponding to the ‘Q’ value, and the next 12 bits corresponding to the ‘I’ value. The following figure demonstrates this:



To load the module as a transmitter, open a Diamond Server and launch ‘SMT911_362_SX50T_TX.app’. The application will begin by resetting the module for correct initialization, then writing the default configuration settings to the registers mapped in the FPGA. They are then double checked and written from the FPGA to the mezzanine via SPI, at which time the module is placed in Standby and a menu is presented. At this point, all four LED’s on the SMT351T-SX50 should be on:

D5: MAXIM channel A good LO clock lock

D4: MAXIM channel B good LO clock lock

D3: DDR2 memory initialized successfully

D2: Good clock lock from both AD9863 IC's to the FPGA PLL

To step right through the demo using default settings, press '3' to load the 'SINE.dat' file into the DDR2 memory of the SMT351T-SX50, and then press '1' to place the mezzanine into TX mode and repeatedly playback the stored memory wave. The buffer that is created in the DSP's memory to store the data file needs to be the same size as the number of samples in the data file. If a custom waveform is to be selected for playback, this can be set at the top of the header file in the DSP task by:

```
#define TxBUFSIZE          128
```

By default, the sine wave stored in memory will be played onto both channels A and B of the mezzanine, but this can be altered in the 'Data_TX.c' file in the DSP task.

To adjust the gain or to select a different carrier frequency, simply choose the corresponding menu option and follow the directions as presented on screen. To quit the application, press '9'.

3.3.2 System As Receiver

The receiver application works much the same way as the transmitter. Open a Diamond Server and launch 'SMT911_362_SX50T_RX.app'. The mezzanine will reset and initialize the mezzanine into Standby, then write all the configuration registers in the FPGA with the default settings provided from 'BlockofRegisters[]'. These are next double checked, and written via SPI to the ADC and transceiver IC's. At this point a menu similar to the transmitter application should be presented, and all four LED's on the SMT351T-SX50 should be on:

D5: MAXIM channel A good LO clock lock

D4: MAXIM channel B good LO clock lock

D3: DDR2 memory initialized successfully

D2: Good clock lock from both AD9863 IC's to the FPGA PLL

To step through a simple capture from the module, press '1' to turn on the receiver. Next press '5' to store a number of samples to the DDR2 memory of the FPGA base module, and finally '6' to read the memory from the base module into a set of files in 'C:\SMT911 Data\Received Data\' called: 'RxA_I.log', 'RxA_Q.log', 'RxB_I.log' and 'RxB_Q.log'. The number of samples to be stored to file is changeable at the top of the header file in the DSP task as:

```
#define DATALENGTH      (30*1024)
```

Keep in mind if more samples are attempted to be written to file than is stored in memory, the server will halt and the application will need to be restarted.

The user is then free to analyze the data with their preferred application, or the provided MATLAB script 'Test_RX.m' can then be used to view the captured waveforms.

To adjust the gain, monitor RSSI, or select a different carrier frequency, simply choose the corresponding menu option and follow the directions as presented on screen. To quit the application, press '9'.

4 Appendix

4.1 2.4GHz Frequency Plan and Divider Ratio Programming Words

fRF MHZ	(fRF x 4/3) /20MHz Divider Ratio	Integer-Divider Ratio	Fractional-Divider Ratio	
		Reg 0x06, B7-B0	Reg 0x07, B13-B0 (HEX)	Reg 0x06, B13-B12
2412	160.8000	1010 0000	3333	00
2417	161.1333	1010 0001	0888	10
2422	161.4667	1010 0001	1DDD	11
2427	161.8000	1010 0001	3333	00
2432	162.1333	1010 0010	0888	10
2437	162.4667	1010 0010	1DDD	11
2442	1628000	1010 0010	3333	00
2447	163.1333	1010 0011	0888	10
2452	163.4667	1010 0011	1DDD	11
2457	163.8000	1010 0011	3333	00
2462	164.1333	1010 0100	0888	10
2467	164.4667	1010 0100	1DDD	11
2472	164.8000	1010 0100	3333	00
2484	165.6000	1010 0101	2666	01

4.2 5GHz Frequency Plan and Divider Ratio Programming Words

fRF MHZ	(fRF x 4/3) /20MHz Divider Ratio	Integer-Divider Ratio	Fractional-Divider Ratio	
		Reg 0x06, B7-B0	Reg 0x07, B13-B0 (HEX)	Reg 0x06, B13-B12
5180	207.2	1100 1111	0CCC	11
5200	208.0	1101 0000	0000	00
5220	208.8	1101 0000	3333	00
5240	209.6	1101 0001	2666	01
5260	210.4	1101 0010	1999	10
5280	211.2	1101 0011	0CCC	11
5300	2122.0	1101 0100	0000	00
5320	212.8	1101 0100	3333	00
5500	220.0	1101 1100	0000	00
5520	220.8	1101 1100	3333	00
5540	221.6	1101 1101	2666	01
5560	222.4	1101 1110	1999	10
5580	223.2	1101 1111	0CCC	11
5600	224.0	1110 0000	0000	00
5620	224.8	1110 0000	3333	00
5640	225.6	1110 0001	2666	01
5660	226.4	1110 0010	1999	10
5680	227.2	1110 0011	0CCC	11
5700	228.0	1110 0100	0000	00
5745	229.8	1110 0101	3333	00
5765	230.6	1110 0110	2666	01
5785	231.4	1110 0111	1999	10
5805	232.2	1110 1000	0CCC	11

4.3 Reset Register 0x00

This register resets some of the components. In order to save on power, the components will remain in reset until the register is cleared.

Reset Register 0x00																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Reconfigurable bits:

Bit	Default	Description
1	**0**	ADQ A & B reset, '1' = reset, '0' = normal operation
0	**0**	Transceiver A & B Reset ; "1"= reset, "0" = normal operation

4.4 Test Register 0x01

Any 16-bit word can be written and read from this register to verify proper operation of the Comport.

Test Register 0x01																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	1	1	1	1	0	0	0	0	1	0	1	0	1	0	1	0

4.5 Function Register 0 – 0x02

This register allows the basic setup of the SMT911 transceiver card; including activating MIMO operation, choosing the frequency band, selecting memory, and defining TX or RX operation.

Function Register 0 0x02																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Reconfigurable bits:

Bit	Default	Description
3	**0**	"0" =use memory (DDR2 RAM) , "1" = no memory (direct transfer)
2	**0**	Working mode. "1" = Receiver, "0" = Transmitter
1	**1**	Frequency range. "0" = 2.4 GHz (802.11g), "1" = 5.2 GHz (802.11a)
0	**1**	MIMO activation. '0' = SISO mode (only path A) '1' = MIMO active.

4.6 Function Register 1 – 0x03

This register controls the switching of the SMT911; either active (TX/RX) or standby

Function Register 1 0x03																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
7	0	'1' = write to memory, '0' = stop write to memory
6	0	'1' = read from memory, '0' = don't read from memory
5	0	"000000" = standby "111111" = active (actual working mode depends on register 0x02
4	0	
3	0	
2	0	
1	0	
0	0	

4.7 Function Register 2 – 0x04

By default, the gain control is applied through the parallel digital inputs of the MAXIM chips. This register is used to set these digital inputs.

Function Register 2 0x04																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
13	0	Bit 13:Bit 7 are digital gain control of MAXIM B As Receiver: B13:B12 are used for Rx LNA gain control. 00"&"01" = minimum, "10" = medium, "11" = maximum. B11:B7 are used for Rx VGA gain control. "00000" = 0 dB (minimum), "11111" = 62 dB (maximum). As Transmitter: B13 is not used, B12:B7 is used for Tx VGA gain control. "000000" = 0 dB (minimum), "111111" = 30 dB (maximum)
12	0	
11	0	
10	0	
9	0	
8	0	
7	0	
6	0	Bit6:Bit0, are digital gain control for MAXIM A. As Receiver: B6:B5 are used for Rx LNA gain control. "00"&"01" = minimum, "10" = medium, "11" = maximum. B4:B0 are used for Rx VGA gain control. "00000" = 0 dB (minimum), "11111" = 62 dB (maximum). As Transmitter: B6 is not used, B5:B0 is used for Tx VGA gain control. "000000" = 0 dB (minimum), "111111" = 30 dB (maximum)
5	0	
4	0	
3	0	
2	0	
1	0	
0	0	

4.8 MAXIM A Register 0 – 0x05 (Standby)

Various internal blocks of the MAXIM chip can be turned on or off by setting this standby register. Setting bit 13 to 1 turns the clock on, while setting it to 0 turns the block off.

MAXIM A Register 0 0x05																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1

Reconfigurable bits:

Bit	Default	Description
13	1	MIMO mode: '0' = normal operation, '1' = MIMO applications
11	0	Voltage Reference
10	0	PA Bias DAC, in TX Mode

4.9 MAXIM A Register 1 – 0x06 (Integer-Divider Ration)

This register contains the integer portion of the divider ratio of the synthesizer. This register in conjunction with the fractional-divider ratio register, permits selection of a precise frequency. Please refer to the appendix tables.

MAXIM A Register 1 0x06																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	1	1	0	0	0	0	1	0	1	0	0	0	1	1

Reconfigurable bits:

Bit	Default	Description
13	**1**	2 LSBs of the Fractional-Divider Ratio
12	**1**	
7	**1**	Integer-Divider Ratio Word Programming Bits. Valid values are from 128(Bit7:Bit0 = “10000000”) to 255 (Bit7:Bit0 = “11111111”)
6	**0**	
5	**1**	
4	**0**	
3	**0**	
2	**0**	
1	**1**	
0	**0**	

4.10 MAXIM A Register 2 – 0x07 (Fractional-Divider Ratio)

This register (along with bit 13 and bit 12 of the integer divider ratio register) controls the fractional-divider ratio with 16-bit resolution. Bit 13 to bit 0 of this register combined with bit 13 and bit 12 of the integer-divider ratio register form the whole fractional-divider ratio. To retain the complete frequency plan please refer to the appendix tables.

MAXIM A Register 2 0x07																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	1	1	1	0	1	1	1	0	1	1	1	0	1

Reconfigurable bits:

Bit	Default	Description
13	**0**	Bit0:Bit13 = refer to Appendix : Frequency Plan and Divider Ratio Programming Words
12	**1**	
11	**1**	
10	**1**	
9	**1**	
8	**1**	
7	**1**	
6	**1**	
5	**0**	
4	**1**	
3	**1**	
2	**1**	
1	**0**	
0	**1**	

4.11 MAXIM A Register 3 – 0x08 (Band Select and PLL)

This register configures the programmable-reference frequency dividers for the

synthesizer, and sets the DC current for the charge pump. The programmable reference frequency divider provides the reference frequency to the phase detector by dividing the signal of the crystal oscillator.

MAXIM A Register 3 0x08																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	1	1	1	0	0	0	0	0	1	0	0	1	0	0

Reconfigurable bits:

Bit	Default	Description
13	**0**	'0' = normal operation, '1' = MIMO applications
10	**0**	These Bits set the VCO Sub-Band when programmed by using SPI (Bit8=1).
9	**0**	"00" = lowest frequency band; "11" = highest frequency band.
8	**0**	VCO SPI Bandswitch Enable. "0" = disable SPI control, bandswitch is done by FSM; "1" = bandswitch is done by SPI programming.
7	**0**	VCO Bandswitch Enable. "0" = disable; "1" = start automatic bandswitch.
6	**0**	RF Frequency Band Select in 802.11a Mode (Bit0=1). "0" = 4.9GHz to 5.35GHz band; "1" = 5.47GHz to 5.875GHz Band.
5	**0**	PLL Charge-Pump-Current Select. "0" = 2mA, "1" = 4mA.
3	**0**	These Bits Set the Reference-Divider Ratio. "001" corresponds to R = 1 and "111" corresponds to R = 7.
2	**0**	
1	**0**	
0	**0**	RF Frequency Band Select. "0" = 2.4GHz Band; "1" = 5GHz band.

4.12 MAXIM A Register 4 – 0x09 (Calibration)

This register configures the TX/RX calibration modes.

MAXIM A Register 4 0x09																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
12	**1**	Transmitter I/Q Calibration LO Leakage and Sideband-Detector Gain-Control Bits.
11	**1**	"00" = 8 dB; "01" = 18 dB; "10" = 24 dB; "11" = 34 dB
1	**0**	"0" = TX Calibration Mode Disabled; "1" = TX Calibration Mode Enabled
0	**0**	"0" = RX Calibration Mode Disabled; "1" = RX Calibration Mode Enabled

4.13 MAXIM A Register 5 – 0x0A (Low-pass Filter)

This register allows the adjustment of the RX and TX low-pass filter corner frequencies

MAXIM A Register 5 0x0A																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Reconfigurable bits:

Bit	Default	Description
11	**0**	RSSI High Bandwidth Enable. "0" = 2 MHz; "1" = 6MHz
6	**0**	TX LPF Corner Frequency Coarse Adjustment. "00" = undefined; "01" = 12MHz (nominal
5	**0**	mode); "10" = 18MHz (turbo mode 1); "11" = 24MHz (turbo mode 2).
4	**0**	RX LPF Corner Frequency Coarse Adjustment. "00" = 7.5MHz; "01" = 9.5MHz (nominal
3	**0**	mode); "10" = 14 MHz (turbo mode 1); "11" = 18MHz (turbo mode 2).
2	**0**	

1	**0**	RX LPF Corner Frequency Fine Adjustment (Relative to the Course Setting).
0	**0**	"000" = 90%; "001" = 95%; "010" = 100%; "011" = 105%; "100" =110%.

4.14 MAXIM A Register 6 – 0x0B (RX Control/RSSI)

This register is used to adjust the RX section and RSSI output.

MAXIM A Register 6 0x0B															
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1

Reconfigurable bits:

Bit	Default	Description
12	**0**	Enable Rx VGA Gain Programming Serially. "0" = Rx VGA gain programmed with external digital inputs (B7:B1); "1" = Rx VGA gain programmed with serial data bits in the Rx gain register (D6:D0).
11	**0**	RSSI Output Range. "0" = low range (0.5V to 2V); "1" = high range (0.5V to 2.5V).
10	**0**	RSSI Operating Mode. "0" = RSSI disabled if RXHP = 0, and enabled if RXHP = 1; "1" = RSSI enabled independent of RXHP
8	**0**	RSSI Pin Function. "0" = outputs RSSI signal in Rx mode; "1" = outputs temperature sensor voltage in Rx, Tx and standby modes.
2	**1**	Rx high-pass -3dB Corner Frequency when RXHP = 0. "0" = 100Hz; "1" = 30kHz

4.15 MAXIM A Register 7 – 0x0C (TX Linearity/Gain)

This register allows the adjustment of the TX gain and linearity

MAXIM A Register 7 0x0C															
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
10	**0**	Enable Tx VGA Gain Programming Serially. "0" = Tx VGA gain programmed with external digital inputs (B6:B1); "1" = Tx VGA gain programmed with data bits in the Tx gain register (D5:D0).
9	**1**	PA Driver linearity. "00" = 50% current (minimum linearity); "01" = 63% current; "10" = 78% current; "11" = 100% current (maximum linearity)
8	**0**	
7	**0**	Tx VGA linearity. "00" = 50% current (minimum linearity); "01" = 63% current; "10" = 78% current; "11" = 100% current (maximum linearity)
6	**0**	
3	**0**	Tx Upconverter Linearity. "00" = 50% current (minimum linearity); "01" = 63% current; "10" = 78% current; "11" = 100% current (maximum linearity).
2	**0**	
1	**0**	Tx Base-band Gain. "00" = max base-band gain -5dB; "01" = max base-band gain -3dB; "10" = max base-band gain -1.5dB; "11" = max base-band gain.
0	**0**	

4.16 MAXIM A Register 8 – 0x0D (RX Gain)

This register sets the RX base-band gain and RF gain when MAXIM A Register 6 Bit12 = '1'.

MAXIM A Register 8 0x0D															
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Reconfigurable bits:

Bit	Default	Description
6	1	Rx base-band and RF gain-control bits. Bit 6 maps to digital input pin B1. Bit6:BitD0 = “0000000” corresponds to minimum gain.
5	1	
4	1	
3	1	
2	1	
1	1	
0	1	

4.17 MAXIM A Register 9 – 0x0E (TX VGA Gain)

This register sets the TX VGA gain when MAXIM A Register 7 Bit10 = ‘1’.

MAXIM A Register 9 0x0E																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
5	0	For faster Tx VGA gain setting, only Bit5:Bit0 need to be programmed. Tx VGA Gain Control. Bit5 maps to digital input pin B6 and Bit0 maps to digital input pin B1. Bit5:Bit0 = “000000” corresponds to minimum gain.
4	0	
3	0	
2	0	
1	0	
0	0	

4.18 MAXIM B Register 0 – 0x0F (Standby)

Same settings as MAXIM A. See corresponding register.

4.19 MAXIM B Register 1 – 0x10 (Integer-Divider Ratio)

Same settings as MAXIM A. See corresponding register.

4.20 MAXIM B Register 2 – 0x11 (Fractional-Divider Ratio)

Same settings as MAXIM A. See corresponding register.

4.21 MAXIM B Register 3 – 0x12 (Band Select and PLL)

Same settings as MAXIM A. See corresponding register.

4.22 MAXIM B Register 4 – 0x13 (Calibration)

Same settings as MAXIM A. See corresponding register.

4.23 MAXIM B Register 5 – 0x14 (Low-pass Filter)

Same settings as MAXIM A. See corresponding register.

4.24 MAXIM B Register 6 – 0x15 (RX Control/RSSI)

Same settings as MAXIM A. See corresponding register.

4.25 MAXIM B Register 7 – 0x16 (TX Linearity/Gain)

Same settings as MAXIM A. See corresponding register.

4.26 MAXIM B Register 8 – 0x17 (RX Gain)

Same settings as MAXIM A. See corresponding register.

4.27 MAXIM B Register 9 – 0x18 (TX VGA Gain)

Same settings as MAXIM A. See corresponding register.

4.28 ADDAC A Register 0 – 0x19

This register is used for general setting and clock mode of ADDAC A.

ADDAC A Register 0 0x19																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
15	**0**	Clock Mode setting. “000” standard FD, HD10, HD20 (modes 1,4,7); “001” Optional FD timing (mode 2) ; “010” not used; “011” Optional HD20 timing (mode 5); “100” not used; “101” Optional HD10 timing (mode 8); “110” not used; “111” Clone Mode (mode 10)
14	**0**	
13	**0**	
10	**0**	Enable the IFACE2 port to be an output clock
9	**0**	Inv the output clock on IFACE3
7	**0**	SDIO pin. “0” = uni-directional ; “1” = bidirectional
6	**0**	SPI Mode. “0” = MSB; “1” = LSB
5	**0**	Soft Reset. “0” = not reset; “1” = reset register to default value

4.29 ADDAC A Register 1 – 0x1A

This register is used to set Power-Down mode of ADDAC A.

ADDAC A Register 1 0x1A																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
15	**0**	Rx_A Analog Power-Down. “0” = active; “1” = Power-down
14	**0**	Rx_A DC Bias Analog Power-Down. “0” = active; “1” = Power-down
7	**0**	Power Down Tx Analog. “000” = default; “100 = Power down Tx A; “010” = Power-Down Tx B; “111 = Power-Down Tx A and Tx B
6	**0**	
5	**0**	
4	**0**	Tx Digital Power-Down. “0” = active; “1” = Power-down
3	**0**	Rx Digital Power-Down. “0” = active; “1” = Power-down
2	**0**	PLL Power-Down. “0” = active; “1” = Power-down
1	**0**	PLL Output Disconnect. “0” = connect; “1” = disconnect

4.30 ADDAC A Register 2 – 0x1B

This register is used to set Power-Down of ADDAC A.

ADDAC A Register 2 0x1B																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
15	0	Rx Analog Bias Power-Down. “0” = active; “1” = Power-Down
14	0	RxRef Power-Down. “0” = active; “1” = Power-Down
13	0	DiffRef Power-Down. “0” = active; “1” = Power-Down
12	0	VREF Power-Down. “0” = active; “1” = Power-Down
7	0	Rx_B Analog Power-Down. “0” = active; “1” = Power-down
6	0	Rx_B DC Bias Power-Down. “0” = active; “1” = Power-down

4.31 ADDAC A Register 3 – 0x1C

This register is used to set Rx Path of ADDAC A.

ADDAC A Register 3 0x1C																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
13	0	Rx_B 2’s complement. “0” = straight binary; “1” = 2’s complement
12	0	Rx_B Clk Duty. “0” = disable; “1” = enable
5	0	Rx_A 2’s complement. “0” = straight binary; “1” = 2’s complement
4	0	Rx_A Clk Duty. “0” = disable; “1” = enable

4.32 ADDAC A Register 4 – 0x1D

This register is used to set Ultra low power control of Rx path of ADDAC A, in combination with asserting the ADC_LO_PWR pin to reduce power consumption.

ADDAC A Register 4 0x1D																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
14	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow
13	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow
12	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow
3	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow
2	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow

4.33 ADDAC A Register 5 – 0x1E

This register is used to set Ultra low power control of Rx path and DAC A Offset of ADDAC A.

ADDAC A Register 5 0x1E																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
15	0	DAC A Offset [9:2]
14	0	
13	0	
12	0	
11	0	
10	0	
9	0	
8	0	
6	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow
5	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow
4	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow

4.34 ADDAC A Register 6 – 0x1F

This register is used for DAC A offset and DAC A gain control of ADDAC A.

ADDAC A Register 6 0x1F																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
15	0	DAC A Coarse Gain Control. “00” = output current scaling by 1/11; “01” = output current
14	0	scaling by ½; “10” and “11” = no output current scaling
13	0	DAC A Fine Gain [5:0] := “100000” Maximum positive gain adjustment;
12	0	“111111” Minimum positive gain adjustment;
11	0	“000000” default of no adjustment;
10	0	“000001” Minimum negative gain adjustment;
9	0	“011111” Maximum negative gain adjustment
8	0	
7	0	DAC A Offset [1:0]
6	0	
0	0	DAC A Offset Direction. “0” = to negative diff. pin; “1” = to positive diff. pin

4.35 ADDAC A Register 7 – 0x20

This register is used for DAC B offset and its direction of ADDAC A.

ADDAC A Register 7 0x20																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
15	0	DAC B Offset [1:0]
14	0	
8	0	DAC B Offset Direction. “0” = to negative diff. pin; “1” = to positive diff. pin
7	0	DAC B Offset [9:2]
6	0	
5	0	
4	0	
3	0	
2	0	
1	0	
0	0	

4.36 ADDAC A Register 8 – 0x21

This register is used for DAC B offset gain control, fine gain, and TxPGA gain of ADDAC A.

ADDAC A Register 8 0x21																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
15	**1**	TxPGA Gain [7:0], is register control for the Tx programmable gain amplifier (TxPGA). The TxPGA provides a 20 dB continuous gain range with 0.1 dB steps (linear in dB) simultaneously to both Tx channels. Default is 0xFF. "0000 0000" = Minimum gain scaling -20 dB "1111 1111" = Maximum gain scaling 0dB
14	**1**	
13	**1**	
12	**1**	
11	**1**	
10	**1**	
9	**1**	
8	**1**	
7	**0**	DAC B Coarse Gain Control. "00" = output current scaling by 1/11; "01" = output current scaling by ½; "10" and "11" no output current scaling
6	**0**	
5	**0**	DAC B Fine Gain [5:0] := "100000" Maximum positive gain adjustment; "111111" Minimum positive gain adjustment; "000000" default of no adjustment; "000001" Minimum negative gain adjustment; "011111" Maximum negative gain adjustment
4	**0**	
3	**0**	
2	**0**	
1	**0**	
0	**0**	

4.37 ADDAC A Register 9 – 0x22

This register is used for other settings of Tx Path and I/O configuration of ADDAC A.

ADDAC A Register 9 0x22																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
15	**0**	Tx Twos Complement. "0" = straight binary; "1" = twos complement
14	**0**	Rx Twos Complement. "0" = straight binary; "1" = twos complement
13	**0**	Tx Inverse Sample. "0" = sampled on rising edge; "1" = sampled on falling edge clock
9	**0**	Interpolation control. "00" = filters bypassed; "01" = interpolation rate 2x; "10" = interpolation rate 4x.
8	**0**	
6	**0**	TxPGA Slave Enable. "0" = immediately after register updated; "1" = synchronized with falling edge of a signal applied to the TxPwrDwn
4	**0**	TxPGA Fast Update. "0" = normal mode; "1" = fast mode

4.38 ADDAC A Register 10 – 0x23

This register is used for I/O configuration and clock configuration of ADDAC A.

ADDAC A Register 10 0x23																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
15	0	PLL Bypass. “0” = PLL remains active; “1” = PLL bypassed
13	0	ADC Clock Div. “0” = no division; “1” = divides the clock by 2
12	0	Alt timing mode. “0” = normal timing operation; “1” = alternative operation mode
11	0	PLL Div5. “0” = no division; “1” = output of PLL divided by 5
10	0	PLL multiplication factor. “000” = 1x; “001” = 2x; “010” = 4x; “011” = 8x; “100” = 16x; “101” ~ “111”: not used.
9	0	
8	0	
5	0	Dig Loop On. “0” = off; “1” = on (on only in full duplex mode)
4	0	SpiFDnHD. “0” = HD mode; “1” = FD mode
3	0	SpiTxnRx for toggling Tx & Rx in HD mode. “0” = Rx; “1” = Tx
2	0	SpiB10n20, option for 10 or 20 bit. “0” = 20-bit; “1” = 10-bit
1	0	SPI IO Control, in conjunction with Bit3 to override external TxnRx pin operation
0	0	SpiClone. “1” = for clone mode; “0” = other

4.39 ADDAC A Register 11 – 0x24

This register is used for configuring the rest of the clock settings of ADDAC A.

ADDAC A Register 11 0x24																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits:

Bit	Default	Description
5	0	PLL to IFACE2. “0” = IFACE2 normal; “1” = IFACE2 switched to PLL output clock (FD)
2	0	PLL Slow. “0” = standard; “1” = changes phase noise generated from the PLL clock

4.40 ADDAC B Register 0 – 0x25

Same settings as ADDAC A. See corresponding register.

4.41 ADDAC B Register 1 – 0x26

Same settings as ADDAC A. See corresponding register.

4.42 ADDAC B Register 2 – 0x27

Same settings as ADDAC A. See corresponding register.

4.43 ADDAC B Register 3 – 0x28

Same settings as ADDAC A. See corresponding register.

4.44 ADDAC B Register 4 – 0x29

Same settings as ADDAC A. See corresponding register.

4.45 ADDAC B Register 5 – 0x2A

Same settings as ADDAC A. See corresponding register.

4.46 ADDAC B Register 6 – 0x2B

Same settings as ADDAC A. See corresponding register.

4.47 ADDAC B Register 7 – 0x2C

Same settings as ADDAC A. See corresponding register.

4.48 ADDAC B Register 8 – 0x2D

Same settings as ADDAC A. See corresponding register.

4.49 ADDAC B Register 9 – 0x2E

Same settings as ADDAC A. See corresponding register.

4.50 ADDAC B Register 10 – 0x2F

Same settings as ADDAC A. See corresponding register.

4.51 ADDAC B Register 11 – 0x30

Same settings as ADDAC A. See corresponding register.

4.52 Update Register 0x31

The Update bit activates the serial interface (SPI) to pass registers previously written in the FPGA to the corresponding device (MAXIM A and B, and ADDAC A and B).

Update Register 0x31																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Reading back this register returns the Firmware version.

Update Register 0x31																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	Firmware Version							

Reconfigurable bits:

Bit	Default	Description
3	**1**	ADDAC B Update. “0” = not updated; “1” = updated
2	**1**	ADDAC A Update. “0” = not updated; “1” = updated
1	**1**	MAXIM B Update. “0” = not updated; “1” = updated
0	**1**	MAXIM A Update. “0” = not updated; “1” = updated

4.53 Update RSSI Register 0x32

This register is used to update the detected RSSI values.

RSSI Update Register 0x32																
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Reconfigurable bits:

Bit	Default	Description
1	**0**	“0” = not updated, “1” = update RSSI / Power Detect of Channel B
0	**0**	“0” = not updated, “1” = update RSSI / Power Detect of Channel A

4.54 RSSI Register A 0x33

This read only register retrieves the RSSI value from channel A.

Channel A RSSI Register 0x33															
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	A[11:0]											

4.55 RSSI Register B 0x34

This read only register retrieves the RSSI value from channel B.

Channel B RSSI Register 0x34															
Byte 1-0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	B[11:0]											