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Unit / Module Number:	SMT922 RS422 Mezzanine Card
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Original Author:	Sebastien Maury

Product Specification for SMT922 RS422 Mezzanine Card

Sundance Multiprocessor Technology Ltd, Chiltern House, Waterside, Chesham, Bucks. HP5 1PS.

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Revision History

Issue	Changes Made	Date	Initials
1.0	Initial version	07/05/07	SM
1.1	Updated with RS422, 12 LVTTL, 2xSHB	02/11/07	JV

Table of Contents

1 Introduction

This document is the specification document for the design of the PCB for a mezzanine daughter card to be plugged on an SLB.

This mezzanine card allows interfacing the module with an RS-422 interface. The initial requirement is support of the CEDIP camera used.

2 Related Documents

2.1 Referenced Documents

Sundance Local Bus (SLB) specification:

http://www.sundance.com/docs/SLB%20-%20Sundance%20Local%20Bus%20Specification.pdf

2.2 Applicable Documents

None

3 Acronyms, Abbreviations and Definitions

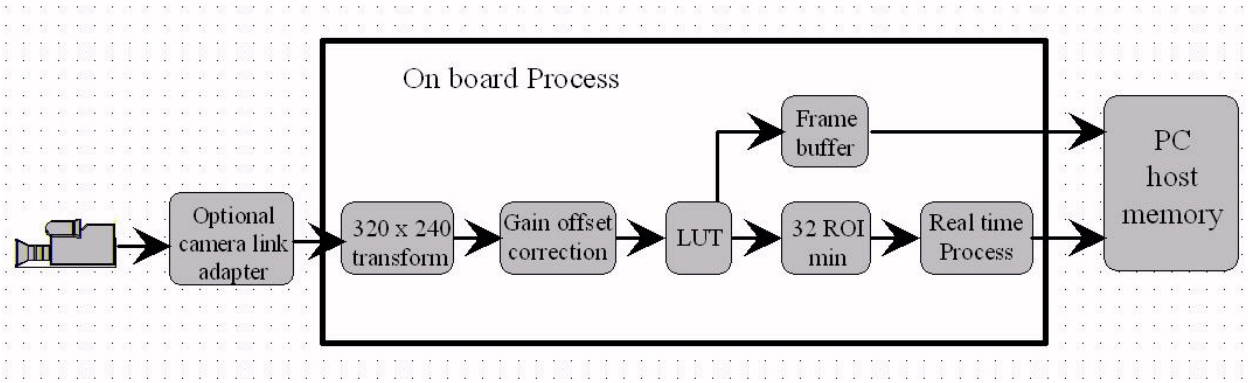
3.1 Acronyms and Abbreviations

SLB : Sundance Local Bus

3.2 Definitions

4 Functional Description

4.1 Block Diagram



4.2 Module Description

The aim of this daughter module is to route digital signal from a 16-bit CEDIP camera to the FPGA supporting module via the SLB interface. On-board processing is not the object of this design specification document.

4.3 Interface Description

There are 20 signals to route:

- 16-bit data bus (parallel bus),
- 1 pixel clock (PIXCLKI),
- 1 horizontal synchronisation (HSYNC, SYLI),
- 1 vertical synchronisation (VSYNC, SYTI),
- 1 trigger (TRIGI)

They all are differential signals according to the RS-422 standard.

TRIGI: this signal starts the signal processing, and it is provided by the chronology of all the acquisitions of Tore Supra.

PIXCLKI: this signal is a continuous 7.5MHz clock signal

DATA: the data signals are synchronous to the rising edges of the PIXCLKI. The data are valid after a propagation time less than 25ns.

VSYNC & HSYNC: the rising and falling edges of VSYNC and HSYNC are synchronous to the rising edge of PIXCLKI. They appear after a propagation time less than 25ns.

The delay between two rising edges of VSYNC is equals to 20ms.

The first rising edge of HSYNC is synchronous to the falling edge of VSYNC.

HSYNC is latched 'HIGH' ('1') for 16 clock cycles.

4.3.1 Mechanical Interface

The signals of the CEDIP camera are transported via a fibre link. The output connector is a DB50 female type with 3 raws of pins. (DD50)

The Sundance daughter card must present the following pinout for the DD50 male type connector on the front panel.

Signal name	DB50 connector Female
+DI0	1
-DI0	34
+DI1	18
-DI1	2
+DI2	35
-DI2	19
+DI3	3
-DI3	36
+DI4	20
-DI4	4
+DI5	37
-DI5	21
+DI6	5
-DI6	38
+DI7	22
-DI7	6
+DI8	39
-DI8	23
+DI9	7
-DI9	40
+DI10	24
-DI10	8
+DI11	41
-DI11	25
+DI12	9
-DI12	42
+DI13	26
-DI13	10
+DI14	43
-DI14	27
+DI15	11
-DI15	44
+SYLI	28
-SYLI	12
+SYTI	45
-FSYTI	29
GND	13
GND	46
+PIXCLKI	30
-PIXCLKI	14
+ TRIGI	49
- TRIGI	33
GND	50

The on-board connector will be a latching connector N10250-5242VC. Pinout TBD to best match with DD50 on front panel.

Twelve LVTTL signals are provided via a latching 0.1” pitch DIL pin header. They are used to generate some alarm signals to the outside.

Those pins may be connected to a LED to see the level of the pins.

Four extra LEDs are routed to the FPGA for display.

Two SHB connectors provide backward compatibility.

There is also a JTAG header to access the FPGA directly routed through the SLB interface of the module. This depends on the supporting module and JTAG cable might have to be connected directly on the supporting module (This is the case for the SMT351T).

4.3.2 Electrical Interface

The RS422 signals are made from RS485 transceivers with the direction set by a jumper for testing purpose. The termination resistors are 150 Ohms.

The twelve LVTTL signals are routed through quick switches to protect the FPGA.

5 SLB Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	SHBB_D0	2	SHBB_D1	3	SHBB_D2	4	SHBB_D3
5	SHBB_D4	6	SHBB_D5	7	SHBB_D6	8	SHBB_D7
9	SHBB_D8	10	SHBB_D9	11	SHBB_D10	12	SHBB_D11
13	SHBB_D12	14	SHBB_D13	15	SHBB_D14	16	SHBB_D15
17	SHBB_D16	18	SHBB_D17	19	SHBB_D18	20	SHBB_D19
21	SHBB_D20	22	SHBB_D21	23	SHBB_D22	24	SHBB_D23
25	SHBB_D24	26	SHBB_D25	27	SHBB_D26	28	SHBB_D27
29	SHBB_D28	30	SHBB_D29	31	SHBB_D30	32	SHBB_D31
33	SHBB_CLK	34	SHBB_NWEN	35	SHBB_REQ	36	SHBB_ACQ
37	LED_0	38	LED _1	39	LED _2	40	LED _3
41	D0	42	D1	43	D2	44	D3
45	D4	46	D5	47	D6	48	D7
49	D8	50	D9	51	D10	52	D11
53	D12	54	D13	55	D14	56	D15
57	PIXCLKI	58	TRIGI	59	HSYNC	60	VSYNC
61	TTL_0	62	TTL_1	63	TTL_2	64	TTL_3
65	TTL_4	66	TTL_5	67	TTL_6	68	TTL_7
69	TTL_8	70		71		72	
73		74		75		76	
77		78		79		80	
81	SHBA_D0	82	SHBA_D1	83	SHBA_D2	84	SHBA_D3
85	SHBA_D4	86	SHBA_D5	87	SHBA_D6	88	SHBA_D7
89	SHBA_D8	90	SHBA_D9	91	SHBA_D10	92	SHBA_D11
93	SHBA_D12	94	SHBA_D13	95	SHBA_D14	96	SHBA_D15
97	SHBA_D16	98	SHBA_D17	99	SHBA_D18	100	SHBA_D19
101	SHBA_D20	102	SHBA_D21	102	SHBA_D22	104	SHBA_D23
105	SHBA_D24	106	SHBA_D25	107	SHBA_D26	108	SHBA_D27
109	SHBA_D28	110	SHBA_D29	111	SHBA_D30	112	SHBA_D31
113	SHBA_CLK	114	SHBA_NWEN	115	SHBA_REQ	116	SHBA_ACQ
117	TTL_9	118	TTL_10	119	TTL_11	120	TTL_12

6 Verification Procedures

7 Review Procedures

8 Validation Procedures

9 Timing Diagrams

10 Circuit Description / Diagrams

11 Footprint

11.1 Top View

11.2 Bottom View

12 Pinout

13 Support Packages

14 Physical Properties

Dimensions		
Weight		
Supply Voltages		
Supply Current	+12V	
	+5V	
	+3.3V	
	-5V	
	-12V	
MTBF		

15 Safety

This module presents no hazard to the user when in normal use.

16 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.