Unit / Module Name:	DVI Transceiver Module
Unit / Module Number:	SMT939
Used On:	SMT339,SMT351T
Document Issue:	1.0
Date:	6th September 2007

CONFIDENTIAL

Sundance Multiprocessor Technology Ltd, Chiltern House, Waterside, Chesham, Bucks. HP5 1PS.

Revision History

Issue	Changes Made	Date	Initials
0.9	Initial Draft	6/07/07	AJP
0.95	Detailed Draft	26/07/07	AJP
0.96	Final Draft	31/07/07	AJP
1.0	Release Version 1	06/09/07	AJP

Table of Contents

Table of Figures

1 Introduction

The SMT939 is a DVI transceiver module SLB expansion card. It is capable of receiving a Single DVI channel running with a maximum clock frequency of 165MHz. The decoded DVI data stream is organised as a 24bit RGB packet with separate syncs and clock. This is fed through level translation buffers to allow the data to be connected to the 2.5V SLB interface header. An onboard EEPROM allows an EDID table to be programmed so that driving hardware can interrogate the DVI input interface.

The SMT939 also has an DVI encoder on the module which supports a single DVI output interface which can run at upto 165Mhz.

The module uses the Sundance Local Bus (SLB) in single ended mode in order to interface to DSP modules such as the SMT339.

1.1 Related Documents

Sundance Local Bus (SLB) Specifications – Sundance.

TIM specifications.

SMT339 – Advanced Video Processing DSP Module.

2 Functional Description

The basic block diagram of the SMT939 is shown in Figure 1.

2.1 DVI Receiver

The DVI receiver is based on the Silicon Image SIL1161 SIL1161 DVI Receiver this allows video formats from 25 to 165 MHz (VGA to UXGA) to be received. The 24-bit data and the control signals (HSYNC,VSYNC,CLK and DE) are fed via a LVTTL to 2.5V bus level converter before being passed to the SLB expansion header.

2.2 DVI Transmitter

The DVI receiver is based on the Texas Instruments TFP410 TI TFP410 DVI Transmitter. Data from the SLB header is passed through the voltage level translator before beign fed to the input pins of the TFP410. It supports 24-bit data ad syncs from 25-165MHz bandwidth.

2.3 EDID Prom

An EDID prom is connected to the relevant pin of the DVI receiver header so that information can be stored in the EDID table for interrogation by the host. To program the EDID the user will require software on a HOST PC that will connect via the DVI cable. A write protection jumper insures the EDID table cannot be corrupted during normal operation.

2.4 SLB Connector

The **S**undance **L**ocal **B**us (*SLB*) allows data from each video decoder to be streamed, using embedded or separate sync formats, to the main processing module. All signals using LVPECL at 2.5V. The I2C interface lines on the SLB connector allows the host processor to configure each DVI encoder/decoder independently over the I2C bus. The use of the I2C bus is optional 939's maybe shipped with default configurations use boot mode resistors.

2.4.1 SLB Power Supplies

When using the SLB interface a separate SLB power header (BKT) is used to supply the Daughterboard. Details of this connector pinout can be found in the SLB Reference Guide.

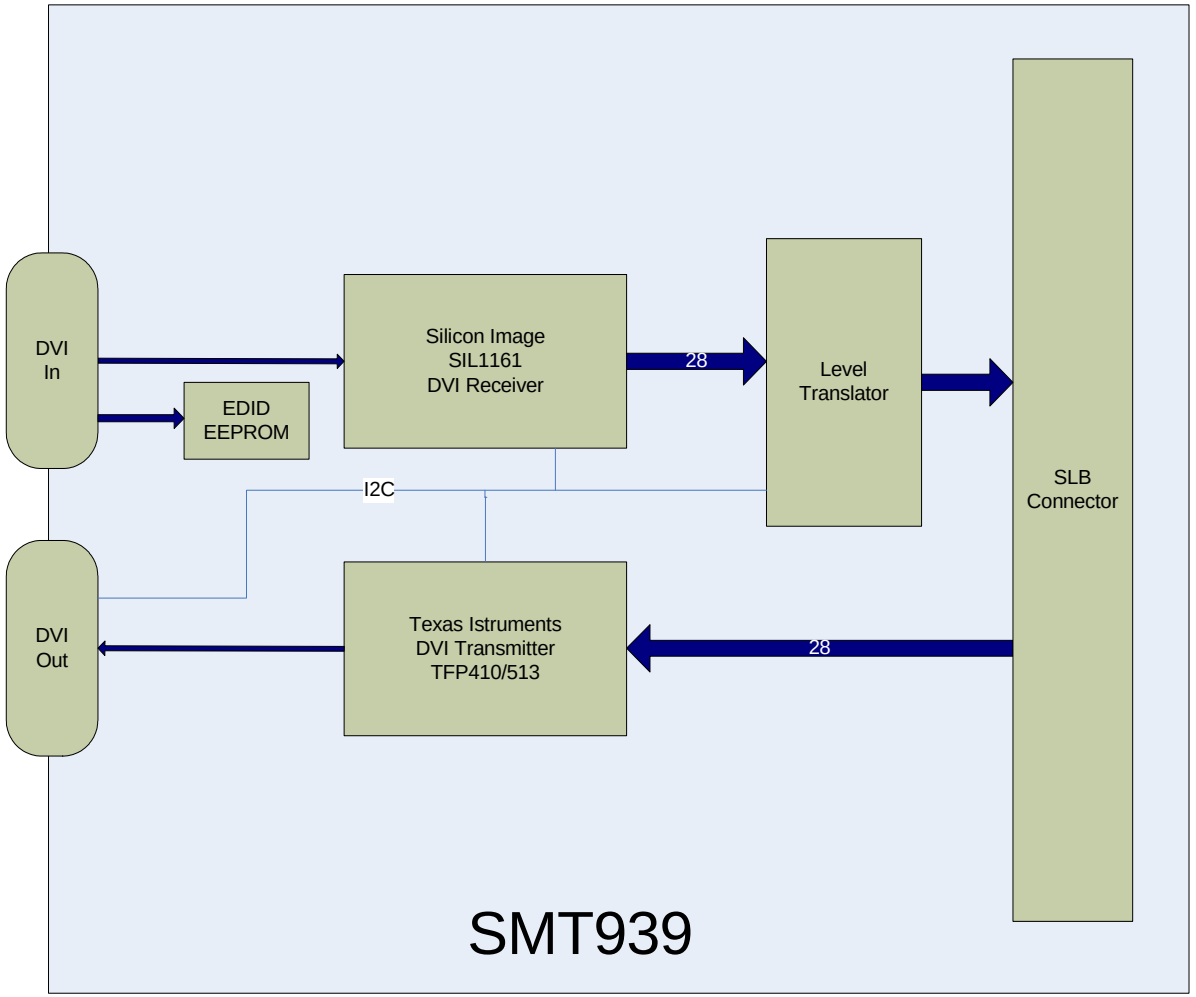


Figure 1 : SMT939 Block Diagram

3 Mechanical Interface

The host board provides power, Ground, data and control lines between the module.

4 Electrical Interface

4.1 SLB Interface Connector(J1)

SMT939 Connector Part No. Samtec QSH-060-01-F-D-DP-A

Mating connector Samtec QTH-060-01-D-DP-A

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	DVI_OUT_D12	2	DVI_OUT_D11	3	DVI_OUT_D13	4	DVI_OUT_D10
5	DVI_OUT_D14	6	DVI_OUT_D9	7	DVI_OUT_D15	8	DVI_OUT_D8
9	DVI_OUT_D16	10	DVI_OUT_D7	11	DVI_OUT_D17	12	DVI_OUT_D6
13	DVI_OUT_D18	14	DVI_OUT_CLK	15	DVI_OUT_D19	16	DVI_OUT_D5
17	DVI_OUT_D20	18	DVI_OUT_D4	19	DVI_OUT_D21	20	DVI_OUT_D3
21	DVI_OUT_D22	22	DVI_OUT_D2	23	DVI_OUT_D23	24	DVI_OUT_D1
25	DVI_OUT_HS	26	DVI_OUT_D0	27	DVI_OUT_VS	28	DVI_OUT_DE
29	DVI_OUT_MSEN	30		31		32	
33		34		35		36	
37		38		39		40	
41	IIC_CLK	42	IIC_DATA	45		44	
45		46		47		48	
49		50		51		52	
53		54		55		56	
57		58		59		60	
61		62		63		64	
65		66		67		68	
69		70		71		72	
73		74		75		76	
77		78		79		80	
81	DVI_IN_D0	82	DVI_IN_D11	83	DVI_IN_D1	84	DVI_IN_D12
85	DVI_IN_D2	86	DVI_IN_D13	87	DVI_IN_D3	88	DVI_IN_D14
89	DVI_IN_D4	90	DVI_IN_D15	91	DVI_IN_D5	92	DVI_IN_D16
93	DVI_IN_D6	94	DVI_IN_D17	95	DVI_IN_D7	96	DVI_IN_D18
97	DVI_IN_D8	98	DVI_IN_D19	99	DVI_IN_D9	100	DVI_IN_D20
101	DVI_IN_D10	102	DVI_IN_D21	103	DVI_IN_STDET	104	DVI_IN_D22
105	DVI_IN_DE	106	DVI_IN_D23	107	DVI_IN_VS	108	DVI_IN_HS
109		110		111		112	
113	DVI_IN_CLK	114		115	DVI_IN_CLK	116	
117		118		119		120	

4.2 SLB Power Connector

SMT939 Connector Part No. BKS-133-03-F-V-A

Mating PCB connector Samtec BKS-133-01-F-V-A

Pin #	Description	Pin #	Description
1	3.3V	2	GND
3	3.3V	4	GND
5	3.3V	6	GND
7	3.3V	8	GND
9	5V	10	GND
11	5V	12	GND
13	5V	14	GND
15	5V	16	GND
17	+12V *	18	GND
19	+12V *	20	GND
21	-12V *	22	GND
23	-12V *	24	GND
25	GND	26	DSP JTAG0 *
27	DSP JTAG1 *	28	DSP JTAG2 *
29	DSP JTAG3 *	30	DSP JTAG4 *
31	DSP JTAG5 *	32	DSP JTAG6 *
33	GND		

*** - Not used on SMT939**

4.3 DVI-I Connector

SMT939 Part N^{o}. : JAE DV2-R029N11E

Mating Part N^{o}. : Any DVI-D or DVI-I Cable (Dual link)

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	TMDS Data2-	9	TMDS Data1-	17	TMDS Data0-
2	TMDS Data2+	10	TMDS Data1+	18	TMDSData0+
3	TMDS Data2/4 Shield	11	TMDS Data1/3 Shield	19	TMDS Data0/5 Shield
4	TMDS Data4-	12	TMDS Data3-	20	TMDS Data5-
5	TMDS Data4+	13	TMDS Data3+	21	TMDS Data5+
6	DDC Clock [SCL]	14	+5 V Power	22	TMDS Clock Shield
7	DDC Data [SDA]	15	Ground (for +5 V)	23	TMDS Clock +
8		16	Hot Plug Detect	24	TMDS Clock -
C1	--	--	--	--	--
C2	--	--	--	--	--
C3	--	--	--	--	--
C4	--	--	--	--	--
C5	--	--	--	--	--

5 Verification Procedures

The verification procedure for the module is as follows.

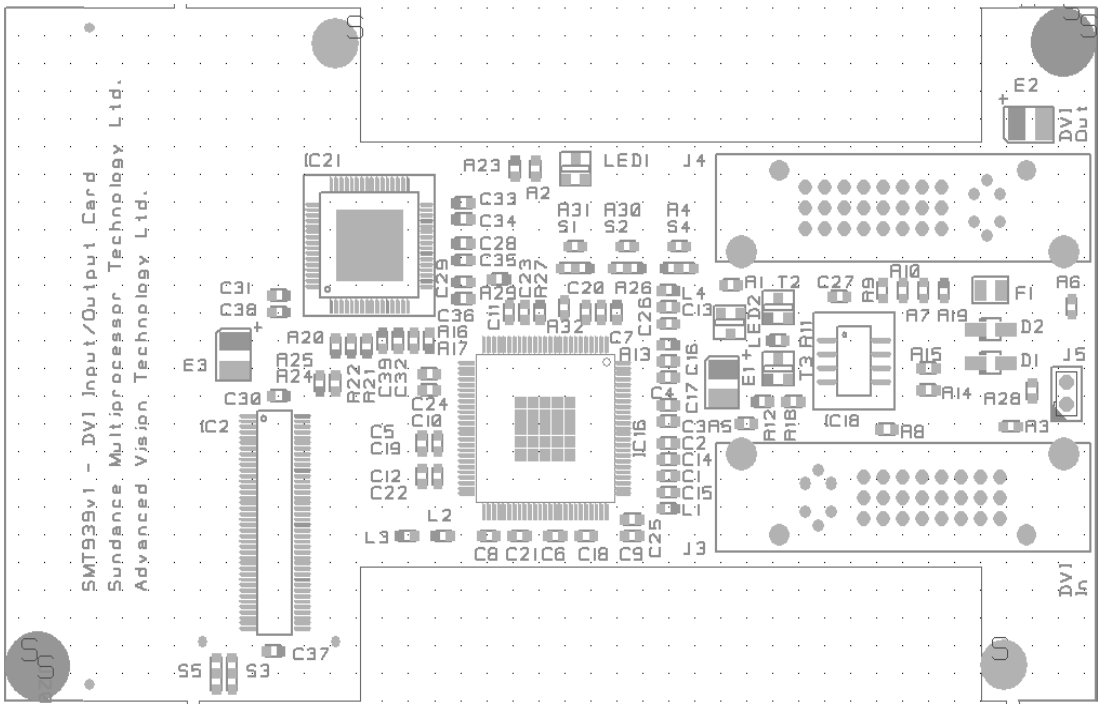
5.1 DVI Encoder/Decoder

Data is looped through on a SMT339 fpga. Video test patterns at the input of the SMT939 are viewed on a DVI monitor at a number of resolutions in order to confirm colour and pixel clarity at the output interface.

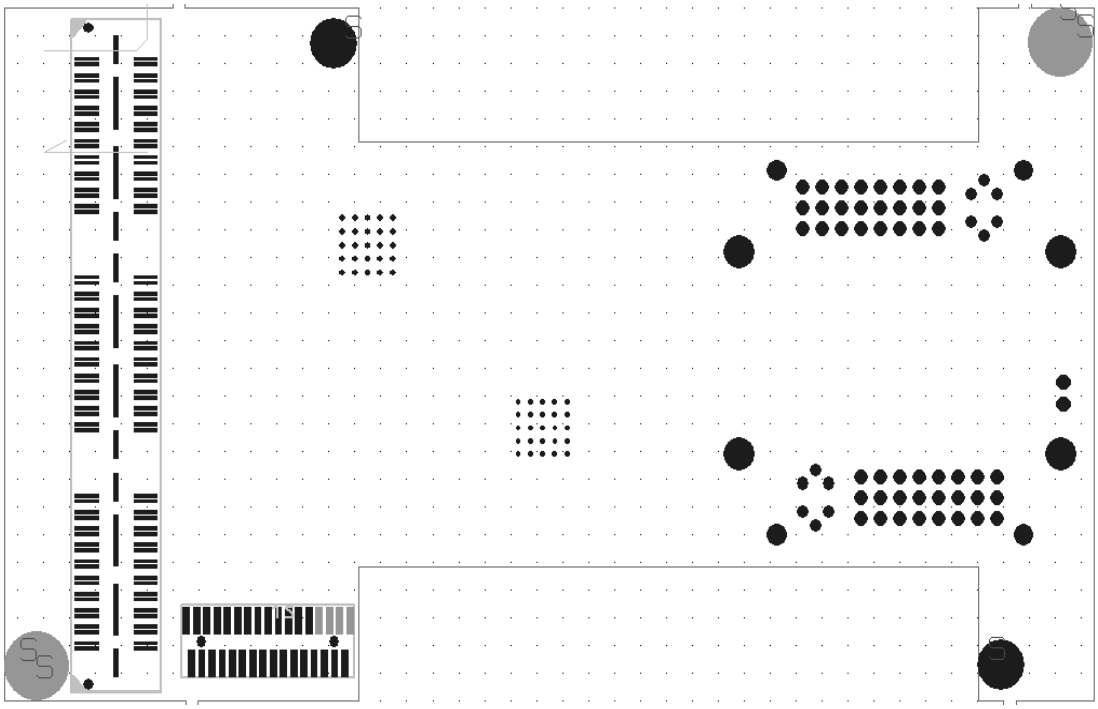
The EDID prom is programmed with a default EDID table for the host system to interrogate.

6 PCB Layout Details

6.1 Top Side



6.2 Bottom Side



7 Safety

This module presents no hazard to the user.

8 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.