Unit / Module Description:	Dual ADC (14bits/250MSPS) and Dual DAC (16bits/800MSPS) SLB Module
Unit / Module Number:	SMT943
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Product Specification for SMT943

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Certificate Number FM 55022

Revision History

Issue	Changes Made	Date	Initials
1	Initial Document created	26/05/08	PhSR
2	Part numbers corrected	20/04/09	PhSR

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1 Introduction

The *SMT943* is a single width expansion TIM that plugs onto an SLB base module, the SMT351T (Virtex-5 LXT or SXT FPGA) as an example and incorporates 2 Analog-to-Digital Converters (ADS62P49) and a Texas Instrument dual-channel Digital-to-Analog Converter (DAC5688). The *SMT943* implements a comprehensive clock circuitry based on a chip (CDCE72010) from Texas instrument that allows synchronisation among the converters and the use of an external reference clock. It provides a complete conversion solution and stands as a platform that can be part of a transmit/receive base station. The SMT943 has an on-board VCXO of frequency 245.76MHz.

ADCs are 14-bit and can sample at up to 250 MHz. The DAC has a resolution of 16 bits and is able to update outputs at up to 800MHz. All converters are 1.8/3.3-Volt.

The Xilinx FPGA (Virtex-5 LXT or SXT series in the case of the SMT351T) on the base module is responsible for handling data going/coming to/from one of the following destination/source: converters, Comports, **R**ocket **S**erial **L**ink (RSL). These interfaces are compatible with a wide range of Sundance's modules.

The memory (DDR2) on the base module can store incoming and/or outgoing samples.

Converter configuration, sampling and transferring modes are set via internal control registers stored inside the FPGA and accessible via Comport.

The SMT943 module is well-suited for multi-carrier, wide bandwidth communication applications.

2 Related Documents

2.1 Referenced Documents

ADC datasheet. Texas Instrument ADS62P49.

DAC datasheet: Texas Instrument DAC5686.

Clock datasheet: Texas Instrument CDCE72010.

2.2 Applicable Documents

3 Acronyms, Abbreviations and Definitions

3.1 Acronyms and Abbreviations

3.2 Definitions

4 Functional Description

4.1 Block Diagram

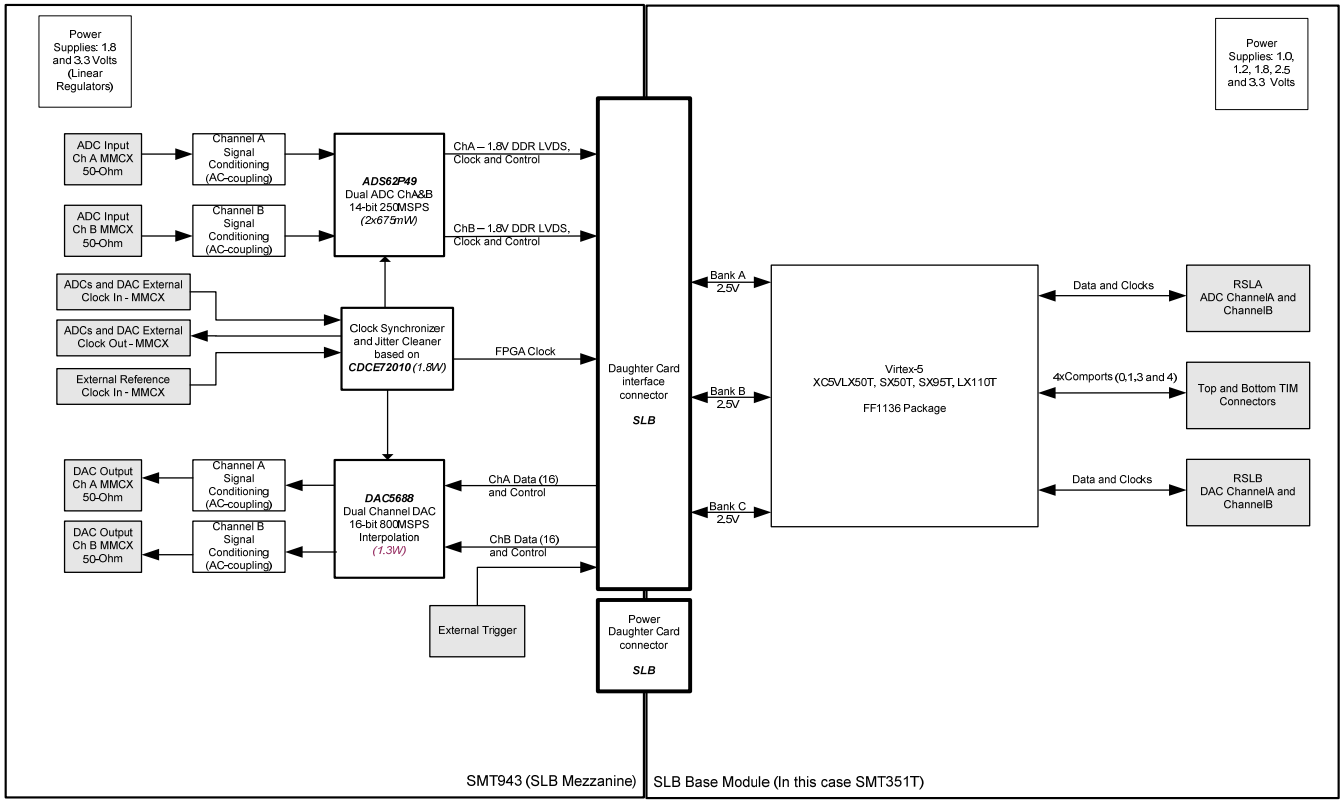

Figure 1 - Block diagram.

4.2 Module Description

The dual channel ADC (ADS62P49) has a resolution of 14 bits and can sample at up to 250 MHz. The chip incorporates a programmable fine gain of up to 6dBs for SNR/SFDR trade-off, a DC offset correction and an internal voltage reference. The ADC has got internal registers to implement the above functionalities and are accessible via a serial interface controlled by the FPGA on the SLB base module.

The dual channel DAC (DAC5688 – Texas Instrument) has integrated 2x-8x interpolation filters, a fine frequency mixer with a 32-bit complex numerically controlled oscillator, an on-board clock multiplier, an IQ compensation and an internal voltage reference.

4.3 Interface Description

4.3.1 Mechanical Interface

4.3.2 Electrical Interface

5 Verification Procedures

6 Review Procedures

7 Validation Procedures

8 Timing Diagrams

9 Circuit Description / Diagrams

10 Footprint

10.1 Top View

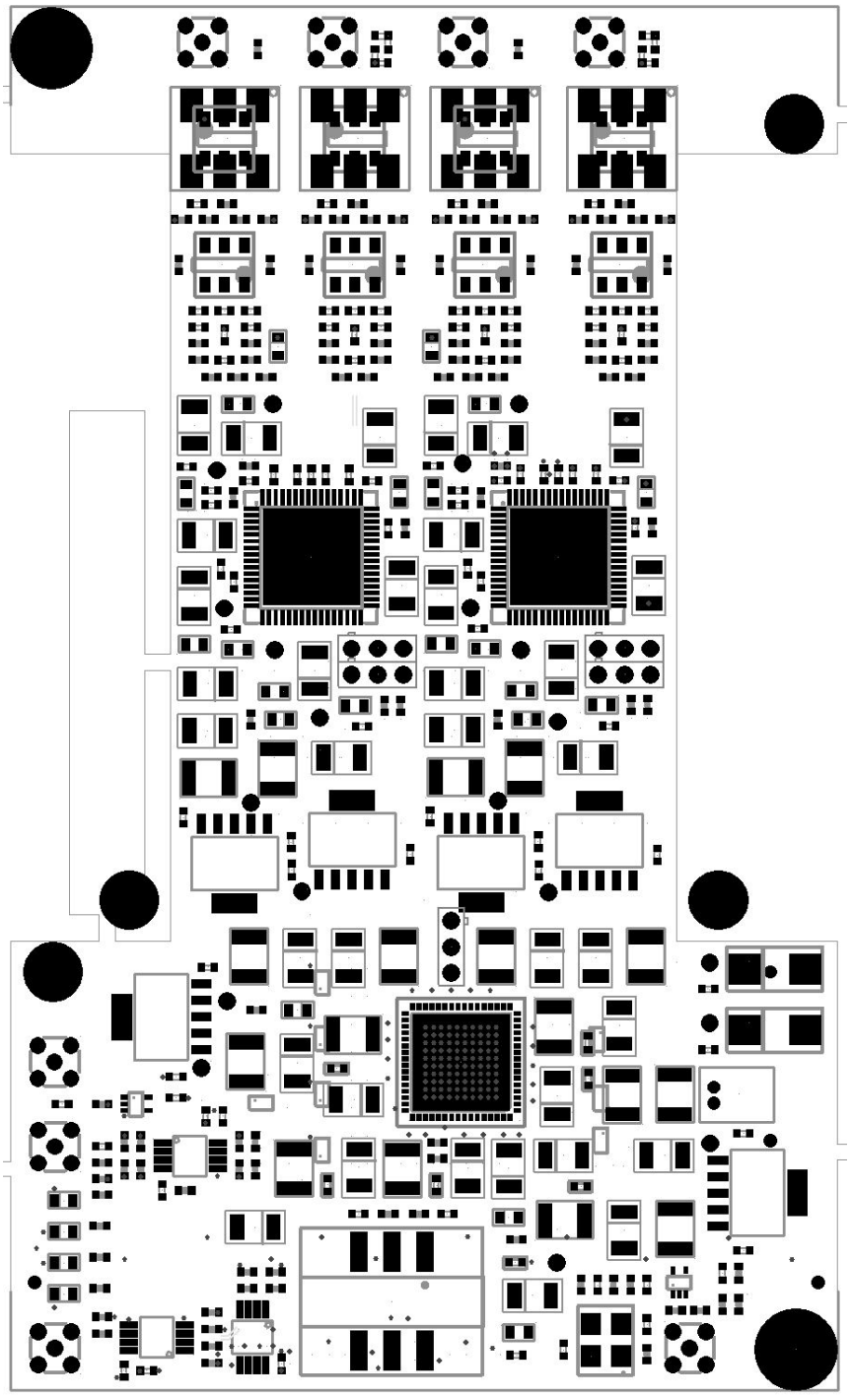

Figure 2 - Layout - Top Layer.

10.2 Bottom View

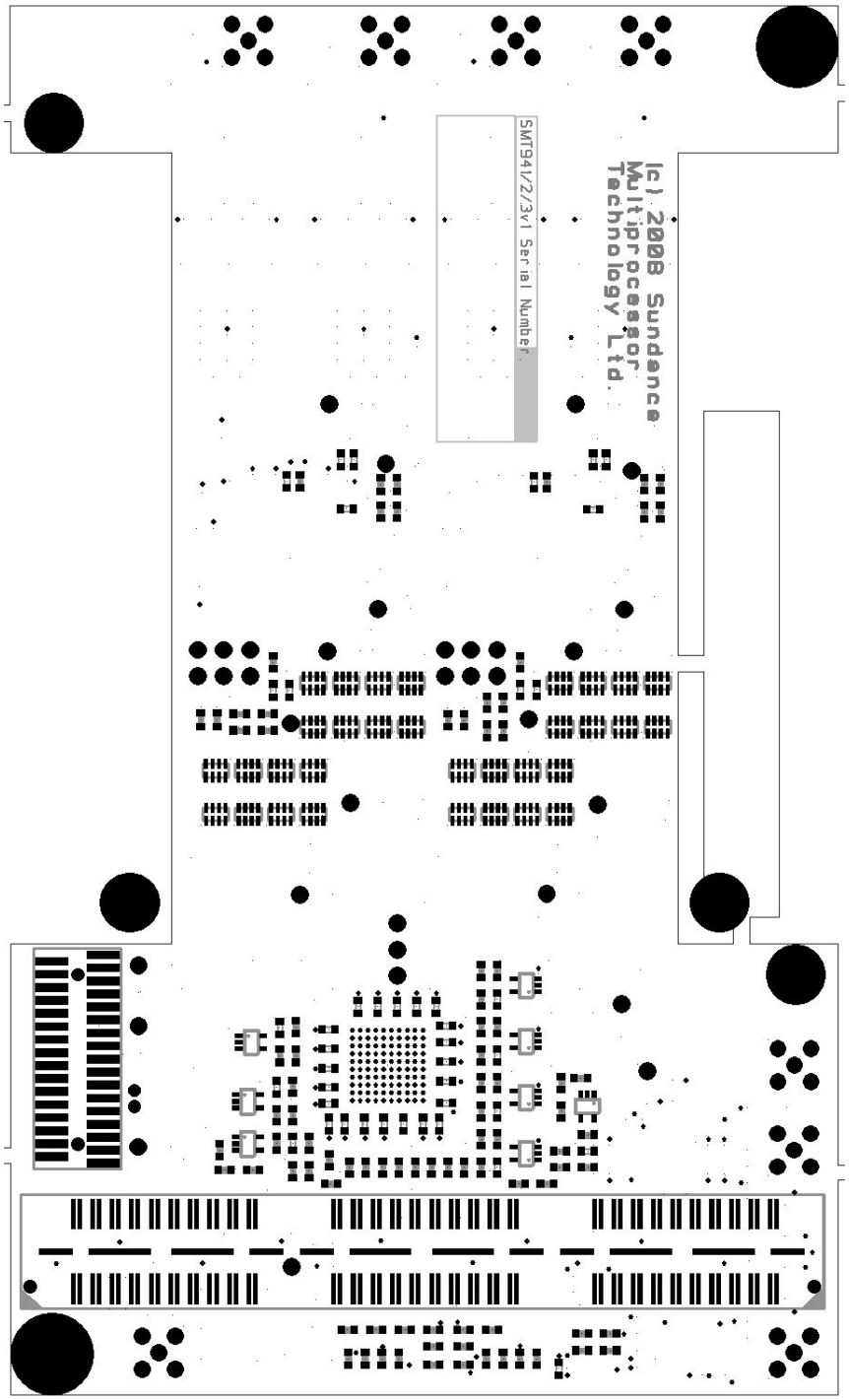

Figure 3 - Layout - Bottom Layer.

11 Pinout

12 Support Packages

13 Physical Properties

Dimensions		
Weight		
Supply Voltages		
Supply Current	+12V	
	+5V	
	+3.3V	
	-5V	
	-12V	
MTBF		

14 Safety

This module presents no hazard to the user when in normal use.

15 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.