Unit / Module Description:	Dual Ethernet & SDRAM SLB Mezzanine
Unit / Module Number:	SMT945
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Product Specification for SMT945

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Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	6/09/07	GKP
1.1	Added SDRAM.	11/09/07	GKP
1.2	RS232 and MicroSD flash added Ethernet rotated. Power added on TTL connector	25/10/07	JV
1.3	Change for bi-directional LVTTL IOs support. Clarification on MicroSD use	02/11/07	JV
1.4	Updated footprint to actual photographs. Added LVTTL I/O direction control description.	25/7/08	GKP
1.5	Added SLB signal description section.	18/9/07	GKP
1.6	Added PHY addresses.	2/10/08	GKP

Table of Contents

1 Introduction / Description

The SMT945 is a single width expansion SLB mezzanine that plugs onto a base TIM that incorporates the SLB (eg SMT368).

It uses 2 Marvell Alaska gigabit PHYs (88E1116) to provide 2 channels of 10/100/1000 Ethernet.
The PHYs interface via the SLB connector directly to the host TIM's FPGA. MAC interfaces and control must be provided within this FPGA.
The PHYs' outputs are presented on RJ45 horizontally mounted connectors.
128Mbytes of 100MHz 32-bit SDRAM is also provided.
All power supplies required by the SLB mezzanine are derived from the 3.3V on the SLB power connector.
Eight LVTTL signals are provided via a latching 0.1" pitch DIL pin header. These are routed through quick switches.
RS232 interface for PowerPC debugging.
Flash MicroSD for PowerPC OS.

The main features of the *SMT945* are listed below:

- Dual Marvell 88E1116 Ethernet PHYs.
- 128Mbytes SDRAM.
- SLB connector to link *SMT945* to base TIM.
- LVTTL signals.
- MicroSD flash.
- RS232 for debug.

2 Related Documents

Xilinx Virtex5 datasheets:
http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?category=Data+Sheets/FPGA+Device+Families/Virtex-5

Sundance Local Bus (SLB) specification:
http://www.sundance.com/docs/SLB%20-%20Sundance%20Local%20Bus%20Specification.pdf

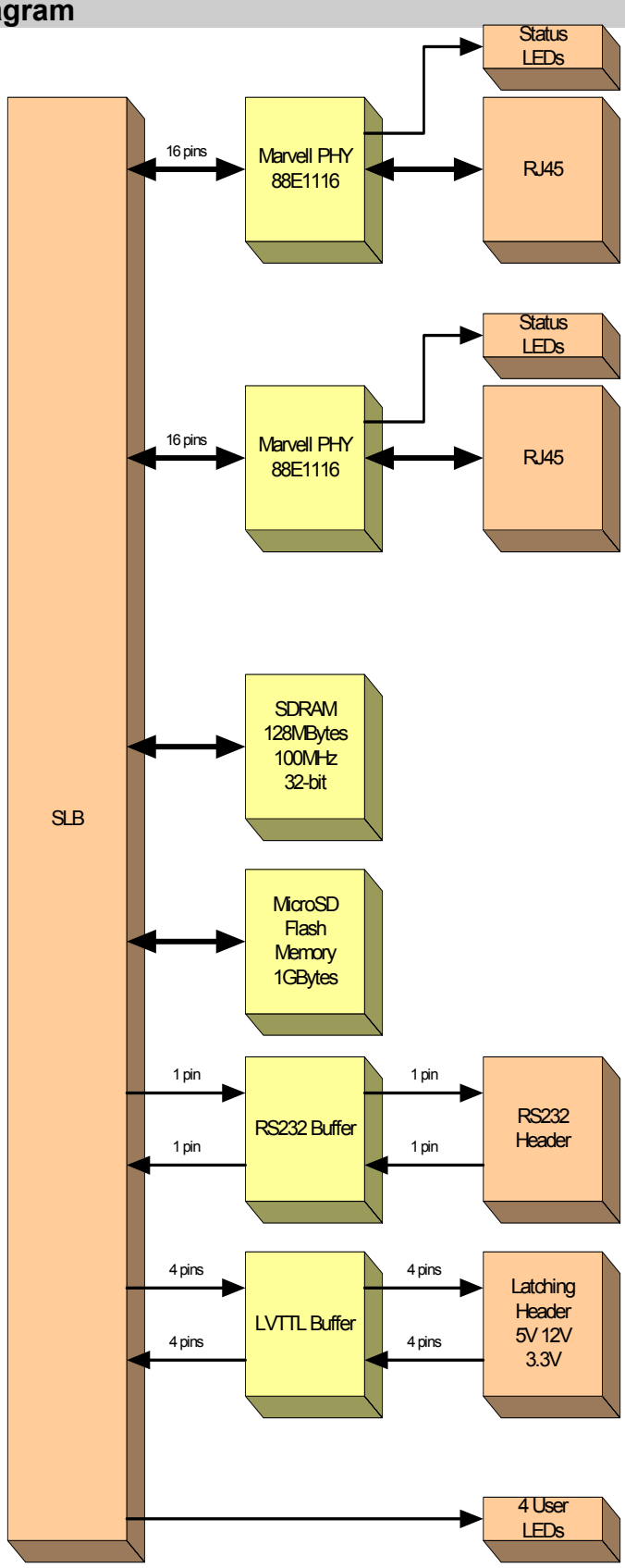
3 Acronyms, Abbreviations and Definitions

A list of acronyms etc: http://www.sundance.com/web/files/static.asp?pagename=acc

4 Functional Description

The major elements of the SMT945 are shown in the block diagram below.

4.1 Block Diagram



4.2 Module Description

4.2.1 FPGA

The SMT945 typically interfaces to an FPGA on a TIM module. This FPGA is responsible for all communication to and from the PHYs, the interface to the flash memory, and the SDRAM interface and controller.

4.2.2 PHY

Each of the Marvell 88E1116 PHYs connect directly to the FPGA using 16 signals.
The PHY connects directly to an RJ45, horizontally mounted, connector. This connector can be omitted and a pin-header fitted in its place. This will allow a wire to connect to a panel mounted RJ45. The connectors are placed so that once fitted on an SMT111 (single TIM-site stand-alone carrier) they can be available on the side of the box.
PHYA, labelled P1, is at address b0011, and PHYB, labelled P2, is at address b1100.

4.2.3 Flash Memory

A flash memory connector for a MicroSD card is fitted. Interface to this is 6 bits: CLK, CMD, DAT0-3. It can also work in a simpler SPI mode (4 bits only).
This will store the OS for the PowerPC. Size depends on the card fitted. 1Gbyte seems a relatively standard size. The flash will be used to store raw data initially but a file system could be used.
A unified format will be needed at a later stage so that the card allows the initial loading and to use the SD file system support provided by the OS.

4.2.4 RS232

A 2 bits RS232 interface is provided for debugging with MAX3227 line driver/receiver. This is available on a 4-pin DIL connector (2 GND associated).
This will provide RS232 interface for stdio used to debug the PowerPC.

4.2.5 SDRAM

Four devices provide 128Mbytes of memory. This is connected to the SLB as a 32-bit wide bus. The target speed for this memory is 100MHz.
Each physical device is 16 bits wide, so two devices are used to create a 32-bit data bus.
The four devices are grouped in two banks of two devices each, thus there are 2 SDRAM chip select signals.

4.2.6 LVTTL I/O

Eight I/Os are provided. They are routed through buffers to protect the FPGA. These are available on a 16-way latched DIL connector.

The position of each signal is indicated on the silkscreen of the module.

Power is provided on the connector. 12 V, -12V, 5V, and 3.3V are provided as well on vias.

TTL_0	TTL_4
TTL_1	TTL_5
TTL_2	TTL_6
TTL_3	TTL_7
+12V	GND
-12V	GND
+5V	GND
+3.3V	GND

The direction of these signals is determined by the setting of jumper JP4. Inserting a jumper between pins 1&2 will cause the signals TTL_0 to TTL_3 to become inputs. Similarly, a jumper on pins 3&4 will cause the signals TTL_4 to TTL_7 to become inputs. No jumper fitted returns the signals to their default output state.
These jumper settings are shown on the module's silkscreen.

4.2.7 LEDs

Four LEDs are available and connected to the TIMs FPGA via the SLB signal pins.

5 SLB Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	D0	2	D1	3	D2	4	D3
5	D4	6	D5	7	D6	8	D7
9	D8	10	D9	11	D10	12	D11
13	D12	14	D13	15	D14	16	D15
17	D16	18	D17	19	D18	20	D19
21	D20	22	D21	23	D22	24	D23
25	D24	26	D25	27	D26	28	D27
29	D28	30	D29	31	D30	32	D31
33	A0	34	A1	35	A2	36	A3
37	A4	38	A5	39	A6	40	A7
41	A8	42	A9	43	A10	44	A11
45	A12	46	BA0	47	BA1	48	RS_TXD
49	LED0	50	LED1	51	LED2	52	RS_RXD
53	CLK	54	CKE	55	SCS0	56	RAS
57	CAS	58	SWE	59	DQM0	60	DQM1
61	DQM2	62	DQM3	63	SCS1	64	F_CLK
65	F_CMD	66	F_DAT0	67	F_DAT1	68	F_DAT2
69	F_DAT3	70		71		72	
73		74		75		76	
77		78		79		80	
81	PB_RXCTRL	82	TTL_0	83	LED3	84	TTL _4
85	PB_RXCK	86	TTL _1	87	P_RST	88	TTL _5
89	PB_RX1	90	TTL _2	91	PB_RX3	92	TTL _6
93	PB_RX0	94	TTL _3	95	PB_RX2	96	TTL _7
97	PB_TXCK	98	PB_TXCTRL	99	PB_MDC	100	PB_MDIO
101	PB_TX0	102	PB_TX1	102	PB_TX2	104	PB_TX3
105	PA_RXCK	106	PA_RXCTRL	107	PA_COMA	108	PB_COMA
109	PA_RX0	110	PA_RX1	111	PA_RX2	112	PA_RX3
113	PA_TXCK	114	PA_TXCTRL	115	PA_MDC	116	PA_MDIO
117	PA_TX0	118	PA_TX1	119	PA_TX2	120	PA_TX3

6 SLB signal Description

SIGNAL	Description
D[0..31]	SDRAM 32-bit data bus.
A[0..12]	SDRAM address bus. Connects to pins A[0..12] of all 4 SDRAM devices.
BA[0..1]	SDRAM bank address bits. Connects to pins BA[0..1] of all 4 SDRAM devices.
CLK	SDRAM clock.
CKE	SDRAM clock enable.
SCS0	SDRAM bank 1 chip select.
SCS1	SDRAM bank 2 chip select.
RAS	SDRAM RAS signal. Common to all 4 devices.
CAS	SDRAM CAS signal. Common to all 4 devices.
SWE	SDRAM WE signal. Common to all 4 devices.
DQM[0..3]	SDRAM data mask. One mask signal per byte. Each mask signal is connected to two devices (one in each bank).

RS_TXD	RS232 transmit data.
RS_RXD	RS232 receive data.

F_CLK	MicroSD clock.
F_CMD	MicroSD command.
F_DAT[0..3]	MicroSD data (4 bits).

LED[0..3]	Direct connection to 4 LEDs.

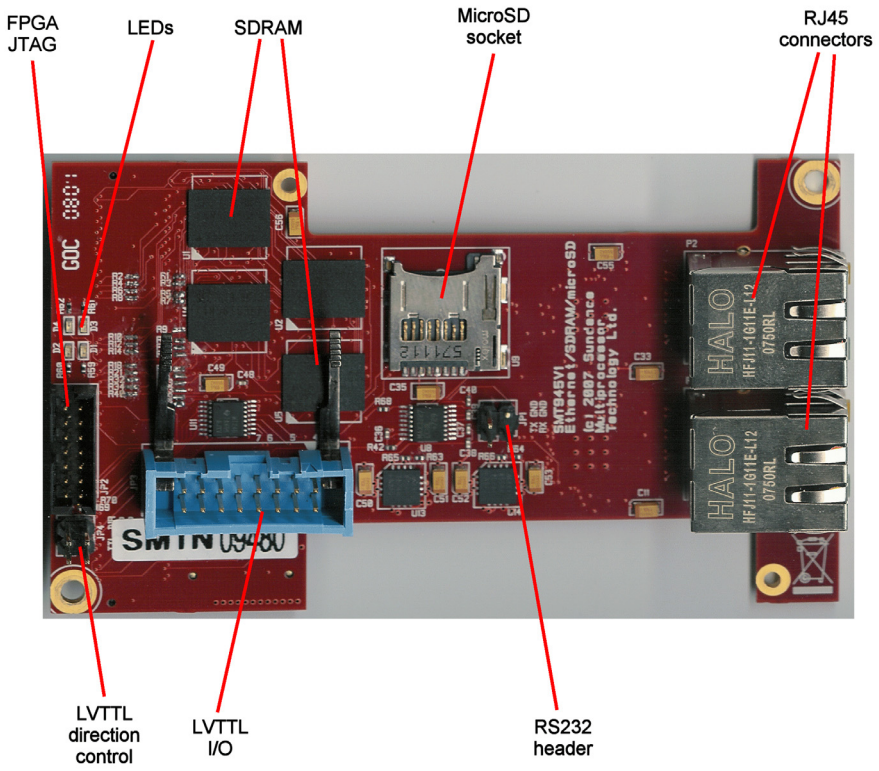
TTL_[0..7]	Inserting a jumper on JP4 pins 1-2 cause TTL[0..3] to become inputs. Removing the jumper will cause them to be outputs. Inserting a jumper on JP4 pins 3-4 cause TTL[4..7] to become inputs. Removing the jumper will cause them to be outputs.

P_RST	PHY reset, active low. Connects to both PHYs.
PA_MDIO	PHY_A MDIO signal.
PA_MDC	PHY_A MDC signal.
PA_TXCK	PHY_A transmit clock.
PA_TX[0..3]	PHY_A transmit data.
PA_RXCK	PHY_A receive clock.
PA_RX[0..3]	PHY_A receive data.
PA_COMA	Power control. Set to ‘1’ for normal operation. ‘0’ for power down.
PA_RXCTRL	PHY_A receive control.
PA_TXCTRL	PHY_A transmit control.

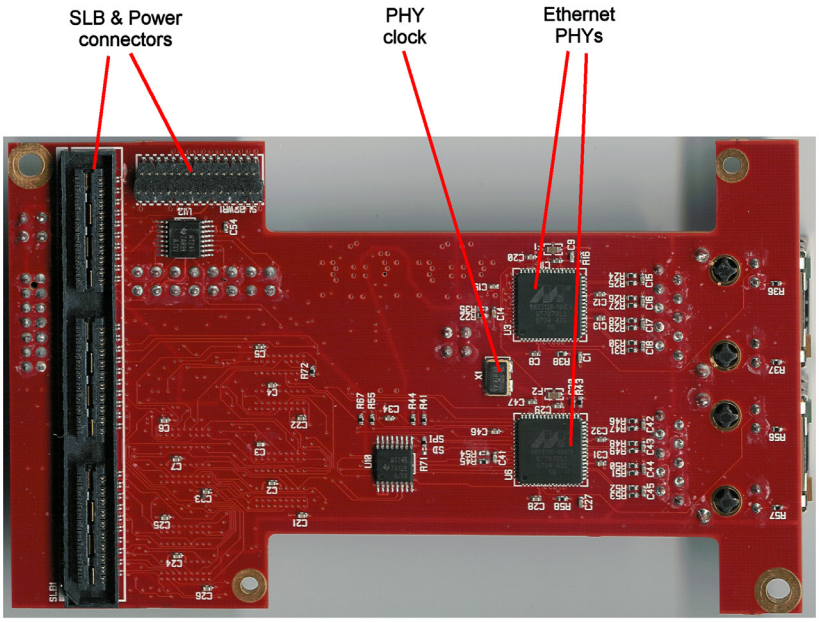
A similar set of signals exist for PHY_B, labelled PB_.
A datasheet for the 88E1116 Ethernet PHY is available under NDA from Marvell.

7 Footprint

7.1 Top View



7.2 Bottom View



8 Support Packages

9 Physical Properties

Dimensions	107mm	64mm

Weight	

Voltage	Current
+12V	TBD
+5V	TBD
+3.3V	TBD
-12V	0

MTBF	

10 Verification, Review & Validation Procedures

To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

11 Safety

This module presents no hazard to the user when in normal use.

12 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.
This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.
Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

13 Ordering Information

Variations of this product are available with RJ45 connectors or pin-headers
Eg. SMT945-rj, or SMT945-ph