HARDWARE SPECIFICATION

FOR

RSL

(Rocket-IO Serial Link)

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1. SCOPE

This document specifies the requirements for the implementation of the Sundance Rocket-IO Serial Link (RSL).

Sundance's move towards RSL aims at:

- Decreasing costs by decreasing the pin count
- Simplifying connectivity solutions by replacing the various parallel interfaces with various bus sizes used up to now by RSL links instead
- Decreasing support by using industry standard protocols and cores for serial links

As a result, the flow of data will be optimised, potential bottlenecks decreased or even eliminated and compatibility with the rest of the industry improved.

The TIM modules created will be a new range of modules with no backward compatibility options with existing TIM modules communication interfaces.

This document describes various aspects of the Rocket Serial Link (RSL). It covers the mechanical specifications for the standard, including the connector types, position and pin-outs. It covers the hardware characteristics of the interconnection standard as well as certain standard hardware building blocks.

1.1. INTRODUCTION

The Rocket-IO Serial Link (RSL) is a serial interconnection standard that is capable of data transfer speeds of up to 2.5Gbit/s per serial link (i.e. up to 250MB/s over one serial link). Up to four of these links can be combined to form a Rocket-IO Serial Link Communications Channel that is capable of data transfer up to 10Gbit/s.

Each RSL is made up of a differential Transmitter and Receiver pair. A single Rocket-IO Serial Link is a full-duplex link and can transfer data at up to 2.5Gbit/s in either direction at the same time. The transmission clock is recovered from the data stream, leaving the link as a fully independent communications link that requires no additional control or data signals.

The RSL standard is based on the Rocket-IO transceiver core embedded on Xilinx Virtex-II Pro and Virtex-IV FPGAs.

These silicon integrated transceiver cores handle the serialization/deserialization of the data streams as well as certain low-level management functions.

Rocket-IO transceivers have flexible features and allow serial transmissions over a wide range of serial standards, which require Sundance to define a framework for their use.

The RSL specification defines all the aspects of how to interconnect Sundance modules in a standard way using the integrated Rocket-IO transceivers in the Xilinx Virtex-II Pro devices. The Rocket-IO transceivers are not limited for use with Sundance RSL compliant hardware only. These transceivers, with adequate physical layers, may be used form many different serial interconnection standards. For instance, these standards include Rapid-IO, Infiniband, Serial ATA and Gigabit Ethernet.

1.2. PURPOSE

Sundance wants to reduce system complexity and increase overall speed performances by using the Rocket-IO of the Xilinx FPGAs as the main communication media between TIM modules or/and carrier boards.

1.3. APPLICABILITY

Any hardware module with a Virtex-II/Pro and a Virtex-IV FPGA device, and RSL connectors should respect these specifications.

2. APPLICABLE DOCUMENTS AND REFERENCES

2.1. APPLICABLE DOCUMENTS

2.1.1. External Documents

[1] Xilinx Virtex-II pro user guide

[2] Xilinx Rocket IO transceiver user guide

[3] Aurora reference design

[4] Aurora application examples

[5] Xilinx Virtex-4 user guide

[6] Xilinx Virtex-4 Rocket-IO Multi-Giga bits Transceivers (MGT)

2.1.2. Internal documents

- D000052-spec
- D000049H-spec
- D000049H-veri
- D000049H-impl
- RSL – pinouts
- RSL Technical specification Rev01 Iss03

2.1.3. Project Documents

- Master design project.mpp

2.2. REFERENCES

2.2.1. External documents

N.A

2.2.2. Internal documents

N.A

2.2.3. Project documents

N.A

2.3. PRECEDENCE

In the event of conflict between the text of this document, and the applicable documents cited herein, the text of this document takes precedence. Nothing in this document however, supersedes applicable laws and regulations unless a specific exemption has been obtained and is identified in the text of this document.

3. ACRONYMS, ABBREVIATIONS AND DEFINITIONS

3.1. ACRONYMS AND ABBREVIATIONS

TIM	Texas Instruments Module
RSL	Rocket-IO Serial Link
MGT	Multi-Gigabit Serial Transceiver
XAUI	10 Gigabit Attachment Unit Interface
PHY	Physical Layer
PMA	Physical Media Attachment
PCS	Physical Coding Sub layer

3.2. DEFINITIONS

Rocket-IO	Rocket-IO is the name given to a multi-gigabit serial transceiver (MGT) technology available in Xilinx Virtex-II Pro devices.
XAUI	Pronounced "Zowie". The "AUI" portion is borrowed from the Ethernet Attachment Unit Interface. The "X" represents the Roman numeral for ten and implies ten gigabits per second. The XAUI is designed as an interface extender, and the interface, which it extends, is the XGMII, the 10 Gigabit Media Independent Interface. Detailed definition
PHY	The PHY is the lowest layer within the OSI Network Model. It deals primarily with transmission of the raw bit stream over the physical transport medium. The PHY contains the functions that transmit, receive and manage the encoded data signals
Differential voltage	The differential voltage across the circuit pair is the desired signal
Common Mode Voltage	The voltage common to both sides of a differential circuit pair. The common voltage signal is the unwanted signal that may have been coupled into the transmission line. If the line is perfectly balanced, the common mode voltage cancels out. The degree of cancellation is called the common mode rejection ratio, or CMRR.
AC coupling	Use of a special circuit to remove the static (DC) components from the input signal to the amplifier in an instrument, leaving only the components of the signal that vary with time.
Pre-emphasis	In pre-emphasis, the initial differential voltage swing is boosted to create a stronger rising or falling waveform. This method compensates for high frequency loss in the transmission media that would otherwise limit the magnitude of this waveform.
PCS	The PCS is the FPGA fabric data interface of the Rocket-IO transceiver
PMA	The PMA is the Rocket-IO transceiver physical interface.
DC balanced	A channel is said to be DC Balanced if it has an equal number of 1's and 0's transmitted across it. Encoding schemes like 8B/10B are designed to ensure this.
DC coupling	Method of interfacing drivers and receivers without the use of series capacitors. A direct connection (through PCB trace) from driver to receiver.
AC coupling	Method of interfacing drivers and receivers through a series capacitor. Often used when the differential swing between drivers and receivers is compatible, but common mode voltages of driver and receiver are not. Requires that a minimum data frequency be established based on the RC time constant, necessitating a run length limit.

4. REQUIREMENTS

4.1. PRIME ITEM DEFINITION

The Rocket-IO provides high speed, serial, point-to-point communication channels within a Sundance system.

The speed over one serial channel can vary:

- From 600Mbits/s up to 3.125Mbits/s for Virtex-II FPGAs
- From 622Mbits/s up to 10.3125Mbits/s for the Virtex-IV FPGAs

Many serial protocols can be implemented using Rocket-IO technology, and none of these new serial standards are expected to out perform all of the others.

The next part of this document characterizes Sundance's current systems communication channels and derives basic communication models for the RSL.

Then, we need to review the major serial communication standards applicable to transfer in these configurations and conclude on feasibility and limitations for Sundance systems.

Finally, clear specifications can be derived so that Sundance can build reliable and compatible systems based on Rocket-IO serial transmissions.

The RSL features are:

- Full duplex communication per RSL
- Data transfer at up to 2.5Gbit/s per RSL
- Grouping of up to four RSL to form a single 10Gbit/s link
- Low voltage differential signalling (LVDS) used
- Full clock recovery from data stream
- Compatibility with emerging serial interconnection standards

4.1.1. Prime Item Diagrams

The system is going to be made of two TIMs performing transfers over the RSL using the Aurora interface. Each RSL can be built with a number of lanes. Each lane is made of two differential pairs, one to receive and one to send.

The lanes can be independent or bonded for higher transfer rates.

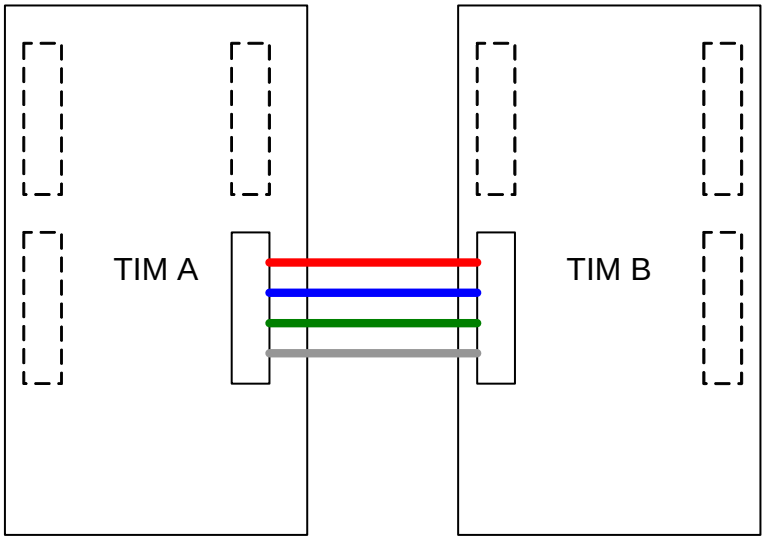


Figure 1: *4 lanes connection between 2 TIMs*

4.1.2. Interface Definition

The interface is based on Xilinx's Aurora protocol that is fully described by them.

On one side is the serial interface going to the next TIM and on the other side is the user interface, which is a standard interface as well from Xilinx, called the Local Link interface. It is as well fully specified by Xilinx.

4.1.3. Major Component List

The elements to consider in the design are:

- Virtex-II/Pro, hardware design to support RSL (power supply, clocks etc…)
- Board interconnections (connectors, cable)
- Aurora interfaces to serial links
- User interfaces to Local Link

4.1.4. Prime item characteristics

Clock rates

4.1.5. Performances

Performances depend on few things:

- Reference clock rates as the data is transferred at (clock_rate* 20 / 10) MB/s

Explanations: /10 because of 8B/10B encoding

- FIFO size, which is directly related to interface latency and flow control
- Number of lanes used for the transfer (data width)

- Speed supported by the interconnection

So with optimum FIFO size, the performances should be as follows:

	1 lane	2 lanes	4 lanes
100 MHz Ref clock (2Gb/s)	200Mb/s	400Mb/s	800Mb/s
125 MHz Ref clock (2.5Gb/s)	250Mb/s	500Mb/s	1000Mb/s
156.25 MHz Ref clock (3.125Gb/s)	312Mb/s	624Mb/s	1248Mb/s

The maximum speed over a serial link depends on the standard implemented.

4.2. SUNDANCE RSL MODELS

This section gives detailed description of the model of the RSL.

4.2.1. Current communications within Sundance systems

The current communications within Sundance systems can take place between:

- Chips on a module: like DSP / FPGA
- Modules on a carrier board, (also including between a module and its carrier board)
- Modules on different carrier boards in the same chassis, (can be front panel to front panel or direct modules inter-connections)
- Equipments or chassis

4.2.2. RSL communications within Sundance systems

So, in theory, the Rocket-IO serial link can be used in any of the combinations listed above.

We can derive four basic categories from the above communication channels:

- Chip-to-chip

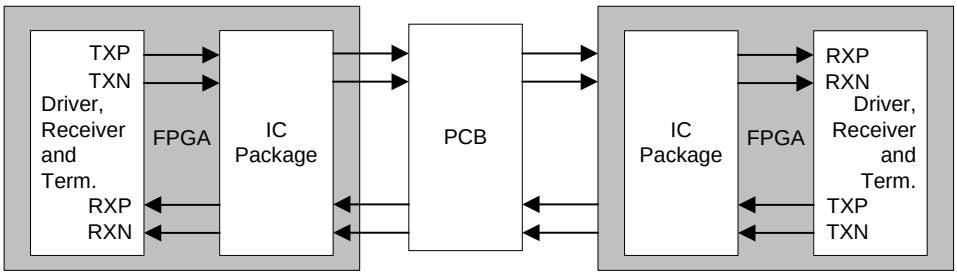


Figure 2: *Basic channel model for chip-to-chip applications*

- Between PCBs

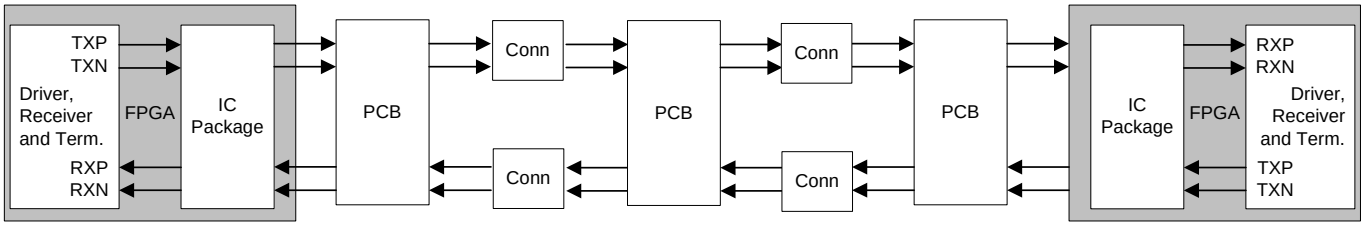


Figure 3: *Basic channel model for module-to-module application*

- Copper cable

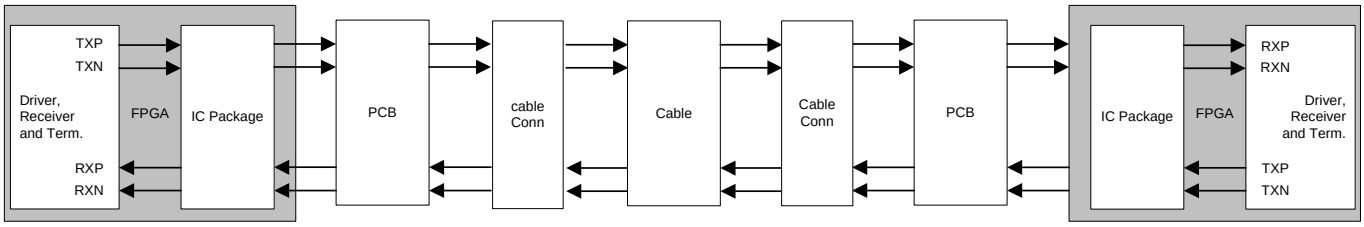


Figure 4: *Basic channel model for Copper cable application*

- Optical cable

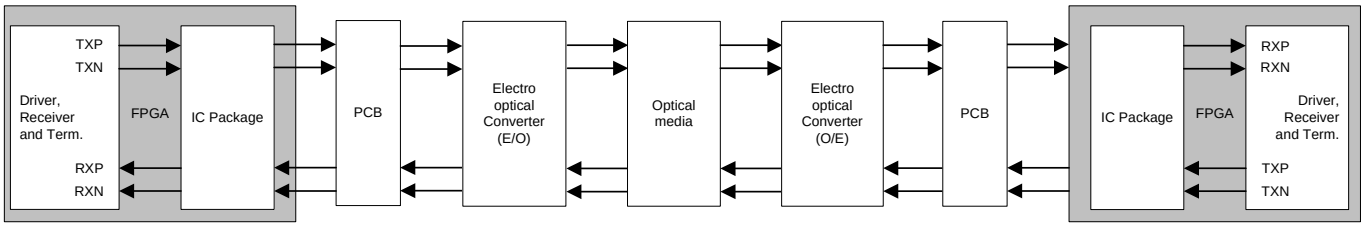


Figure 5: *Basic channel model for optical cable application*

An overview of these four basic models is available from Xilinx in "Usage Models for Multi-Gigabit serial transceivers".

All of these four categories always include the FPGA as the essential part of the system.

Then more elements are involved depending on the distance to cover:

- Connectors
- Cables
- Optical fibers
- Passive/Active components

4.2.3. RSL protocol

Sundance wants to be as flexible as possible and support as many protocols as possible. The protocols used depend on the application/system and different protocols could be used on the same module. For the module-to-module communications in the previous models Sundance implements an Aurora protocol in its FPGA firmware.

4.2.4. Basic protocols and IO rates

The next table includes specific baud rates used by the standards supported by the Rocket-IO transceiver.

Mode	Channels	IO bit rate (Gb/s)
Fiber Channel	1	1.06
		2.12
Gigabit Ethernet	1	1.25
XAUI (10 Gbit Ethernet)	4	3.125
Infiniband	1, 4, 12	2.5
Aurora	1, 2, 3, 4	0.600-3.125
Custom	1, 2, 3, 4	0.600-3.125

Table 1: *Protocols supported by the Rocket-IO transceiver*

Each of these protocols uses its specific IO bit rate, which is NOT the same as the effective data rate as data needs to be encoded/decoded in most cases.

Encoding data guarantees a DC-balanced, edge-rich serial stream, facilitating DC-or AC-coupling and clock recovery.

The FPGA Rocket-IO supports 8B/10B encoding/decoding therefore the effective data rate is 4/5 of the actual IO bit rate.

Detailed information is available in Xilinx Rocket IO transceiver User guide section "8B/10B Encoding/Decoding" in Chapter 2. (page 63)

4.2.5. RSL features

The choice of Virtex-II PRO to be fitted on-board is CRUCIAL as it determines:

- The amount of Rocket IO channels available for serial transfers
- Whether a power filtering capacitor is internal to the FPGA or must be added on-board
- The maximum serial speed

The following table include device, package and speed grade combinations showing the amount of available Rocket-IO transceivers per device, the maximum speed achievable and which devices have power filtering capacitors internal to the package.

Internal power filtering capacitor	FG packages
External power filtering capacitor	FF packages

Table 2: *Colour scheme*

FPGA speed grade	-5	2.0 Gb/s			2.0 Gb/s						
	-6	2.5 Gb/s			3.125 Gb/s						
	-7	2.5 Gb/s			3.125 Gb/s						
MGT per device		FG256	FG456	FG676	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
XC2VP2		4	4								
XC2VP4		4	4								
XC2VP7			4		8	8					
XC2VP20				8		8	8				
XC2VP30				8		8	8				
XC2VP40				8			12	No MGT			
XC2VP50							16	No MGT	16		
XC2VP70									16	20	
XC2VP100										20	No MGT

Table 3: *Virtex-II pro FPGA Device, package speed grade combinations for RSL*

Important notes relevant to the table 3:

- Wire bond packages FG256, FG456, and FG676 are also available in Pb-free versions FGG256, FGG456, and FGG676.
- The Rocket-IO transceivers in devices in the FF1148 and FF1696 packages are not bonded out to the package pins (noted No MGT in the table 3).
- -7 speed grade devices are not available in Industrial grade.

- The 2VP30, 2VP40, 2VP50, 2VP70 and 2VP100 have always had the internal capacitors. The 2VP2, 2VP4, 2VP7, and 2VP20 have had the internal capacitors beginning with data code 0317 (17th week of 2003). The date code is the last three numbers of the second line of markings on the part (same line as the package, i.e. FG456)

More detailed information is available in the Xilinx Rocket IO transceiver User guide section "Passive Filtering" in Chapter 3 (page 113).

MGT per device	SF363	FF672	FF668	FF1148	FF1152	FF1513	FF1517	FF1760
XC4VFX12	N/A		N/A					
XC4VFX20		8						
XC4VFX40		12			12			
XC4VFX60		12			16			
XC4VFX100					20		20	
XC4VFX140							24	24

Table 4: *Virtex-IV FPGA Device, package combinations for RSL*

4.3. MECHANICAL SPECIFICATIONS

This section describes the mechanical specifications of the RSL connectors (the orientation, connector type).

4.3.1. Connector type

The RSL connectors used on the TIM modules and carrier boards are 0.8mm pitch differential Samtec connectors. Any single connector makes provision for a maximum of 14 differential pairs. The Samtec QSE-014-xx-DP and QTE-014-xx-DP type of connectors are used on both the TIM modules and the Carriers.

The following two diagrams show the Top View of the QSE and QTE type connectors.

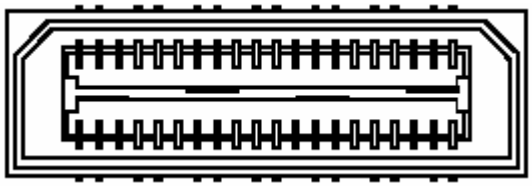


Figure 6: *RSL QSE-014-xx-DP Type Connector*

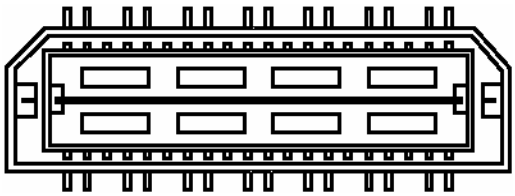


Figure 7: *RSL QTE-014-xx-DP Type Connector*

Both connectors have a single pin omitted on either side of the connector after every second pin. This architecture creates 14 individual differential pairs in the connector with proper isolation between pairs. The connector also contains a solid integrated ground plain in the middle throughout the full length of the connector. This provides addition shielding to the differential pairs. The connector characteristics for a 5.03mm QSE/QTE connector stack is given in the following table:

Impedance Mismatch (Ohm)		**Near End Cross Talk**	
Period	**Impedance**	**Frequency**	**Percentage**
30 ps	111.6 to 88.0	6.40 GHz	~1.75%
50 ps	103.6 to 94.0	10.00 GHz	~2.0%
100 ps	98.8 to 98.2		
250 ps	100.0 to 99.6		

Table 5: *QSE / QTE Connector Characteristics*

The connectors are keyed to ensure correct insertion. The default QSE/QTE stacking height is 5.03 mm. The following stacking heights are also available: 8.03mm, 11.03mm, 16.00mm, 19.00mm, and 22.00mm. The QSE connector always stays the same height. The QTE connector determines the stacking height.

The table underneath list the preferred TIM module and Carrier connector part numbers for a stacking height of 5.03mm. A description of which connectors are used where is provided in the following section.

No	Connector Description	Document Reference	Samtec Part Number
1	TIM and Carrier RSL Type A Connector	QSE-014-xx-DP	QSE-014-01-F-D-DP-A
2	TIM and Carrier RSL Type B Connector	QTE-014-xx-DP	QTE-014-01-F-D-DP-A

Table 6: *Full RSL Connector Part Numbers*

For more information about the QSE-014-xx-DP or QTE-014-xx-DP connectors please visit the Samtec website.

4.3.2. Connector location

Unlike the SHB, the RSL signals are not bi-directional. To prevent inadvertent connection from Tx-to-Tx (and Rx-to-Rx), different connector genders with different signal assignments are used.

There are two sets of signal assignments: RSL Type A (uses the Samtec *QSE-014-01-F-D-DP-A* connector) and RSL Type B (uses the Samtec *QTE-014-01-F-D-DP-A* connector). When interconnecting RSL pairs RSL Type A must always interface to RSL Type B and visa versa. *Note: It is however possible for similar connectors in the same group to have different pin-outs, depending on the connectors location.*

A connecting cable will therefore have a different gender at each end, and also be a straight one-to-one connection.

A single RSL is bi-directional. The RSL Type A signal group and the RSL Type B signal group thus contains a certain amount of bi-directional links each. RSL Type A links should NOT be confused as outputs only and RSL Type B links as inputs only.

If the TIM board space permits, an additional connector should be fitted on the underside of the module, directly beneath the connector on the top. The underside connector should have the same gender as the corresponding one on top. Connectivity is such that a single via should allow connection to both pins. So that pin 1 (top) will connect to pin 27 (bottom) and so on.

4.3.2.1. Compliant TIM module

On a TIM module the RSL connectors replace the optional second set of SHB connectors. Next to the SHB-A connector the RSL Type A connector is located. This connector is a QSE-014-xx-DP type connector. Next to the SHB-B connector the RSL Type B connector is located. This connector is a QTE-014-xx-DP type connector. These two connectors are located on the Top of the TIM Module and are ideal for module-to-module inter-connection. Identical connectors, but with a different pin-out, are located right underneath the RSL Type

A and RSL Type B connectors. This set of connectors makes it possible to connect a RSL between a TIM module and a carrier without having to route the signals through a cable.

A TIM module thus contains two sets of two RSL connectors. Each set contains one connector on the Top of the module, and one on the Bottom of the module. The RSL Type A connector is a QSE type connector, and the RSL Type B connector is a QTE connector.

The following two diagrams show the exact location of the RSL Type A and RSL Type B connectors on the Top and Bottom of a TIM module.

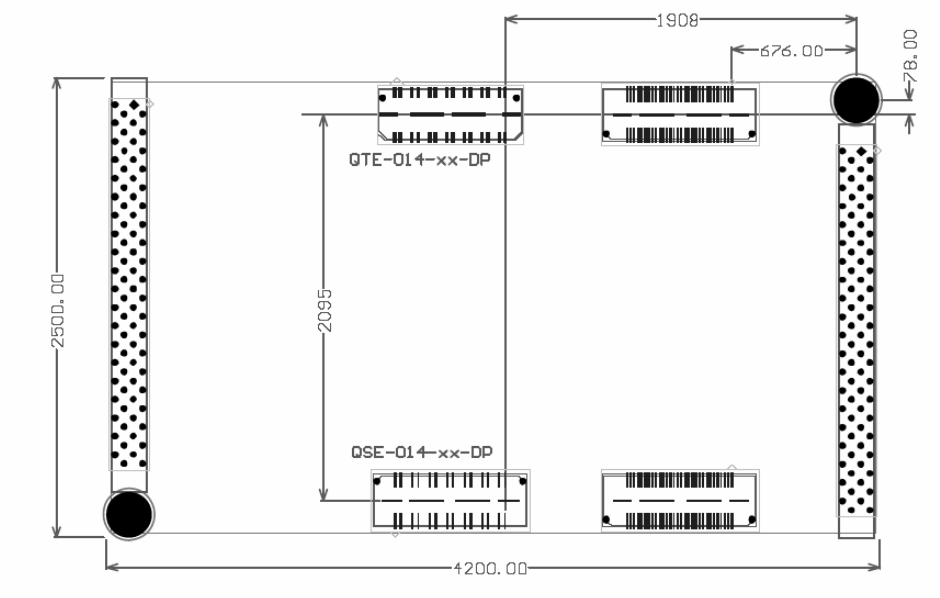


Figure 8: *Location of RSL Connectors on Top of a TIM Module*

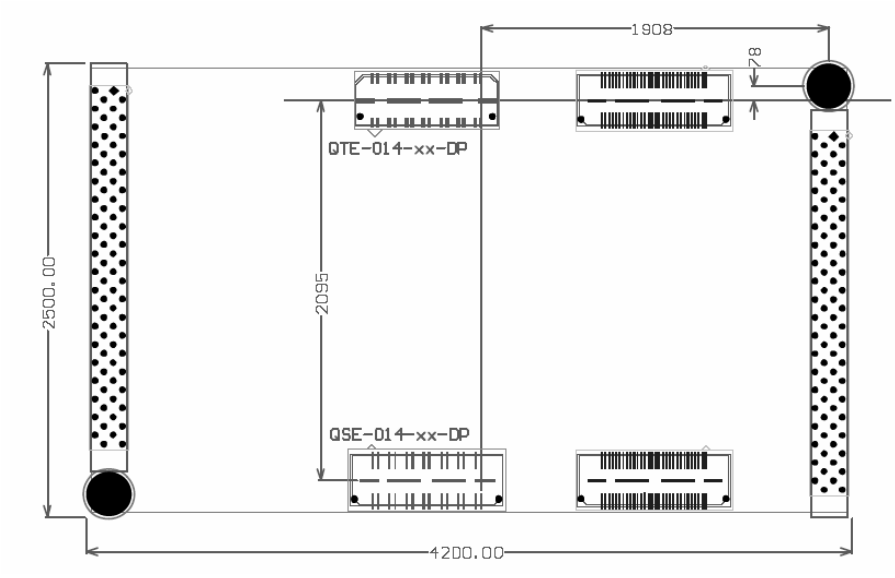


Figure 9: *Location of RSL Connectors on Bottom of a TIM Module*

4.3.2.2. Compliant TIM carrier boards

All RSL compliant carrier boards contain only two RSL connectors per TIM site. There is one RSL Type B QTE connector to mate with the RSL Type A QSE connector on the TIM module. And there is one RSL Type A QSE connector to mate with the RSL Type B QTE connector.

The exact mechanics of the connector placement may vary according to the type of the carrier board. For this reason only a diagram depicting the location of the RSL Type A and B Connectors in relation to the TIM site is shown in the following diagram:

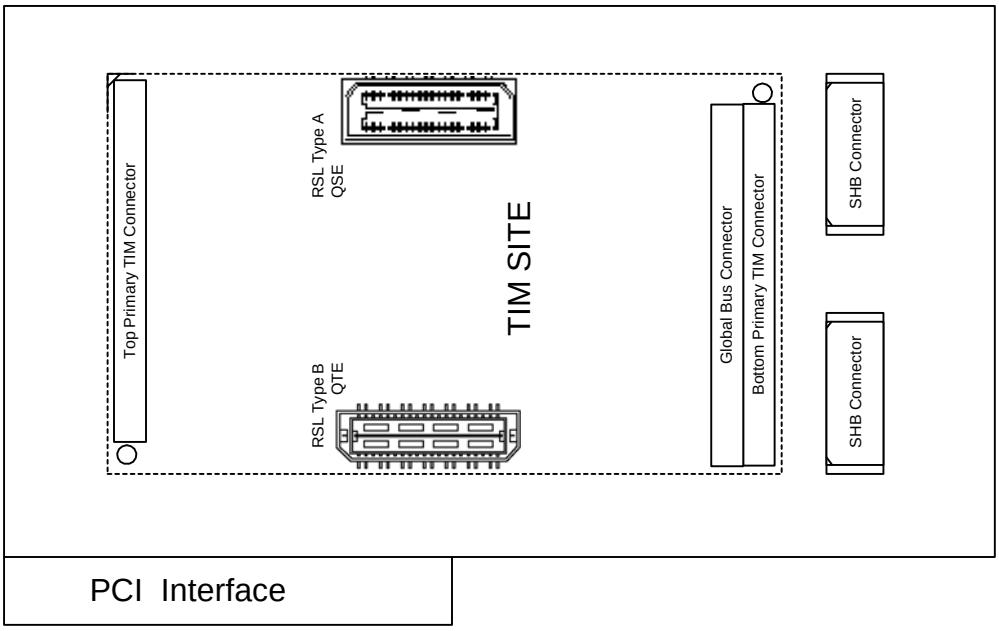


Figure 10: *Location of RSL Connectors on Carrier TIM Site*

Future RSL compliant carrier boards may expand the RSL standard to include industry standard connectors for interfaces such as Rapid-IO, SATA, Infiniband and Gigabit Ethernet. In general the design impact of conforming to one of the above-mentioned standards is very small on the hardware side, but rather large on the firmware and software side. The Xilinx Virtex-II Pro Rocket-IO transceivers and Virtex-IV Rocket-IO MGT are compatible with the above-mentioned standards.

4.3.3. Rigid Printed Circuit Boards

Rigid Printed Circuit Boards may be used to interconnect two adjacent TIM Modules. When two TIM modules are placed side by side the RSL Type A connector from the one module is adjacent to the RSL Type B connector form the other. The Rigid PCB provides a RSL Type A-to-Type B bridge between the two modules. The Rigid PCB contains a RSL Type B connector to connect to the Module RSL Type A connector and visa-versa. The routing on the PCB is a straight through one-to-one routing.

The two following diagrams illustrate this concept. The notation used to describe the location and type of connector is explained in the following section: *4.3.5*.

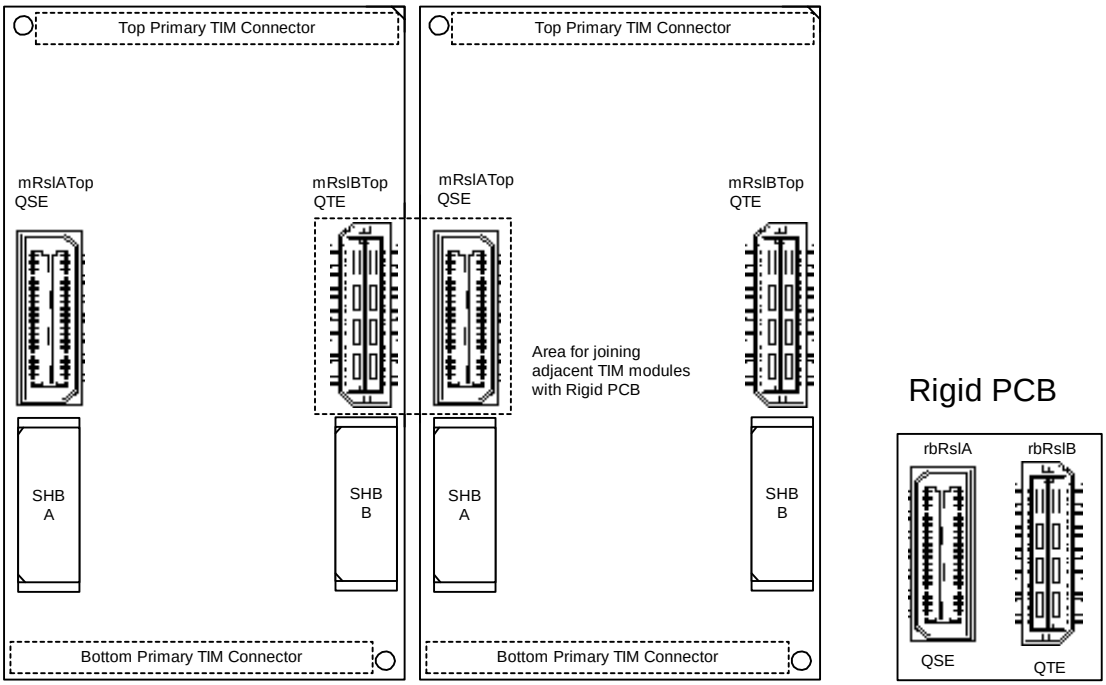


Figure 11: *Joining two adjacent TIM modules*

The above diagram illustrates the area for joining two adjacent TIM modules with a Rigid PCB. The diagram above illustrates the rigid PCB.

Note: on the rigid PCB a RSL QSE Type B connector mates with the TIM module RSL QTE Type A connector.

4.3.4. Cables

It is also possible to connect a RSL Type A connector to a RSL Type B connector using a high-speed flexible cable with a QTE connector on the one side and a QSE connector on the other side. Like the rigid PCB the cable is a straight through one-to-one cable.

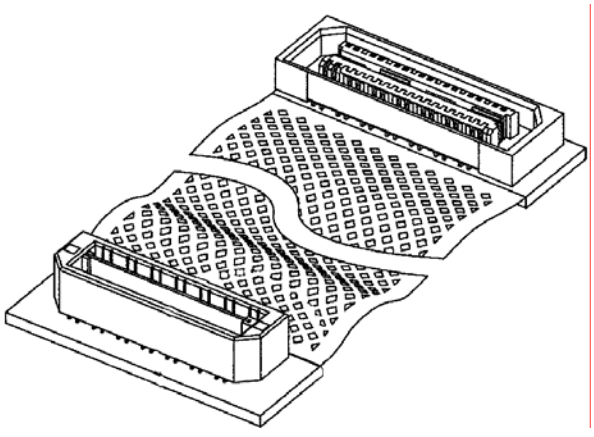


Figure 12: *RSL High Speed Data Link Cable*

The matching cable for the RSL Type A and Type B connectors is the Samtec High Speed Data Link Cable (HFEM Series). An illustration of this cable is shown the in figure 12 above. The cable comes in three lengths, measured from the outer edges of both connectors. These lengths are 76.2mm, 127.0mm and 242.32mm. The main characteristics of the cable are:

Insertion Loss		Impedance (Ohm)	
Frequency	**Loss**	**Frequency**	**Percentage**
500 MHz	-0.7 dB	Full Range	+/- 10%
1.0 GHz	-1.2 dB		
1.5 GHz	-1.3 dB		
2.0 GHz	-2.2 dB		
2.5 GHz	-2.2 dB		
3.0 GHz	-2.5 dB		
3.5 GHz	-3.4 dB		

Table 7: *HFEM cable characteristics*

4.3.5. Connector type/location

A unique identifier is assigned to each possible position. It is recommended that this identifier or similar identification appears in all RSL schematics to help with identifying the connector Type and Location.

No	Location	RSL Connector	Location	Identifier	Part Nber
1	Carrier	Type A	TIM site on Carrier	cRslA	QSE-014-xx-DP
2	Carrier	Type B	TIM site on Carrier	cRslB	QTE-014-xx-DP
3	TIM Module	Type A	Top of TIM Module	mRslATop	QSE-014-xx-DP
4	TIM Module	Type A	Bottom of TIM Module	mRslABot	QSE-014-xx-DP
5	TIM Module	Type B	Top of TIM Module	mRslBTop	QTE-014-xx-DP
6	TIM Module	Type B	Bottom of TIM Module	mRslBBot	QTE-014-xx-DP
7	RSL Cable	Type A	Module-to-Module or Module-to-Carrier	icRslA	QSE-014-xx-DP
8	RSL Cable	Type B	Module-to-Module or Module-to-Carrier	icRslB	QTE-014-xx-DP
9	Module-to-Module Bridging PCB	Type A	Rigid Module-to-Module PCB	rbRslA	QSE-014-xx-DP
10	Module-to-Module Bridging PCB	Type B	Rigid Module-to-Module PCB	rbRslB	QTE-014-xx-DP

Table 8: *RSL Connector Type and Position*

The prefix in the Identifier column in the table above helps to identify and locate the specific RSL connector/location that is referred to. The following table summarizes the use of the prefix:

No	Prefix	Abbreviation For	Usage Example
1	'c'	Carrier	cRslA = RSL Type A connector located on carrier
2	'm'	Tim Module	mRslBTop = RSL Type B connector located on the Top of the module
3	'ic'	Inter-connecting Cable	icRslA = RSLType A connector located on a module-to-module flexible cable
4	'rb'	Rigid PCB	rbRslB = RSL Type B connector located on a rigid module-to-module interconnection PCB

Table 9: *RSL Prefix explanation*

4.4. RSL PINOUTS

This section provides the pinout definitions for the different RSL connectors. The pin-outs vary depending on the RSL Type and the connector location. Depending on the Carrier or TIM module configuration there will always be the four, eight or twelve links available. The amount of links is split over the RSL Type A and RSL Type B connector. So, a module with four links will have two links on the RSL Type A connector and the other two on the RSL Type B connector. Remember that a link is made up out of four signals – a differential Tx pair and a differential Rx pair. The connector pin assignments for all connector locations and the amount of links per connector are provided in the tables in this section.

4.4.1. Naming convention

Each table defines the signal direction as seen from the local perspective of that specific connector. So if the signal name on a RSL Type A connector on a TIM module reads as mRxLink0 it means that it is a signal that is received on the module and thus transmitted from a carrier. The following diagram clarifies this issue:

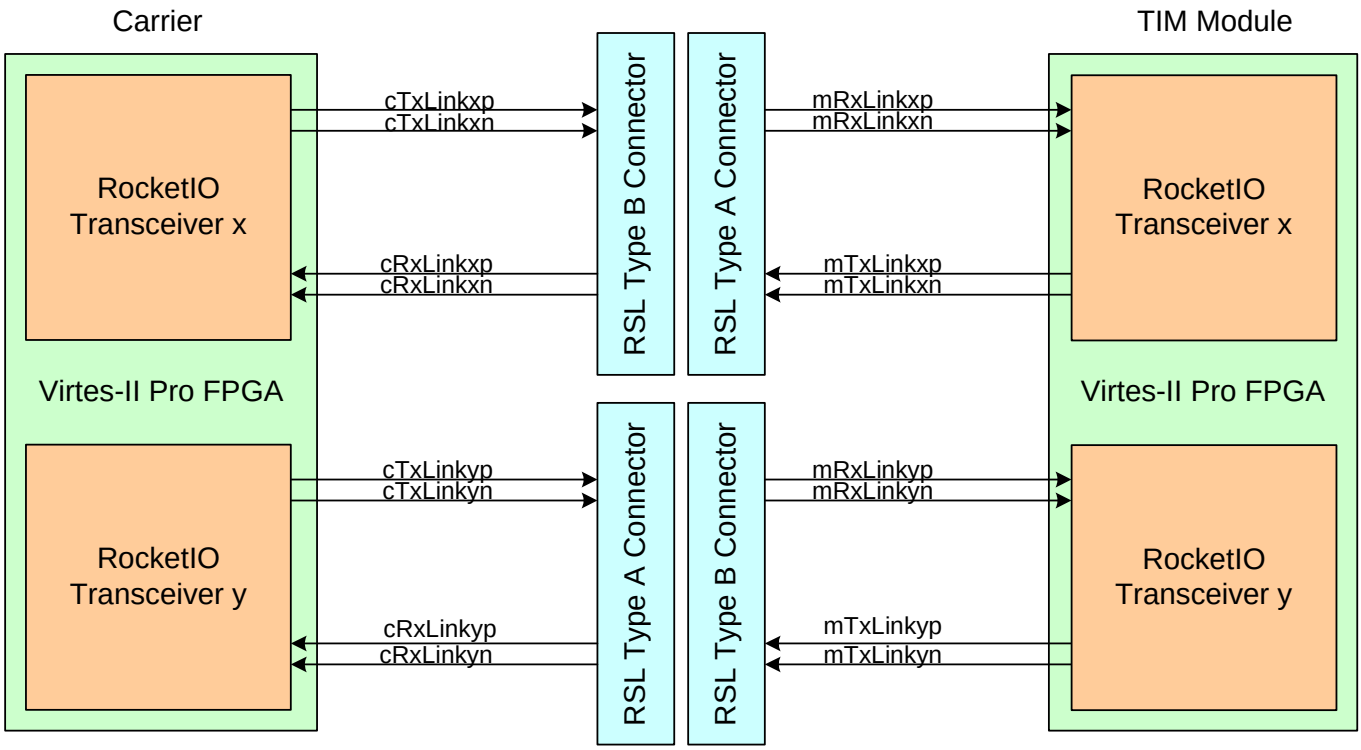


Figure 13: *RSL Naming Convention*

The use of the prefix in the signal naming convention is explained in the section titled '*Connector Type/Location*' earlier in this document.

4.4.2. TIM module

The TIM module comes with the most possibilities. The RSL links are routed to an RSL Type A connector and an RSL Type B connector on the Top of the module. The same links are also routed to the same type of connectors underneath the module. This leaves the option open for connecting the links to a carrier, or to an adjacent TIM module. Please note that the links are not multi-drop links and that you can't be connected to a carrier and to another module at the same time. Depending on the size of the FPGA mounted on the module four, eight or twelve links are available. Even thought the same type of connector is used for the RSL Type A and RSL Type B groups on the Top and the Bottom of the module the pin assignments differ. The reasoning behind this is explained in the next section – Carrier Pin Assignments.

4.4.2.1. Connectors pinouts

The next tables list the pin-outs for all of these combinations.

4.4.2.1.1. RSL type A, Top, 4 links, TIM:

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mRxLink0p	Module Receive Link 0, positive	2	mTxLink0p	Module Transmit Link 0, positive
3	mRxLink0n	Module Receive Link 0, negative	4	mTxLink0n	Module Transmit Link 0, negative
5	mRxLink1p	Module Receive Link 1, positive	6	mTxLink1p	Module Transmit Link 1, positive
7	mRxLink1n	Module Receive Link 1, negative	8	mTxLink1n	Module Transmit Link 1, negative
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.2.1.2. RSL Type B, Top, 4 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mTxLink0p	Module Transmit Link 0, positive	2	mRxLink0p	Module Receive Link 0, positive
3	mTxLink0n	Module Transmit Link 0, negative	4	mRxLink0n	Module Receive Link 0, negative
5	mTxLink1p	Module Transmit Link 1, positive	6	mRxLink1p	Module Receive Link 1, positive
7	mTxLink1n	Module Transmit Link 1, negative	8	mRxLink1n	Module Receive Link 1, negative
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.2.1.3. RSL Type A, Top, 8 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	RxLink0p	Receive Link 0, positive	2	TxLink0p	Transmit Link 0, positive
3	RxLink0n	Receive Link 0, negative	4	TxLink0n	Transmit Link 0, negative
5	RxLink1p	Receive Link 1, positive	6	TxLink1p	Transmit Link 1, positive
7	RxLink1n	Receive Link 1, negative	8	TxLink1n	Transmit Link 1, negative
9	RxLink2p	Receive Link 2, positive	10	TxLink2p	Transmit Link 2, positive
11	RxLink2n	Receive Link 2, negative	12	TxLink2n	Transmit Link 2, negative
13	RxLink3p	Receive Link 3, positive	14	TxLink3p	Transmit Link 3, positive
15	RxLink3n	Receive Link 3, negative	16	TxLink3n	Transmit Link 3, negative
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.2.1.4. RSL Type B, Top, 8 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	TxLink0p	Transmit Link 0, positive	2	RxLink0p	Receive Link 0, positive
3	TxLink0n	Transmit Link 0, negative	4	RxLink0n	Receive Link 0, negative
5	TxLink1p	Transmit Link 1, positive	6	RxLink1p	Receive Link 1, positive
7	TxLink1n	Transmit Link 1, negative	8	RxLink1n	Receive Link 1, negative
9	TxLink2p	Transmit Link 2, positive	10	RxLink2p	Receive Link 2, positive
11	TxLink2n	Transmit Link 2, negative	12	RxLink2n	Receive Link 2, negative
13	TxLink3p	Transmit Link 3, positive	14	RxLink3p	Receive Link 3, positive
15	TxLink3n	Transmit Link 3, negative	16	RxLink3n	Receive Link 3, negative
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.2.1.5. RSL Type A, Top, 12 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mRxLink0p	Receive Link 0, positive	2	mTxLink0p	Transmit Link 0, positive
3	mRxLink0n	Receive Link 0, negative	4	mTxLink0n	Transmit Link 0, negative
5	mRxLink1p	Receive Link 1, positive	6	mTxLink1p	Transmit Link 1, positive
7	mRxLink1n	Receive Link 1, negative	8	mTxLink1n	Transmit Link 1, negative
9	mRxLink2p	Receive Link 2, positive	10	mTxLink2p	Transmit Link 2, positive
11	mRxLink2n	Receive Link 2, negative	12	mTxLink2n	Transmit Link 2, negative
13	mRxLink3p	Receive Link 3, positive	14	mTxLink3p	Transmit Link 3, positive
15	mRxLink3n	Receive Link 3, negative	16	mTxLink3n	Transmit Link 3, negative
17	mRxLink4p	Receive Link 4, positive	18	mTxLink4p	Transmit Link 4, positive
19	mRxLink4n	Receive Link 4, negative	20	mTxLink4n	Transmit Link 4, negative
21	mRxLink5p	Receive Link 5, positive	22	mTxLink5p	Transmit Link 5, positive
23	mRxLink5n	Receive Link 5, negative	24	mTxLink5n	Transmit Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.2.1.6. RSL Type B, Top, 12 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mTxLink0p	Module Transmit Link 0, positive	2	mRxLink0p	Module Receive Link 0, positive
3	mTxLink0n	Module Transmit Link 0, negative	4	mRxLink0n	Module Receive Link 0, negative
5	mTxLink1p	Module Transmit Link 1, positive	6	mRxLink1p	Module Receive Link 1, positive
7	mTxLink1n	Module Transmit Link 1, negative	8	mRxLink1n	Module Receive Link 1, negative
9	mTxLink2p	Module Transmit Link 2, positive	10	mRxLink2p	Module Receive Link 2, positive
11	mTxLink2n	Module Transmit Link 2, negative	12	mRxLink2n	Module Receive Link 2, negative
13	mTxLink3p	Module Transmit Link 3, positive	14	mRxLink3p	Module Receive Link 3, positive
15	mTxLink3n	Module Transmit Link 3, negative	16	mRxLink3n	Module Receive Link 3, negative
17	mTxLink4p	Module Transmit Link 4, positive	18	mRxLink4p	Module Receive Link 4, positive
19	mTxLink4n	Module Transmit Link 4, negative	20	mRxLink4n	Module Receive Link 4, negative
21	mTxLink5p	Module Transmit Link 5, positive	22	mRxLink5p	Module Receive Link 5, positive
23	mTxLink5n	Module Transmit Link 5, negative	24	mRxLink5n	Module Receive Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.2.1.7. RSL Type A, Bottom, 4 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mTxLink0p	Module Transmit Link 0, positive	2	mRxLink0p	Module Receive Link 0, positive
3	mTxLink0n	Module Transmit Link 0, negative	4	mRxLink0n	Module Receive Link 0, negative
5	mTxLink1p	Module Transmit Link 1, positive	6	mRxLink1p	Module Receive Link 1, positive
7	mTxLink1n	Module Transmit Link 1, negative	8	mRxLink1n	Module Receive Link 1, negative
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.2.1.8. RSL Type B, Bottom, 4 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mRxLink0p	Module Receive Link 0, positive	2	mTxLink0p	Module Transmit Link 0, positive
3	mRxLink0n	Module Receive Link 0, negative	4	mTxLink0n	Module Transmit Link 0, negative
5	mRxLink1p	Module Receive Link 1, positive	6	mTxLink1p	Module Transmit Link 1, positive
7	mRxLink1n	Module Receive Link 1, negative	8	mTxLink1n	Module Transmit Link 1, negative
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.2.1.9. RSL Type A, Bottom, 8 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mTxLink0p	Module Transmit Link 0, positive	2	mRxLink0p	Module Receive Link 0, positive
3	mTxLink0n	Module Transmit Link 0, negative	4	mRxLink0n	Module Receive Link 0, negative
5	mTxLink1p	Module Transmit Link 1, positive	6	mRxLink1p	Module Receive Link 1, positive
7	mTxLink1n	Module Transmit Link 1, negative	8	mRxLink1n	Module Receive Link 1, negative
9	mTxLink2p	Module Transmit Link 2, positive	10	mRxLink2p	Module Receive Link 2, positive
11	mTxLink2n	Module Transmit Link 2, negative	12	mRxLink2n	Module Receive Link 2, negative
13	mTxLink3p	Module Transmit Link 3, positive	14	mRxLink3p	Module Receive Link 3, positive
15	mTxLink3n	Module Transmit Link 3, negative	16	mRxLink3n	Module Receive Link 3, negative
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.2.1.10. RSL Type B, Bottom, 8 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mxLink0p	Module Receive Link 0, positive	2	mxLink0p	Module Transmit Link 0, positive
3	mxLink0n	Module Receive Link 0, negative	4	mxLink0n	Module Transmit Link 0, negative
5	mxLink1p	Module Receive Link 1, positive	6	mxLink1p	Module Transmit Link 1, positive
7	mxLink1n	Module Receive Link 1, negative	8	mxLink1n	Module Transmit Link 1, negative
9	mxLink2p	Module Receive Link 2, positive	10	mxLink2p	Module Transmit Link 2, positive
11	mxLink2n	Module Receive Link 2, negative	12	mxLink2n	Module Transmit Link 2, negative
13	mxLink3p	Module Receive Link 3, positive	14	mxLink3p	Module Transmit Link 3, positive
15	mxLink3n	Module Receive Link 3, negative	16	mxLink3n	Module Transmit Link 3, negative
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.2.1.11. RSL Type A, Bottom, 12 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mTxLink0p	Module Transmit Link 0, positive	2	mRxLink0p	Module Receive Link 0, positive
3	mTxLink0n	Module Transmit Link 0, negative	4	mRxLink0n	Module Receive Link 0, negative
5	mTxLink1p	Module Transmit Link 1, positive	6	mRxLink1p	Module Receive Link 1, positive
7	mTxLink1n	Module Transmit Link 1, negative	8	mRxLink1n	Module Receive Link 1, negative
9	mTxLink2p	Module Transmit Link 2, positive	10	mRxLink2p	Module Receive Link 2, positive
11	mTxLink2n	Module Transmit Link 2, negative	12	mRxLink2n	Module Receive Link 2, negative
13	mTxLink3p	Module Transmit Link 3, positive	14	mRxLink3p	Module Receive Link 3, positive
15	mTxLink3n	Module Transmit Link 3, negative	16	mRxLink3n	Module Receive Link 3, negative
17	mTxLink4p	Module Transmit Link 4, positive	18	mRxLink4p	Module Receive Link 4, positive
19	mTxLink4n	Module Transmit Link 4, negative	20	mRxLink4n	Module Receive Link 4, negative
21	mTxLink5p	Module Transmit Link 5, positive	22	mRxLink5p	Module Receive Link 5, positive
23	mTxLink5n	Module Transmit Link 5, negative	24	mRxLink5n	Module Receive Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.2.1.12. RSL Type B, Bottom, 12 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mRxLink0p	Receive Link 0, positive	2	mTxLink0p	Transmit Link 0, positive
3	mRxLink0n	Receive Link 0, negative	4	mTxLink0n	Transmit Link 0, negative
5	mRxLink1p	Receive Link 1, positive	6	mTxLink1p	Transmit Link 1, positive
7	mRxLink1n	Receive Link 1, negative	8	mTxLink1n	Transmit Link 1, negative
9	mRxLink2p	Receive Link 2, positive	10	mTxLink2p	Transmit Link 2, positive
11	mRxLink2n	Receive Link 2, negative	12	mTxLink2n	Transmit Link 2, negative
13	mRxLink3p	Receive Link 3, positive	14	mTxLink3p	Transmit Link 3, positive
15	mRxLink3n	Receive Link 3, negative	16	mTxLink3n	Transmit Link 3, negative
17	mRxLink4p	Receive Link 4, positive	18	mTxLink4p	Transmit Link 4, positive
19	mRxLink4n	Receive Link 4, negative	20	mTxLink4n	Transmit Link 4, negative
21	mRxLink5p	Receive Link 5, positive	22	mTxLink5p	Transmit Link 5, positive
23	mRxLink5n	Receive Link 5, negative	24	mTxLink5n	Transmit Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.3. Carrier board

Care should be taken with the assignment of pin names on all carriers to ensure that the Tx and Rx pairs on the carrier match that of the TIM module. The signal assignments on the TIM module is confusing as the same type of connector is used for the RSL Type A signals on the Top and the Bottom of the module, but with different signal assignments give to pin one on both connectors. The reason for this strange pin assignment is to easy the routing of the differential pairs on the TIM modules. Extreme care should be taken when routing the RSL links as all stubs and vias should be minimized. This topic is further discussed in the '*Electrical Specifications*' section in this document. The reasoning behind the signal assignments on the TIM module is illustrated in the following diagram:

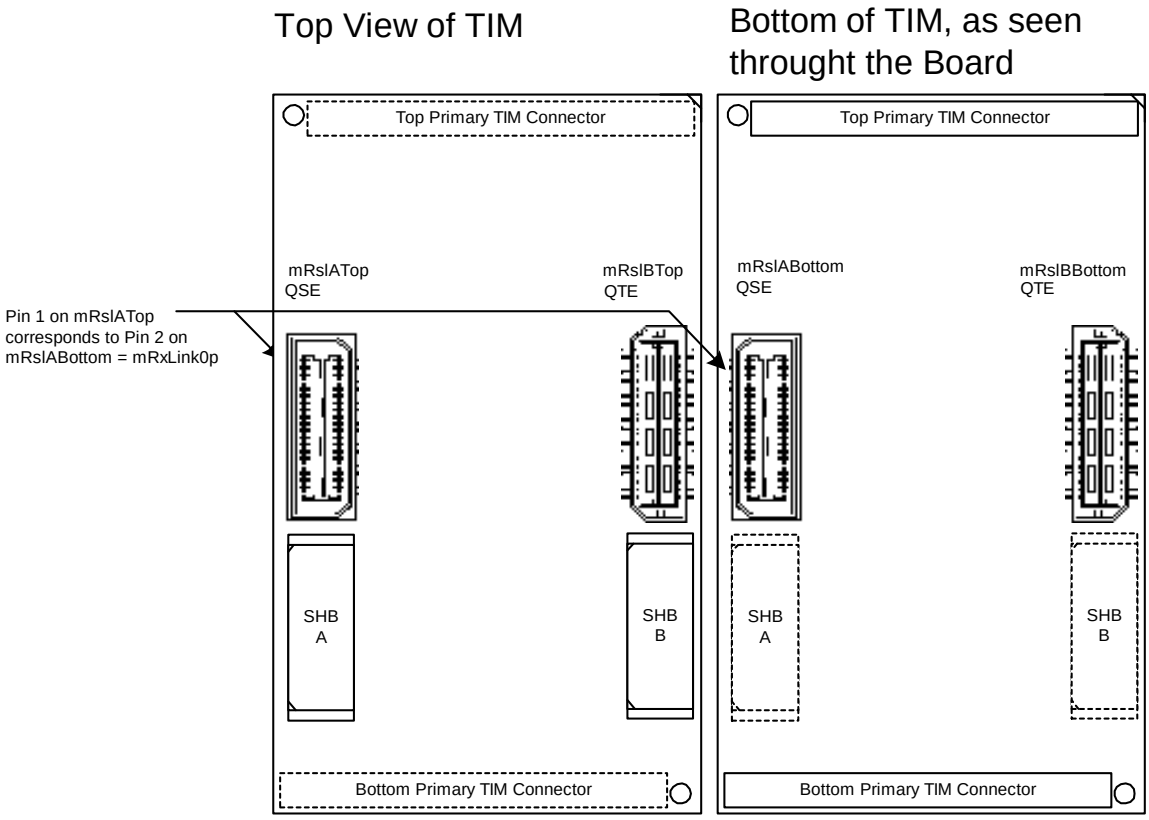
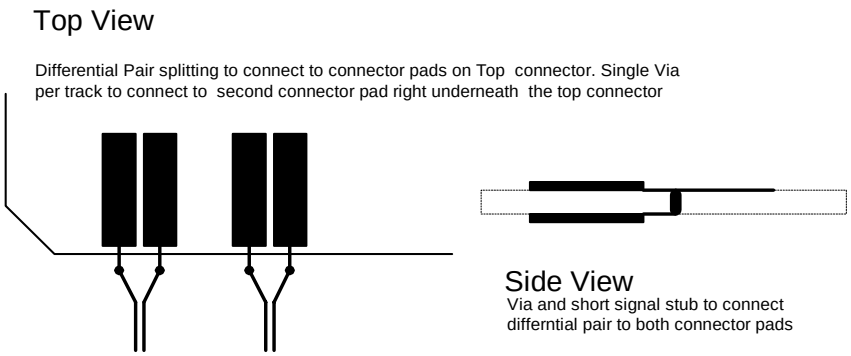


Figure 14: *Top and Bottom RSL Connector on TIM Module*



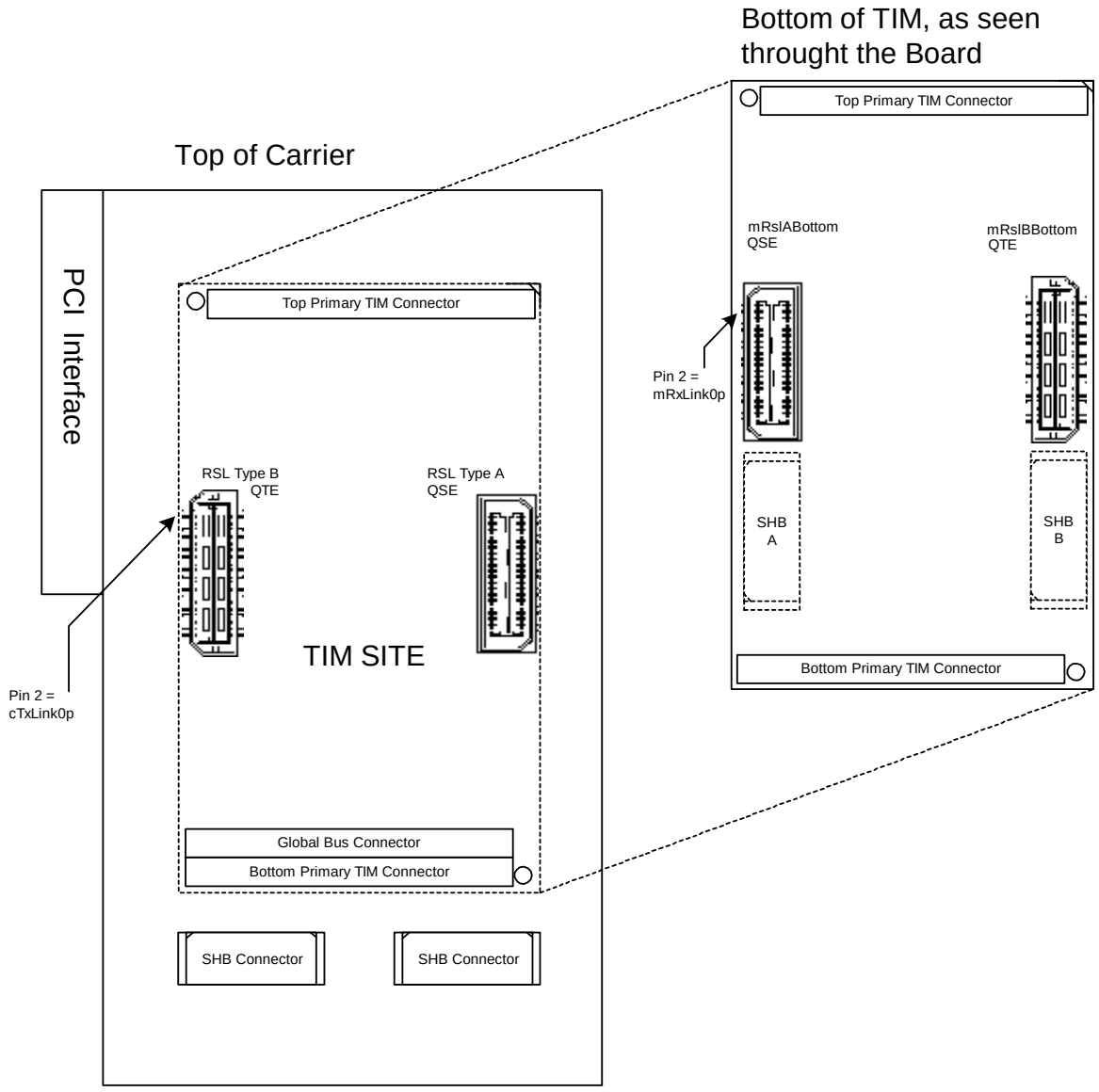


Figure 15: *RSL Connection between TIM Module and Carrier*

The above figure illustrates how the Bottom RSL Type A and Type B connectors connect to the RSL connectors on the Carrier. Pin 1 on the RSL Type A connector on the Bottom of the TIM module is mTxLink0p. This connects to pin 1 on the RSL Type B connector on the carrier – cRxLink0p. Pin 2 on the module, mRxLink0p, connects to cTxLink0p on the carrier. The full lists of RSL Type A and RSL Type B connectors for carriers follow in the tables underneath.

4.4.3.1. Connectors pinouts

The following sub-sections define the connector pinouts on the carrier board.

4.4.3.1.1. RSL Type A, 4 Links, Carrier

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	cTxLink0p	Carrier Transmit Link 0, positive	2	cRxLink0p	Carrier Receive Link 0, positive
3	cTxLink0n	Carrier Transmit Link 0, negative	4	cxLink0n	Carrier Receive Link 0, negative
5	cTxLink1p	Carrier Transmit Link 1, positive	6	cxLink1p	Carrier Receive Link 1, positive
7	cTxLink1n	Carrier Transmit Link 1, negative	8	cxLink1n	Carrier Receive Link 1, negative
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.3.1.2. RSL Type B, 4 Links, Carrier

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	cRxLink0p	Carrier Receive Link 0, positive	2	cTxLink0p	Carrier Transmit Link 0, positive
3	cRxLink0n	Carrier Receive Link 0, negative	4	cTxLink0n	Carrier Transmit Link 0, negative
5	cRxLink1p	Carrier Receive Link 1, positive	6	cTxLink1p	Carrier Transmit Link 1, positive
7	cRxLink1n	Carrier Receive Link 1, negative	8	cTxLink1n	Carrier Transmit Link 1, negative
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.3.1.3. RSL Type A, 8 Links, Carrier

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	cTxLink0p	Carrier Transmit Link 0, positive	2	cRxLink0p	Carrier Receive Link 0, positive
3	cTxLink0n	Carrier Transmit Link 0, negative	4	cxLink0n	Carrier Receive Link 0, negative
5	cTxLink1p	Carrier Transmit Link 1, positive	6	cxLink1p	Carrier Receive Link 1, positive
7	cTxLink1n	Carrier Transmit Link 1, negative	8	cxLink1n	Carrier Receive Link 1, negative
9	cTxLink2p	Carrier Transmit Link 2, positive	10	cxLink2p	Carrier Receive Link 2, positive
11	cTxLink2n	Carrier Transmit Link 2, negative	12	cxLink2n	Carrier Receive Link 2, negative
13	cTxLink3p	Carrier Transmit Link 3, positive	14	cxLink3p	Carrier Receive Link 3, positive
15	cTxLink3n	Carrier Transmit Link 3, negative	16	cxLink3n	Carrier Receive Link 3, negative
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.3.1.4. RSL Type B, 8 Links, Carrier

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	cRxLink0p	Carrier Receive Link 0, positive	2	cTxLink0p	Carrier Transmit Link 0, positive
3	cRxLink0n	Carrier Receive Link 0, negative	4	cTxLink0n	Carrier Transmit Link 0, negative
5	cRxLink1p	Carrier Receive Link 1, positive	6	cTxLink1p	Carrier Transmit Link 1, positive
7	cRxLink1n	Carrier Receive Link 1, negative	8	cTxLink1n	Carrier Transmit Link 1, negative
9	cRxLink2p	Carrier Receive Link 2, positive	10	cTxLink2p	Carrier Transmit Link 2, positive
11	cRxLink2n	Carrier Receive Link 2, negative	12	cTxLink2n	Carrier Transmit Link 2, negative
13	cRxLink3p	Carrier Receive Link 3, positive	14	cTxLink3p	Carrier Transmit Link 3, positive
15	cRxLink3n	Carrier Receive Link 3, negative	16	cTxLink3n	Carrier Transmit Link 3, negative
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.3.1.5. RSL Type A, 12 Links, Carrier

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	cTxLink0p	Carrier Transmit Link 0, positive	2	cRxLink0p	Carrier Receive Link 0, positive
3	cTxLink0n	Carrier Transmit Link 0, negative	4	cxLink0n	Carrier Receive Link 0, negative
5	cTxLink1p	Carrier Transmit Link 1, positive	6	cxLink1p	Carrier Receive Link 1, positive
7	cTxLink1n	Carrier Transmit Link 1, negative	8	cxLink1n	Carrier Receive Link 1, negative
9	cTxLink2p	Carrier Transmit Link 2, positive	10	cxLink2p	Carrier Receive Link 2, positive
11	cTxLink2n	Carrier Transmit Link 2, negative	12	cxLink2n	Carrier Receive Link 2, negative
13	cTxLink3p	Carrier Transmit Link 3, positive	14	cxLink3p	Carrier Receive Link 3, positive
15	cTxLink3n	Carrier Transmit Link 3, negative	16	cxLink3n	Carrier Receive Link 3, negative
17	cTxLink4p	Carrier Transmit Link 4, positive	18	cxLink4p	Carrier Receive Link 4, positive
19	cTxLink4n	Carrier Transmit Link 4, negative	20	cxLink4n	Carrier Receive Link 4, negative
21	cTxLink5p	Carrier Transmit Link 5, positive	22	cxLink5p	Carrier Receive Link 5, positive
23	cTxLink5n	Carrier Transmit Link 5, negative	24	cxLink5n	Carrier Receive Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.3.1.6. RSL Type B, 12 Links, Carrier

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	cRxLink0p	Carrier Receive Link 0, positive	2	cTxLink0p	Carrier Transmit Link 0, positive
3	cRxLink0n	Carrier Receive Link 0, negative	4	cTxLink0n	Carrier Transmit Link 0, negative
5	cRxLink1p	Carrier Receive Link 1, positive	6	cTxLink1p	Carrier Transmit Link 1, positive
7	cRxLink1n	Carrier Receive Link 1, negative	8	cTxLink1n	Carrier Transmit Link 1, negative
9	cRxLink2p	Carrier Receive Link 2, positive	10	cTxLink2p	Carrier Transmit Link 2, positive
11	cRxLink2n	Carrier Receive Link 2, negative	12	cTxLink2n	Carrier Transmit Link 2, negative
13	cRxLink3p	Carrier Receive Link 3, positive	14	cTxLink3p	Carrier Transmit Link 3, positive
15	cRxLink3n	Carrier Receive Link 3, negative	16	cTxLink3n	Carrier Transmit Link 3, negative
17	cRxLink4p	Carrier Receive Link 4, positive	18	cTxLink4p	Carrier Transmit Link 4, positive
19	cRxLink4n	Carrier Receive Link 4, negative	20	cTxLink4n	Carrier Transmit Link 4, negative
21	cRxLink5p	Carrier Receive Link 5, positive	22	cTxLink5p	Carrier Transmit Link 5, positive
23	cRxLink5n	Carrier Receive Link 5, negative	24	cTxLink5n	Carrier Transmit Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.4. Rigid PCB and RSL Cable

The purpose of the rigid PCB is to connect the RSL links of two adjacent TIM modules to each other. When two TIM modules are placed next to each other one Top RSL Type A and one Top RSL Type B connector is right next to each other. The reasoning behind the pin assignments is illustrated in the following diagram:

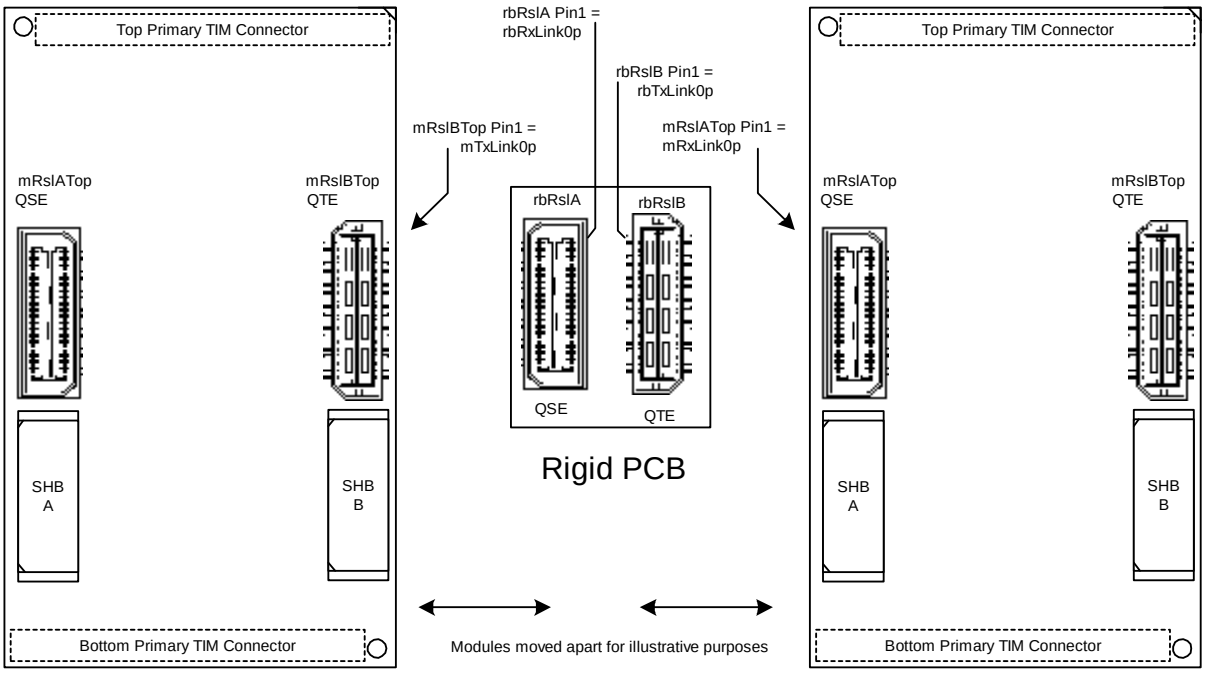


Figure 16: *Rigid PCB Pin Assignments*

On the TIM Module RSL Type B connector pin 1, mRSLBTop, is mTxLink0p. This signal connects to a RSL Type A connector on the Rigid PCB, called rbRxLink0p. Similarly mRxLink0p on the TIM Module RSL Type A connector connects to rbTxLink0p on the rigid PCB. The signals on the rigid PCB map 1-to-1 to each other. Thus rbRxLink0p connects straight to rbTxLink0p.

The RSL interconnecting cable serves the same purpose of the rigid PCB, with the exception that it can interconnect modules that are not adjacent to each other. The signal allocations on the connector pins are the same and the cable also maps one-to-one. The only difference between the Rigid PCB and the Interconnecting Cable is the prefix assigned to the signal names. The Rigid PCB signals use ‘rb’ as a prefix and the Interconnecting Cable uses ‘ic’ as a prefix. No distinction is made between four, eight or twelve links as all the links are interconnected on both the PCB and the cable. Note that six (total of 12 over two connectors) of the possible seven links per connector are connected over the PCB. The seventh link is left as reserved like on all the other connectors. The seventh link is however connected on the inter-connecting cable.

4.4.4.1. Connectors pinouts

The signal assignments for the RSL connectors on the Rigid PCB and the Interconnecting Cable follow.

4.4.4.1.1. RSL Type A, Top, Rigid PCB

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	rbRxLink0p	RPCB Receive Link 0, positive	2	rbTxLink0p	RPCB Transmit Link 0, positive
3	RxLink0n	RPCB Receive Link 0, negative	4	rbTxLink0n	RPCB Transmit Link 0, negative
5	rbRxLink1p	RPCB Receive Link 1, positive	6	rbTxLink1p	RPCB Transmit Link 1, positive
7	rbRxLink1n	RPCB Receive Link 1, negative	8	rbTxLink1n	RPCB Transmit Link 1, negative
9	rbRxLink2p	RPCB Receive Link 2, positive	10	rbTxLink2p	RPCB Transmit Link 2, positive
11	rbRxLink2n	RPCB Receive Link 2, negative	12	rbTxLink2n	RPCB Transmit Link 2, negative
13	rbRxLink3p	RPCB Receive Link 3, positive	14	rbTxLink3p	RPCB Transmit Link 3, positive
15	rbRxLink3n	RPCB Receive Link 3, negative	16	rbTxLink3n	RPCB Transmit Link 3, negative
17	rbRxLink4p	RPCB Receive Link 4, positive	18	rbTxLink4p	RPCB Transmit Link 4, positive
19	rbRxLink4n	RPCB Receive Link 4, negative	20	rbTxLink4n	RPCB Transmit Link 4, negative
21	rbRxLink5p	RPCB Receive Link 5, positive	22	rbTxLink5p	RPCB Transmit Link 5, positive
23	rbRxLink5n	RPCB Receive Link 5, negative	24	rbTxLink5n	RPCB Transmit Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.4.1.2. RSL Type B, Top, Rigid PCB

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	rbTxLink0p	RPCB Transmit Link 0, positive	2	rbRxLink0p	RPCB Receive Link 0, positive
3	rbTxLink0n	RPCB Transmit Link 0, negative	4	rbRxLink0n	RPCB Receive Link 0, negative
5	rbTxLink1p	RPCB Transmit Link 1, positive	6	rbRxLink1p	RPCB Receive Link 1, positive
7	rbTxLink1n	RPCB Transmit Link 1, negative	8	rbRxLink1n	RPCB Receive Link 1, negative
9	rbTxLink2p	RPCB Transmit Link 2, positive	10	rbRxLink2p	RPCB Receive Link 2, positive
11	rbTxLink2n	RPCB Transmit Link 2, negative	12	rbRxLink2n	RPCB Receive Link 2, negative
13	rbTxLink3p	RPCB Transmit Link 3, positive	14	rbRxLink3p	RPCB Receive Link 3, positive
15	rbTxLink3n	RPCB Transmit Link 3, negative	16	rbRxLink3n	RPCB Receive Link 3, negative
17	rbTxLink4p	RPCB Transmit Link 4, positive	18	rbRxLink4p	RPCB Receive Link 4, positive
19	rbTxLink4n	RPCB Transmit Link 4, negative	20	rbRxLink4n	RPCB Receive Link 4, negative
21	rbTxLink5p	RPCB Transmit Link 5, positive	22	rbRxLink5p	RPCB Receive Link 5, positive
23	rbTxLink5n	RPCB Transmit Link 5, negative	24	rbRxLink5n	RPCB Receive Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

4.4.4.1.3. RSL Type A, Top, Inter-connecting Cable

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	icRxLink0p	Cable Receive Link 0, positive	2	icTxLink0p	Cable Transmit Link 0, positive
3	icRxLink0n	Cable Receive Link 0, negative	4	icTxLink0n	Cable Transmit Link 0, negative
5	icRxLink1p	Cable Receive Link 1, positive	6	icTxLink1p	Cable Transmit Link 1, positive
7	icRxLink1n	Cable Receive Link 1, negative	8	icTxLink1n	Cable Transmit Link 1, negative
9	icRxLink2p	Cable Receive Link 2, positive	10	icTxLink2p	Cable Transmit Link 2, positive
11	icRxLink2n	Cable Receive Link 2, negative	12	icTxLink2n	Cable Transmit Link 2, negative
13	icRxLink3p	Cable Receive Link 3, positive	14	icTxLink3p	Cable Transmit Link 3, positive
15	icRxLink3n	Cable Receive Link 3, negative	16	icTxLink3n	Cable Transmit Link 3, negative
17	icRxLink4p	Cable Receive Link 4, positive	18	icTxLink4p	Cable Transmit Link 4, positive
19	icRxLink4n	Cable Receive Link 4, negative	20	icTxLink4n	Cable Transmit Link 4, negative
21	icRxLink5p	Cable Receive Link 5, positive	22	icTxLink5p	Cable Transmit Link 5, positive
23	icRxLink5n	Cable Receive Link 5, negative	24	icTxLink5n	Cable Transmit Link 5, negative
25	icRxLink6p	Cable Receive Link 6, positive	26	icTxLink6p	Cable Transmit Link 6, positive
27	icRxLink6n	Cable Receive Link 6, negative	28	icTxLink6n	Cable Transmit Link 6, negative

4.4.4.1.4. RSL Type B, Top, Inter-connecting Cable

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	icTxLink0p	Cable Transmit Link 0, positive	2	icRxLink0p	Cable Receive Link 0, positive
3	icTxLink0n	Cable Transmit Link 0, negative	4	icRxLink0n	Cable Receive Link 0, negative
5	icTxLink1p	Cable Transmit Link 1, positive	6	icRxLink1p	Cable Receive Link 1, positive
7	icTxLink1n	Cable Transmit Link 1, negative	8	icRxLink1n	Cable Receive Link 1, negative
9	icTxLink2p	Cable Transmit Link 2, positive	10	icRxLink2p	Cable Receive Link 2, positive
11	icTxLink2n	Cable Transmit Link 2, negative	12	icRxLink2n	Cable Receive Link 2, negative
13	icTxLink3p	Cable Transmit Link 3, positive	14	icRxLink3p	Cable Receive Link 3, positive
15	icTxLink3n	Cable Transmit Link 3, negative	16	icRxLink3n	Cable Receive Link 3, negative
17	icTxLink4p	Cable Transmit Link 4, positive	18	icRxLink4p	Cable Receive Link 4, positive
19	icTxLink4n	Cable Transmit Link 4, negative	20	icRxLink4n	Cable Receive Link 4, negative
21	icTxLink5p	Cable Transmit Link 5, positive	22	icRxLink5p	Cable Receive Link 5, positive
23	icTxLink5n	Cable Transmit Link 5, negative	24	icRxLink5n	Cable Receive Link 5, negative
25	icTxLink6p	Cable Transmit Link 6, positive	26	icRxLink6p	Cable Receive Link 6, positive
27	icTxLink6n	Cable Transmit Link 6, negative	28	icRxLink6n	Cable Receive Link 6, negative

4.5. XILINX MULTI-GIGABYTES TRANSCEIVERS

The RSL interconnection architecture is based on the Rocket-IO (or Multi-Gigabit) transceivers found in Xilinx Virtex-II Pro FPGAs. This section is intended as a quick introduction to these transceiver hardware cores placed in the FPGA fabric. The Rocket-IO transceiver consists of the Physical Media Attachment (PMA) and Physical Coding Sublayer (PCS). For more detailed information refer to the Xilinx documentation listed at the start of this document.

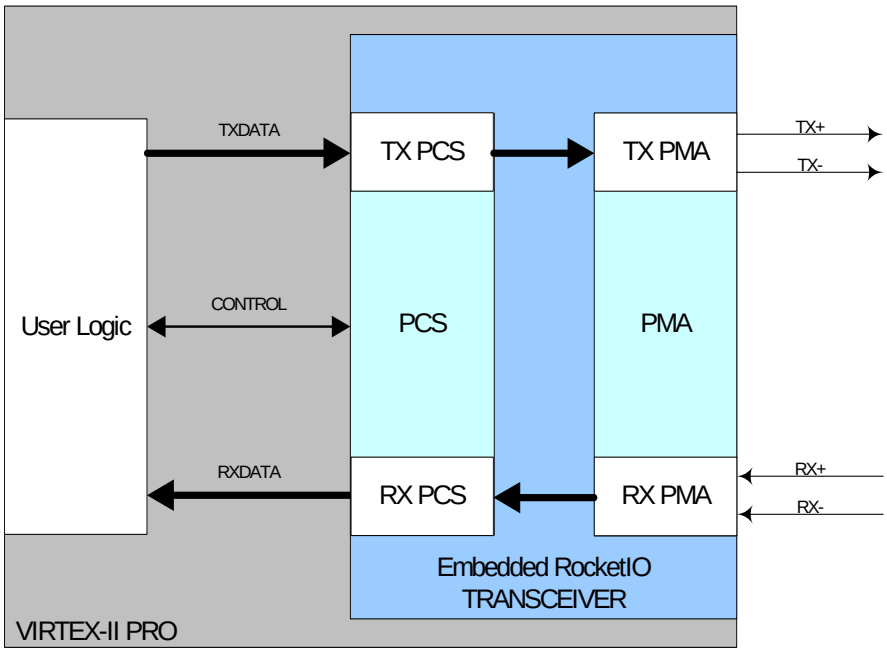


Figure 17: *Basic transceiver model*

The PMA contains the serializer/deserializer (SERDES), TX and RX buffers, clock generator, and clock recovery circuitry.

The PCS contains the 8B/10B encoder/decoder and the elastic buffer supporting channel bonding and clock correction. The PCS also handles Cyclic Redundancy Check (CRC).

The Rocket-IO transceivers are highly generic. The transceiver is configurable to implement or not various features which permit the implementation of various serial communication standards.

For this reason certain firmware and hardware limitations may be imposed on their functionality to simplify interconnection. The user should take special note of these limitations when design their own custom hardware to interface with Sundance RSL compliant hardware. A typical example of one of these limitations is operating frequency of the RSL link. Even though the Rocket-IO transceiver may operate anywhere in the range of 0.622 to 3.125 Gbits/s the RSL operating frequency is fixed at 3.125Gbit/s[1].

[1] The effective data throughput is given as 2.5Gbit/s at the start of this document under *RSL Features*. Yet the link speed is given as 3.125Gbit/s here. This 'discontinuity' is explained in the *Reference Clock* section further on in this document.

Some of the information in this section was copied straight from the Xilinx documentations and is copyrighted to Xilinx.

4.5.1. FPGA devices supported

Only the Xilinx Virtex-II Pro and Virtex-IV FPGAs support the hardware Rocket-IO core. The following table lists the supported devices and the amount of links per device:

Device	Rocket-IO Cores	Device	Rocket-IO Cores
XC2VP2	4	XC2VP40	0 or 12
XC2VP4	4	XC2VP50	0 or 16
XC2VP7	8	XC2VP70	20
XC2VP20	8	XC2VP100	0 or 20
XC2VP30	8	XC2VP125	0, 20 or 24

Table 10: *Xilinx Virtex-II pro Devices Supporting Rocket-IO*

Device	Rocket-IO Cores
XC4VPFX20	8
XC4VPFX40	12
XC4VPFX60	12 or 16
XC4VPFX100	20
XC4VPFX140	24

Table 11: *Xilinx Virtex-IV Devices Supporting Rocket-IO MGT*

It is possible to interface this core to many third party manufacturers silicon. The user should carefully compare the electrical specifications of the Xilinx Virtex-II Pro (found in the appropriate Xilinx datasheet listed in the references at the start of this document) and of the device to interface to. Additional hardware in the form of termination, level conversion or isolation might be required.

4.5.1.1. Power supply requirements

Parameter	Description	Min (V)	Typ (V)	Max (V)	Power at max data rate (mW)
PCS power supply: Vccint	VirtexII-PRO internal supply voltage relative to ground	1.425	1.5	1.575	28
PMA power supply: Vccaux	VirtexII-PRO Auxiliary supply voltage relative to ground.	2.375	2.5	2.625	48

Parameter	Description	Min (V)	Typ (mV)	Max (V)	Power at Max data rate (mW)		Conditions
VTTX	Tx Termination supply	1.8	2.5	2.625	AC 75	DC 37.5	AC or DC coupled
AVCCAUXTX	Analog Tx supply		2.5 (5%)		130		N/A

Parameter	Description	Min	Typ	Max	Conditions
Vout	Serial output differential peak to peak (TXP/TXN)	800 (mV)		1600 (mV)	Output differential voltage is programmable
Vtcm	Common mode output voltage range	1100 (mV)		2000 (mV)	Depends on AC or DC coupling, VTTX, VTRX, differential swing.

Parameter	Description	Min (V)	Typ (V)		Max (V)	Power at Max data rate (mW)		Conditions
VTRX	Rx Termination supply	1.8	AC 1.8	DC 2.5	2.625	AC 0	DC 37.5	AC or DC coupled
AVCCAUXRX	Analog Rx supply		2.5 (5%)			90		N/A

Parameter	Description	Min	Typ	Max	Conditions
Vin	Serial input differential peak to peak (RXP/RXN)	175(mV)		2000 (mV)	Output differential voltage is programmable
Vicm	Common mode input voltage range	500(mV)		2500 (mV)	Output differential voltage is programmable

4.5.1.2. Issues

- The common mode voltage of the driver and receiver is THE determinant factor for low bit error rate transmission.
- The Rocket-IO differential receiver produces the best bit-error rates when its common-mode voltage falls between 1.6V and 1.8V.
- The common mode voltage varies depending on AC or DC coupling, VTTX, VTRX and differential swing.
- When DC coupled, Xilinx recommended voltage is VTTX = VTRX = 2.5V because pre-emphasis and swing are optional at that voltage.
- Nevertheless, any voltage is valid as long as both VTRX and VTTX are the same voltage, and within the specifications shown in the previous tables.
- VTTX can be as low as 1.8 V for speeds lower than 1.22 Gb/s. It is advisable to contact an FAE if such an application needs to be developed.
- When the receiver is AC-coupled to the line, VTRX is the sole determinant of the receiver common-mode voltage, and therefore must be set to a value within this range.
- When two transceivers, both terminated with 2.5V, are DC coupled, the common-mode voltage will establish itself at around 1.7V to 1.8V.

4.5.2. Rocket-IO Features[2]

The Rocket-IO transceiver's flexible, programmable features allow a multi-gigabit serial transceiver to be easily integrated into any Virtex-II Pro design:

- Variable-speed, full-duplex transceiver, allowing 600Mbps to 3.125Gbps baud transfer rates
- Monolithic clock synthesis and clock recovery system, eliminating the need for external components
- Automatic lock-to-reference function
- Five levels of programmable serial output differential swing (800 mV to 1600 mV peak-peak), allowing compatibility with other serial system voltage levels
- Four levels of programmable pre-emphasis
- AC and DC coupling
- Programmable 50Ω/75Ω on-chip termination, eliminating the need for external termination resistors
- Serial and parallel TX-to-RX internal loop back modes for testing operability

[2] Copyrights to Xilinx

- Programmable comma detection to allow for any protocol and detection of any 10-bit character

4.5.3. The Xilinx MGT Core

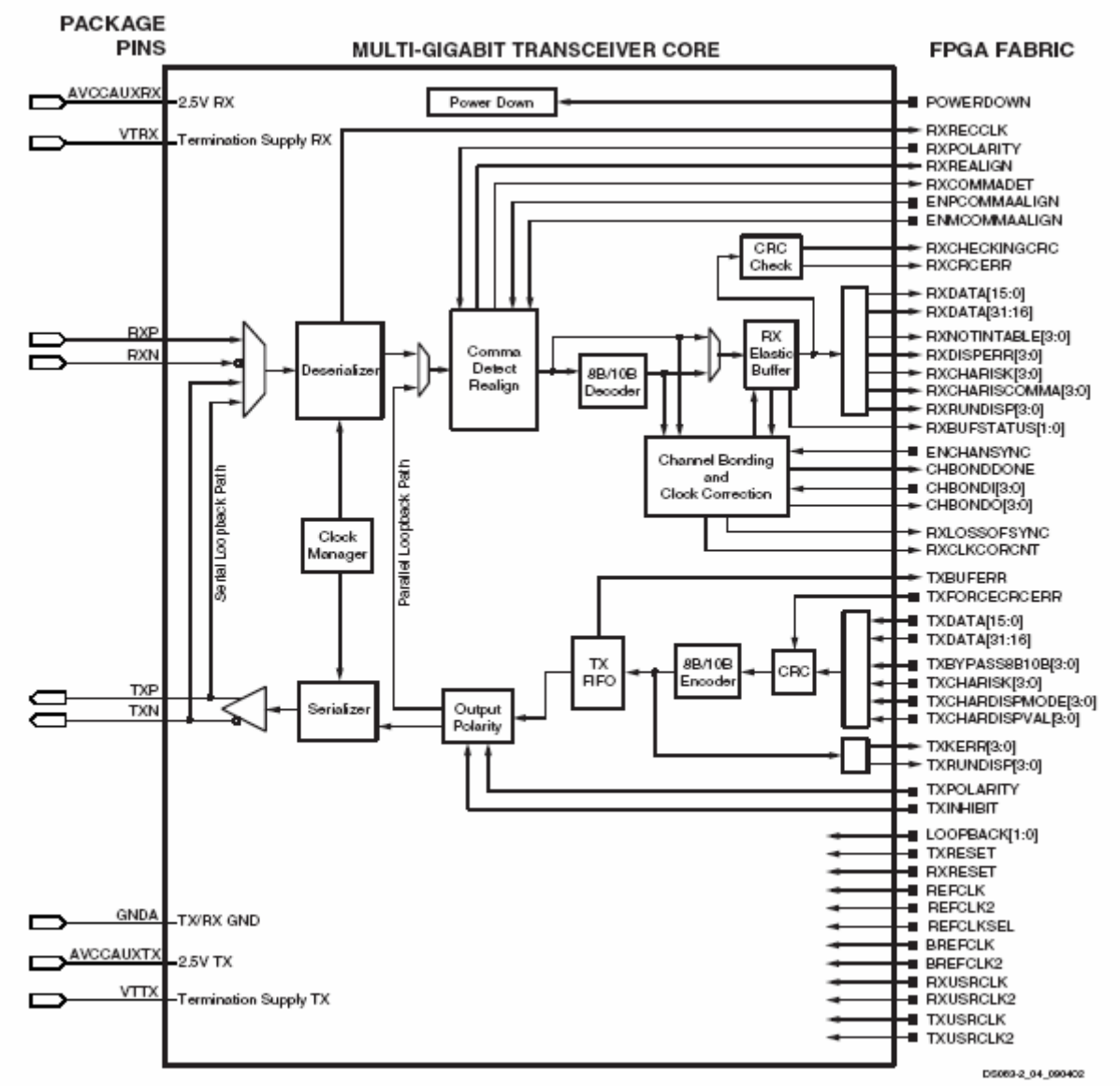


Figure 18: *The Xilinx Multi-Gigabit Transceiver Core*[3]

4.5.3.1. Clock synthesizer

A clock/data recovery circuit facilitates synchronous serial data reception. This circuit uses a fully monolithic Phase Lock Loop (PLL), which does not require any external components. The clock/data recovery circuit extracts both phase and frequency from the incoming data stream. The recovered clock is presented on output RXRECCLK at 1/20 of the serial received data rate.

[3] Copyrights to Xilinx

The gigabit transceiver multiplies the reference frequency provided on the reference clock input (REFCLK) by 20. The multiplication of the clock is achieved by using a fully monolithic PLL that does not require any external components.

4.5.3.2. Clock and Data Recovery

The clock/data recovery (CDR) circuits will lock to the reference clock automatically if the data is not present. For proper operation, the frequency of the reference clock must be within ±100ppm of the nominal frequency.

4.5.3.3. FPGA Transmit Interface

The FPGA can send either one, two, or four characters of data to the transmitter. Each character can be either 8 bits or 10 bits wide. If 8-bit data is applied, the additional inputs become control signals for the 8B/10B encoder.

4.5.3.4. 8B/10B Encoder[4]

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters that are used for Gigabit Ethernet, Fiber Channel, and Infiniband. The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10-bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

4.5.3.5. Transmit FIFO

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

4.5.3.6. Serializer

The multi-gigabit transceiver multiplies the reference frequency provided on the reference clock input (REFCLK) by 20. Clock multiplication is achieved by using a fully monolithic PLL requiring no external components. Data is converted from parallel to serial format and transmitted on the TXP and TXN differential outputs.

4.5.3.7. Transmit Termination

On-chip termination is provided at the transmitter, eliminating the need for external termination. Programmable options exist for 50Ω (default) and 75Ω termination.

---

[4] The 8B to 10B encoder ensures that the data stream is always DC balanced (same amount of 1s as 0s). This is required by the PLL to lock onto and maintain lock on the data stream. 8B/10B encoding contains the encoded data, but you can also include control characters into the data stream that is uniquely identifiable. These control characters are referred to as K characters and are used to indicate the start of a data pack, the end of a data packet and control commands for re-syncing, reset, etc…

4.5.3.8. Pre-Emphasis and Swing Control

Four selectable levels of pre-emphasis (10% [default], 20%, 25%, and 33%) are available. Optimizing this setting allows the transceiver to drive various distances of PCB or cable at the maximum baud rate. The programmable output swing control can adjust the differential output level between 400mV and 800mV in four increments of 100mV.

4.5.3.9. Deserializer

The Rocket-IO transceiver accepts serial differential data on its RXP and RXN inputs. The clock/data recovery circuit extracts the clock and retimes incoming data to this clock. It uses a fully monolithic PLL requiring no external components. The clock/data recovery circuitry extracts both phase and frequency from the incoming data stream. The recovered clock is presented on output RXRECCLK at 1/20 of the received serial data rate.

4.5.3.10. Comma Detect

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indication is given at the receiver interface. The realignment indicator is a distinct output. The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma–, both, or a unique user-defined and programmed sequence.

4.5.3.11. Receive Termination

On-chip termination is provided at the receiver, eliminating the need for external termination. The receiver includes programmable on-chip termination circuitry for 50 Ω (default) or 75Ω impedance.

4.5.3.12. 8B/10B Decoder

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both “disparity errors” and “out-of-band” errors.

4.5.3.13. Receive Buffer

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

4.5.3.14. Transmit Buffer

The transmitter buffer writes pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

4.5.3.15. CRC

The Rocket-IO transceiver CRC logic supports the 32-bit invariant CRC calculation used by Infiniband, Fiber channel, and Gigabit Ethernet.

4.5.3.16. Reference Clock

The External Reference Clock must be $1/20^{th}$ the frequency of the desired data rate of the serial link. For 3.125Gbit/s operation a reference clock of 156.25MHz is required. For a serial data rate of 2.5Bbit/s an external clock of 125MHz is required.

When data is transmitted by the RSL link it is 8B/10B encoded. The effective data throughput of the link is thus only 8/10. If the link is running at 3.125Gbit/s the effective data throughput is only 2.5Gbit/s. If the link is running at 2.5Gbit/s the effective data rate is 2Gbit/s.

4.5.3.17. RSL Specific Implementations

4.5.3.17.1. VHDL Instantiation

The RSL VHDL interface instantiates a subset of the Rocket-IO transceiver. Some of the default settings are as follows:

- FPGA Transmit Interface: Two character wide interface
- Transmit FIFO: Enabled
- 8B/10B Encoder: Enabled
- Transmit Termination: 50 Ohm
- Pre-Emphasis: 10%
- Swing Control: 400mV
- 8B/10B Decoder: Enabled
- Receive Termination: Enabled
- CRC: Enabled

4.5.3.17.2. Hardware implementation

The following hardware implementation is followed by the RSL implementation:

- External Reference Clock: 156.25MHz
- AC/DC Coupling: DC Coupling

4.6. HARDWARE INTERFACE

This section deals with the hardware implementation of the RSL interface. It is focused on Xilinx's Aurora link-layer protocol.

4.6.1. Top-level design

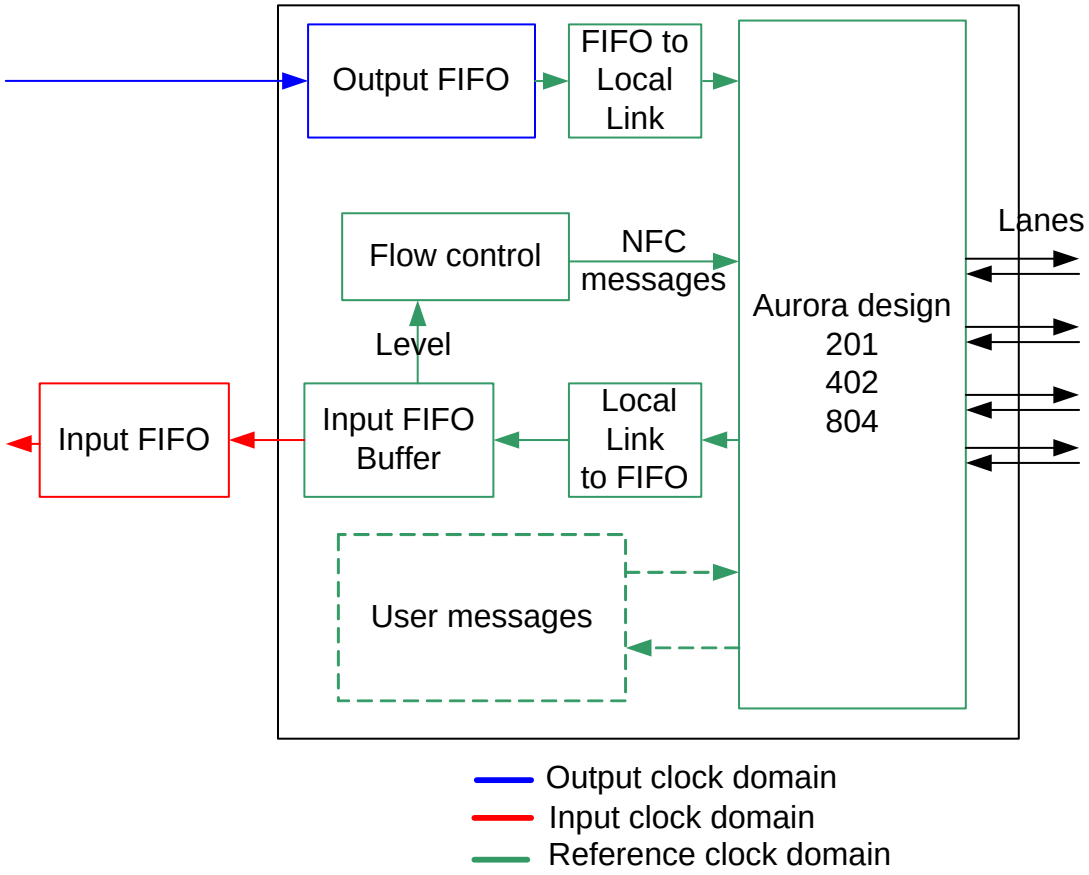


Figure 19: *Top-level design - Subsystem breakdown*

4.6.2. System states and modes

The possible parameters are:

- **Data width**

The aurora interface has the option of 2 or 4 bytes per lanes. Only selecting 2 bytes per lanes allows the maximum clock frequency to be used. So the data width can be 16, 32 or 64 bits with 1, 2 or 4 lanes respectively.

The designs names are following Xilinx's naming convention (for example 201 means a 2 bytes interface on 1 lane).

The standard data width is 32 bit for the DSP so the 16-bit interface is provided with additional data width conversion (32-to-16 in output and 16-to-32 in input).

- **Reference clock (transfer speed)**

The reference clock on both TIMs needs to be identical.

It can be from any FPGA I/O if it is below 100 MHz or needs to be from special I/Os from dedicated low jitter crystals for higher speed (100-156.25).

Each Aurora design supports one clock architecture, and should be selected according to the transfer speed required and the available on-board clock.

- **FIFO sizes**

The FIFO sizes can be chosen freely except from the one used as a buffer as its size is directly linked to the interface latency to respond to the flow control messages.

Practically the buffer size needs to be bigger than 100 words to be able to support the flow control.

- **Input and output clocks**

The design is made to allow independent read and write clocks. The speed of which will be a speed factor obviously.

- **Aurora protocol support**

The RSL do not meet the full hardware protocol specifications, as it requires AC coupling.

The eye diagram has not been verified yet. They will be once the faster designs are available.

The designs currently available are:

- 32 bit, aurora 201, 2Gb/s (with 100Mhz refclk), with 256 words buffer and independent output clock and refclk used as input clock.

- 32 bit, aurora 804, 2Gb/s (with 100Mhz refclk), with 256 words buffer and independent output clock and refclk used as input clock.

The settings used for the serial link transceiver (MGT) are the following

```
ALIGN_COMMA_MSB          => TRUE,

CHAN_BOND_MODE           => "SLAVE_1_HOP", "MASTER" or "OFF"

CHAN_BOND_ONE_SHOT       => FALSE,

CHAN_BOND_SEQ_1_1        => "00101111100",

REF_CLK_V_SEL            => 0,

CLK_COR_INSERT_IDLE_FLAG => FALSE,

CLK_COR_KEEP_IDLE        => FALSE,

CLK_COR_REPEAT_WAIT      => 8,
```

```
CLK_COR_SEQ_1_1          => "00111110111",
CLK_COR_SEQ_1_2          => "00111110111",
CLK_COR_SEQ_2_USE        => FALSE,
CLK_COR_SEQ_LEN          => 2,
CLK_CORRECT_USE          => TRUE,
COMMA_10B_MASK           => "1111111111",
MCOMMA_10B_VALUE         => "1100000101",
PCOMMA_10B_VALUE         => "0011111010",
RX_CRC_USE               => FALSE,
RX_DATA_WIDTH            => 2,
RX_LOSS_OF_SYNC_FSM      => FALSE,
RX_LOS_INVALID_INCR      => 1,
RX_LOS_THRESHOLD         => 4,
SERDES_10B               => FALSE,
TERMINATION_IMP          => 50,
TX_CRC_USE               => FALSE,
TX_DATA_WIDTH            => 2,
TX_DIFF_CTRL             => 600,
TX_PREEMPHASIS           => 1
```

4.6.3. Detailed design

4.6.3.1. Aurora

This module is generated from Xilinx's Coregen tool. To get it, after selecting Virtex-II/Pro device, select Aurora 2.1 under the serial interface design.

For more fully details, refer to the Xilinx's Aurora protocol specifications sp002.pdf

4.6.3.2. FIFO to local link

This module makes the interface between a FIFO and Xilinx local link interface.

When data is available it sets up a locallink transfer. The size of the transfer is the number of data available at that point in the FIFO.

4.6.3.2.1. Input/output data

Name	Dir	Description
clk	in	Clock input: All signals are synchronous to this clock.
rst	in	Reset input Active high
fifo_data[:]	in	Fifo data bus
fifo_rd	out	Fifo read. Reads data from the FIFO
fifo_level[:]	in	Fifo level. Indicates the amount of data in the FIFO
ll_sof_n	out	Start of Frame: Indicates the first transfer for a given frame.
ll_eof_n	out	End of Frame, indicates the last transfer for a given frame
ll_src_rdy_n	out	Source ready, signal indicating that the source logic is ready to transfer data
ll_dst_rdy_n	in	Destination ready, signal indicating that the destination logic is ready to accept data
ll_rem	out	Remainder: Indicates number of valid bytes on given transfers
ll_d[:]	out	Local link data bus

4.6.3.2.2. Local data element

This module initialises local link transfers when data is available in the FIFO. The length of the bust depends on the amount of data available in the FIFO. The maximum burst length is limited by the FIFO size.

4.6.3.2.3. Error handling

No error handling is implemented. A zero sized transfer is not possible as the size is directly used to start the transfer.

4.6.3.3. Local link to FIFO

This module makes the interface between Xilinx local link interface and a FIFO.

The local link interface from the aurora module does not use the feed back from the FIFO as this is taken care by the flow control.

4.6.3.3.1. Input/output data

Name	Dir	Description
clk	in	Clock input: All signals are synchronous to this clock.
rst	in	Reset input Active high
ll_src_rdy_n	in	Source ready, signal indicating that the source logic is ready to transfer data
ll_dst_rdy_n	out	Destination ready, signal indicating that the destination logic is ready to accept data.
ll_d[:]	in	Local link data bus
fifo_data[:]	out	Fifo data bus
fifo_wr	out	Fifo write. Writes data into the FIFO
fifo_full	in	Fifo full. Signal indicating that the FIFO is full.

4.6.3.3.2. Local data element

This module simply maps the data from local link to the FIFO and generates the write signal according to local link ready signal.

The FIFO full flag is not used as the feed back for the local link in that design.

This is the role of the flow control to make sure that no overflow occurs.

4.6.3.3.3. Error handling

No error handling is implemented.

4.6.3.4. Flow control

This module takes care of generating flow control messages in order of preventing the receiving FIFOs to overflow. It monitors the buffer size and sends messages to stop and restart the transfers.

The flow control can be switched on or off.

4.6.3.4.1. Input/output data

Name	Dir	Description
clk	in	Clock input: All signals are synchronous to this clock.
rst	in	Reset input Active high
nfc_req_n	out	A level-sensitive signal to request that an NFC data unit be sent to the channel partner
nfc_nb[:]	out	Indicates the number of pause idles to be sent as part of an NFC data unit
nfc_ack_n	in	Asserted when the interface accepts an NFC request
use_nfc	in	Signal used to enable or disable flow control messages
min_buffer_space[:]	in	Space below which nfc will be transferred. Typically is the maximum number of words received before nfc stops the transfer. This is related to the latency of the interface.
buffer_space[:]	in	Indicates the number of spaces left in the FIFO.

4.6.3.4.2. Local data element

A state machine takes care of controlling the data flow.

4.6.3.4.3. Error handling

No error handling is implemented. The flow control can be switched off.

4.6.3.4.4. Logic flow

State machine diagram

4.6.3.5. Input/output FIFO

These modules are generic input and output FIFOs.

4.6.3.5.1. Input/output data

Name	Dir	Description
rst	in	Reset signal active high
rd_clk	in	Read clock
rd_en	in	Read enable. A data is read out of the FIFO at each rising edge when this signal is high.
rd_data[:]	out	Read data bus. According to the FIFO mode selected the FIFO behaves as a fall through type or not.
rd_level[:]	out	Number of words available in the FIFO. Number shown is always valid. Initial value of 0.
rd_empty	in	FIFO empty signal. This shows if the FIFO contains at least one data. This signal is showing if there is data before the level is updated.
wr_clk	in	Write clock. It can be independent of rd_clk or not.
wr_en		Write enable. A data is written into the FIFO at each rising edge when this signal is high.
wr_data[:]	in	Write data bus. Data to be written in the FIFO.
wr_level[:]	out	Number of space available in the FIFO. Number shown is always valid. Initial value shows the maximum number of words the FIFO can contain.
wr_full	in	FIFO full signal. This shows if the FIFO has at least one space left for data. This signal is showing if there is space before the level is updated.

The other parameters are:

- FIFO depth from the number of address bits
- Data size
- Fall through type or not
- Use blockram or distributed logic
- Independent read and write clock or not. If the clocks are independent then the signals named wr_… are synchronised on wr_clk and the signal named rd_… are synchronised on rd_clk.

4.6.3.5.2. Local data element

Logic generates read and write pointers and levels.

It can be made of block of RAM or distributed logic, and support independent input and out put clocks or not.

4.6.3.5.3. Error handling

No error handling is implemented.

4.6.3.6. Clocking scheme

The basis of the clocking scheme is that the reference clock has to be provided directly from the input pad whereas the user clock can be buffered and match lane frequency / 20.

The Xilinx Rocket IO transceiver User guide section "clocking" in chapter 3 (page 41) provides information regarding the reference clock, nevertheless, Sundance RSL standard follows the following guidelines.

4.6.3.7. Performance

The reference clocks for the protocols supported by the RocketIO are the following:

Mode	Reference clock frequency to SERDES (MHz)	IO bit rate (Gb/s)
Fiber Channel	53.125	1.06
	106.25	2.12
Gigabit Ethernet	125	1.25
	250	2.5
	156.25	3.125
Infiniband	250	2.5
Aurora	Custom	0.600-3.125
Custom	Custom	0.600-3.125

Table 12: *Reference clock for Rocket-IO standard applications*

The maximum allowable jitter on the reference clock input to the SERDES scales inversely with speed:

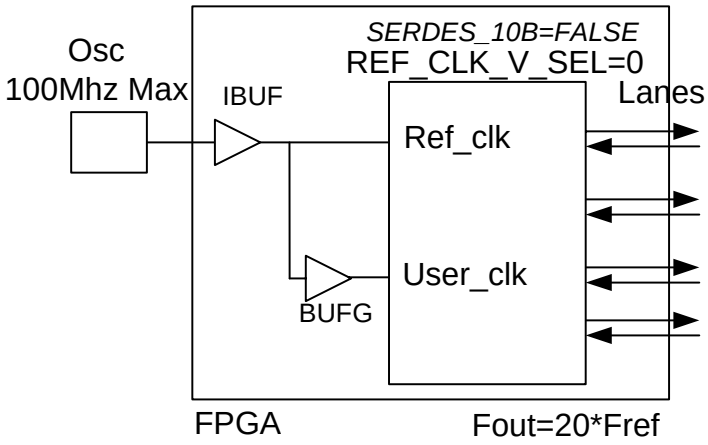
Speed	Reference clock Max jitter
3.125	40ps
2.500	50ps
1.060	120ps
0.622 Gbps	201ps

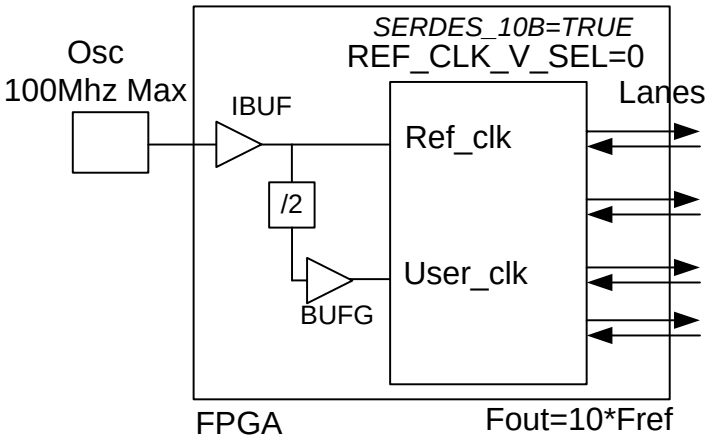
Table 13: *Maximum jitter*

- Because of dedicated routing to reduce jitter inside the FPGA, the reference clock for the RocketIO MUST be routed onto BREFCLK or BREFCLK2 pin of the FPGA to meet the RSL specification of 2.5Gb/s on a serial link.
- When implementing specific protocols with lower serial speed than 2.5Gb/s, REFCLK or REFCLK2 can be used for the reference clock input.
- REFCLK is required for both transmission and RECEPTION. This implies that the transmitter and receiver of the same transceiver MUST operate at the same rate.
- REFCLK should be routed through an IBUFG only to minimise jitter.
- Routing of REFCLK through a BUFG may introduce too much jitter. The only reason why going through a BUFG is when driving 2 or more MGTs on opposite side of the FPGA. In this case, the ideal solution is to bring the REFCLK in through two separate input pins. (BREFCLK and BREFCLK2 for 2.5Gb/s or higher serial speed)
- Sundance RSL standard specifies that a module can support more than one protocol operating on the same RocketIO at different points in time. Achieving such a scheme implies that the REFCLK input can be changed dynamically. (i.e, once the board has been powered up, the REFCLK must be changed to the right frequency for the new protocol to operate.). The RocketIO User Guide includes an example that describes how to set this up properly. The issue being that the transceiver's CDR unit will lose lock when the REFCLK changes; consequently, the appropriate synchronization process must be executed.
- Modules that support more than one protocol can use a clock synthesiser to generate the appropriate clock frequency. The ICS clock synthesizer 8442, should be used to generate any frequencies between 31.25 MHz up to 700MHz with a jitter lower than 40ps required for the Rocket I/O transceiver REFCLK input. A 25MHz crystal oscillator can be used as the reference crystal for the ICS8442.

4.6.3.7.1. Using Refclk

For clocks of 100Mhz or below the following clock architectures can be followed:

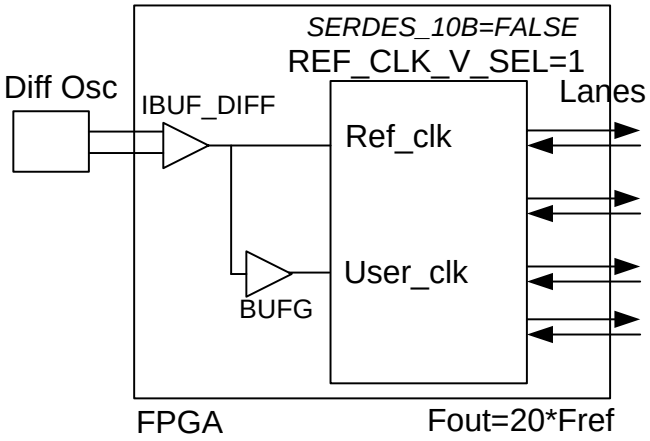


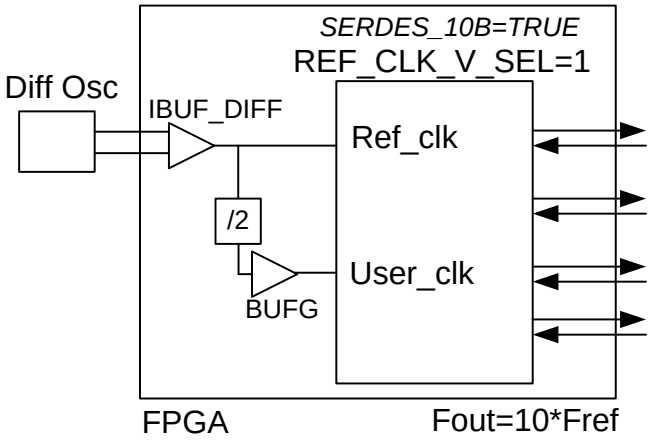


The *SERDES_10B* parameter is set in the user constraint file (ucf).

4.6.3.7.2. Using Brefclk

The following clock architectures can be followed:





The *SERDES_10B* parameter is set in the user constraints file (ucf)

4.6.3.8. Channel bonding techniques

Therefore, Sundance's systems do NOT need to support any higher IO bit rates than 2.5Gb/s and if higher throughput is required, then channel bonding techniques should be considered.

Channel bonding techniques are detailed in Xilinx Rocket IO transceiver User guide section "Channel Bonding" in Chapter 2 (Page 81).

Up to 16 transceivers (the maximum available in a 2VP50) can be bonded. The key timing issue is that the total routing delay from the CHBONDO of one transceiver to the CHBONDI of the next transceiver must be less than (RXUSERCLK period - {CHBONDO clk-to-out + CHBONDI setup + RXUSERCLK skew).

At this time, it is not confirmed that this requirement can be met in a 2VP50. Aside from the CHBONDO-CHBONDI delay requirement, no data rate limitations exist.

4.7. HARDWARE SPECIFICS

4.7.1. RSL Printed Circuit Board

Layout and bypassing guidelines are included in the Xilinx Rocket IO transceiver User guide section "PCB Design Requirements" in Chapter 3 (page 111).

Since bypassing requirements are easily determined because of the predictable nature of the Rocket-IO power consumption, a pre-designed solution is provided.

4.7.2. RSL transmission media

The transmission media must meet the above requirements in terms of speed and signal integrity.

4.7.2.1. The Driver, driver termination

The driver transmits differential signals, TXP pin and TXN pin.

This feature operates at a nominal supply voltage of 2.5 V DC.

Differential switching is performed at the crossing of the two complementary signals.

Therefore, no separate reference level is needed.

On-chip termination is provided at the transmitter, eliminating the need for external termination. Programmable options exist for 50Ω (default) and 75Ω termination.

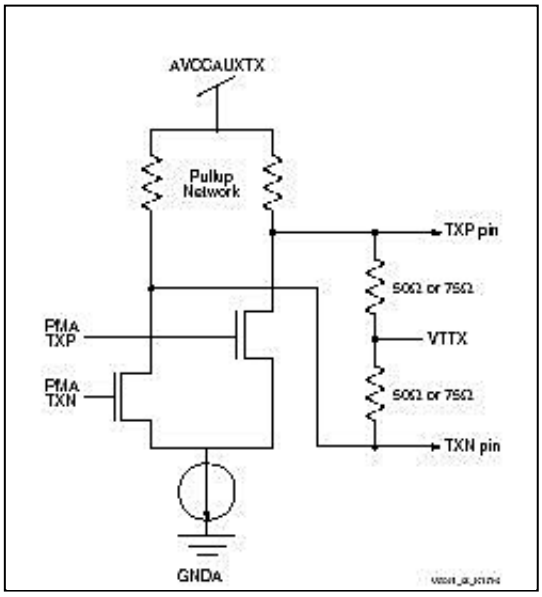


Figure 20: *MGT Differential Driver*

4.7.2.2. The receiver, receiver termination

The receiver receives on differential signals, RXP pin and RXN pin.

All input data must be nominally biased to a common mode voltage of 0.5V –2.5V, or AC coupled.

Differential switching is performed at the crossing of the two complementary signals.

Therefore, no separate reference level is needed.

The receiver includes programmable on-chip termination circuitry for 50Ω (default) or 75Ω impedance.

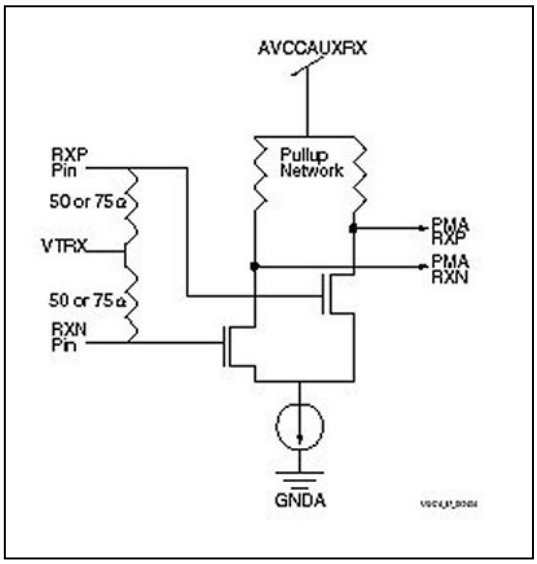


Figure 21: *MGT differential Receiver*

4.7.3. Power filtering capacitor

Power filtering capacitors that are not available internally need to be mounted externally on the PCB.

The capacitors are 0.22uF.

- The 0.22uF capacitors must be placed within 1cm of the pins they are connected to for devices that do not contain filtering capacitors in their package.
- External ferrite beads must be used in all cases since ferrite beads are not included inside the package in any device.
- Placing external capacitors on a package that has internal capacitors will not degrade performance.

4.7.4. Coupling

4.7.4.1. AC-coupling

If a design requires AC coupling, capacitors must be supplied externally. But, the Xilinx Rocket IO transceiver User guide only gives recommended AC-coupling capacitors for 3.125 Gbps 8B/10B encoded data.

The following application note from Maxim describes a methodology for choosing AC coupling capacitors http://pdfserv.maxim-ic.com/en/an/hfan11v2.pdf

C = 7.8 * Ncid * Tb / R

Where:

- C is the capacitance in nanofarads
- Ncid is the number of consecutive identical bits (the maximum run length of the data). When 8B/10B encoding used Ncid = 0
- Tb = the bit time in nanoseconds
- R = the resistance of the line.

Another consideration is the Pattern Dependent Jitter (PDJ). The value calculated from the above equation is usually too small and results in higher PDJ. The equations provided for PDJ in the Application Note in conjunction with the above equation will yield a good AC coupling capacitor value.

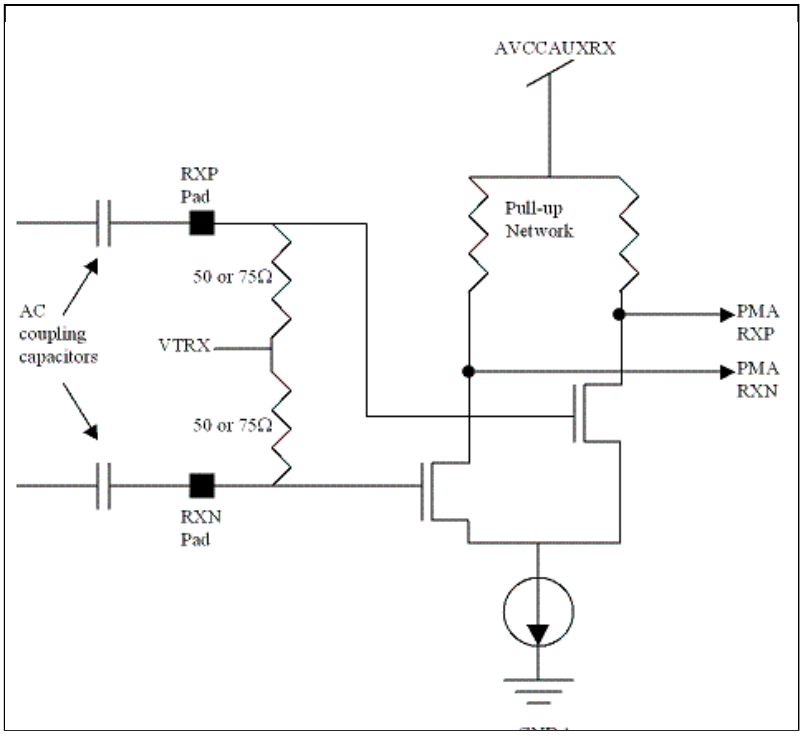


Figure 22: *AC coupled Rocket-IO receiver*

Concerning restrictions due to AC-DC coupling, in Xilinx Rocket IO transceiver User guide section "PCB Design Requirements" in Chapter 3, table 3.8 (p.119), it is recommended to provide 1.6-1.8 V for VTRX in AC coupled configuration.

Nevertheless, when AC coupling needs to be used, it is NOT necessary to provide 1.8V for the VTRX supply with a SEPARATE regulator. Due to the very small current draw of the VTRX pins, you can use the following circuit to derive 1.78V from the 2.5V analog supplies for the VTRX pins on the Virtex-II Pro device:

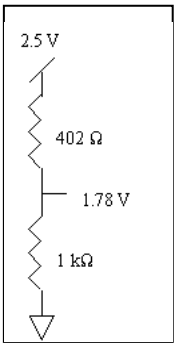


Figure 23: *Voltage divider*

One voltage divider is required for each VTRX pin in AC-coupled configuration.

The VTRX and VTTX voltages for different coupling environments are summarized in the following table:

Coupling	**VTRX**	**VTTX**
AC	1.6V to 1.8V	2.5V ±5%
DC	2.5V ±5%	2.5V ±5%

Recommended VTRX and VTTX for AC- and DC-Coupled Environments

Supporting AC coupling involves on all modules:

- Using the solution above
- Using a dedicated voltage regulator
- Any of these 2 solutions increases board complexity and components count
- Defining where the AC-coupled lines should be on the RSL connectors and FPGA
- Defining how many AC coupled lines according to the FPGA.

4.7.5. Speed grade and clock speed

The optimum RSL solution for Sundance is lies in the choice of the right RSL FPGA.

With –5 FPGA the limit is at 2GB/s (100MHz clock) the clock can be provided from any I/O.

With –6[5] and –7 the limit is 3.125GB/s (156.125MHz clock) provided on top and bottom reference clocks.

[5] A –6 speed grade FPGA in FF package guaranties to meet the speed requirements and optimises board space by saving termination resistors and power filtering capacitors.

5. QUALIFICATION REQUIREMENTS

5.1. QUALIFICATION TESTS OF THE FIRMWARE

The tests described will test the following hardware components:

- RSL link
- RSL Interface

5.1.1. RSL link test

This test verifies that the RSL Link works. The RSL Link is provided to interface two DSPs using RSL.

5.1.1.1. Test layout

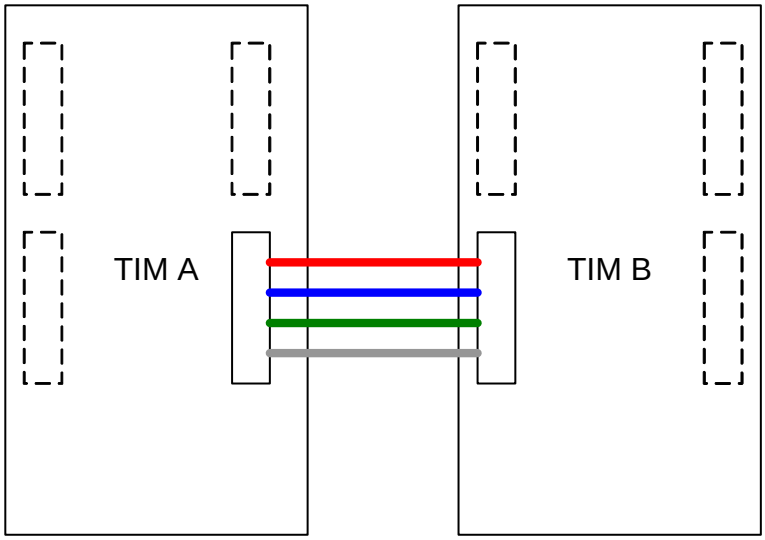


Figure 24: *Test layout for the RSL link*

The two DSP are sending random data between each other. The test verifies data integrity and flow control.

5.1.1.2. Test preparation

Connect 2 SMT395 together using RSL cable.

5.1.1.3. Test performed

Run the 3L app called rsl loopback random 2x395 and leave it to run for few minutes.

5.1.1.4. Results format

The test will display any error found and stop. If it hangs it should be considered as failed.

5.1.2. RSL interface test

This test verifies that the RSL interface works. The RSL interface is provided to interface two FPGAs using RSL.

5.1.2.1. Test layout

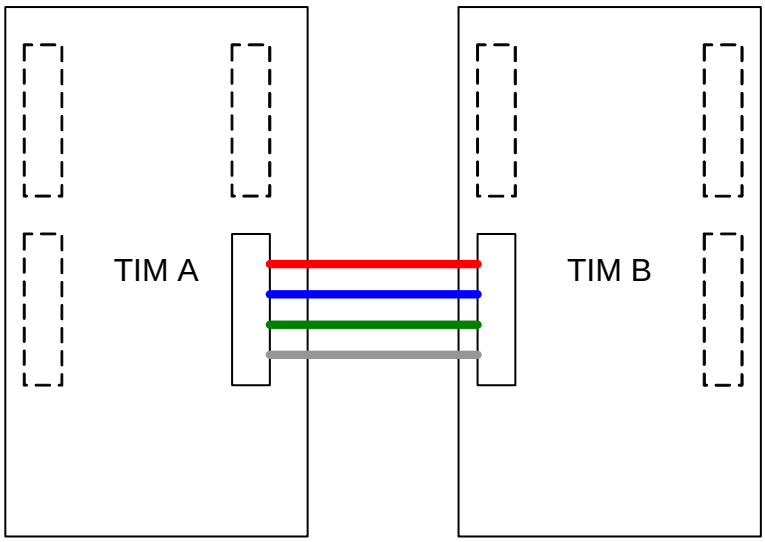


Figure 25: *Test layout for the RSL interface*

The DSP is sending and receiving back random data on its RSL. The firmware loops back all RSLs on themselves.

The format and speed of the RSL need to be matched between the two TIMs.

5.1.2.2. Test preparation

1. Define the RSL test speed you want to test (Ftest in Mb/s), It is selected according to the reference clock available to your TIM and the ones on the SMT395 available.

2. Choose the SMT395 that can run at that speed. The choice is made according to the oscillators frequency available (Fosc in MB/s). The ratio can be Ftest=Fosc*20 or Ftest=Fosc*10 (div2 option). Typically on-board refclk of 100MHz can give 1Gb/s or 2Gb/s, 125MHz can give 1.25Gb/s (not used) or 2.5Gb/s and 56.125 can give 561.25Mb/s(not used) and 1.065Gb/s. A standard 395 can provide 1Gb/s, 2Gb/s and 2.5Gb/s

3. Choose the rsl pins being tested (201, 402, 804).

4. Use flexpcb cables.

On the SMT310Q carrier board:

- Plug a SMT395 on the first TIM site.
- Plug the TIM under test on the second TIM site.
- Connect RSL cables between TIMs. The test is independent.

5.1.2.3. Test performed

Program the SMT395 with the firmware providing the right RSL frequency using the SMT6001. (Choose from $/SMT395/Firmware/rsl_test_pattern)

The software downloads an idle key first on comport 0 so if an FPGA tim is used it should be programmed with the corresponding loopback firmware before running the test. The test should be changed if additional settings have to be programmed before running the tset.

5.1.2.3.1. Toggling data test

Program the SMT395 using the SMT6001 with an embedded application that tests the RSL.
($/SMT395/Firmware/rsl_test_pattern/software/loopback_single_connector_toggle)

It tests the maximum toggling rate for the selected frequency. The led should be toggling on the SMT395 and stop if any error occurs.

The connector can be looped back on the SMT395 to see the working pattern.

5.1.2.3.2. Random data test

Program the SMT395 using the SMT6001 with an embedded application that tests the RSL.
($/SMT395/Firmware/rsl_test_pattern/software/loopback_single_connector_random)

It tests the random data pattern at the selected frequency. The led should be toggling on the SMT395 and stop if any error occurs.

The connector can be looped back on the SMT395 to see the working pattern.

5.1.2.4. Results format

The tests need to be left running for a few hours and eye pattern would be needed to verify the margin of error.

5.2. ERROR DETECTION

Refer to Xilinx's specifications.

Extracted from TechXclusives (Bit error rate, 03/03/2004) by Austin Lesea (principal engineer at Xilinx San Jose):

"To be obsessed about BER is foolish. To use BER alone as a measure is dangerous, because you are dealing with a stochastic process that is affected by many errors and is based on many assumptions. In the absence of other results, BER tells you practically nothing."

http://www.xilinx.com/bvdocs/appnotes/xapp762.pdf

http://www.xilinx.com/bvdocs/userguides/ug137.pdf

6. PCB DESIGN: REVIEW CHECK LIST

The aim of this section is to make a list of the rules required for a successful RSL design and to end up with a checklist for designer and gather the information for future use.
It does not substitute to Xilinx's recommendation and is only to be used as a guideline for checking a design. The idea is that by checking for all the following requirements in a design most of the pitfalls can be avoided and a high-speed reliable transfer can be reached. It should give a basis of comparison between designs as well.
Most of the information is already provided in Xilinx's documentation (ug024 RocketIO Transceiver User Guide and ug076 Virtex-4 RocketIO Multi-Gigabit Transceiver) and the RSL technical specifications. This document should be read in conjunction of these documents as it often refers to them.

6.1. SCHEMATICS

6.1.1. Powering circuitry

6.1.1.1. Regulator part

Check that the part belongs to the recommended one.

W*e are using LT1963EST-2.5 for V2Pro. One per 4 lanes.*

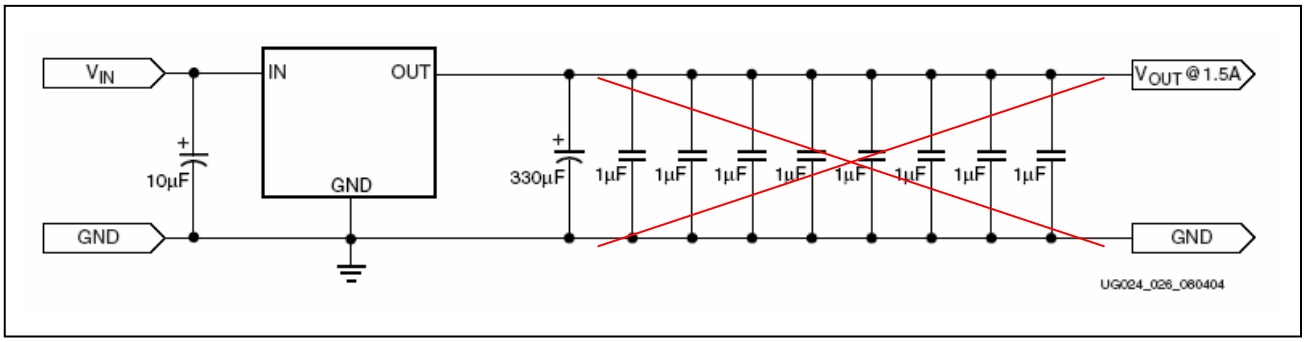
6.1.1.2. Input and output decoupling

Check Xilinx's recommendations.

Input decoupling should be 10uF capacitor.

Output decoupling should be 330uF capacitor + eight 1uF.

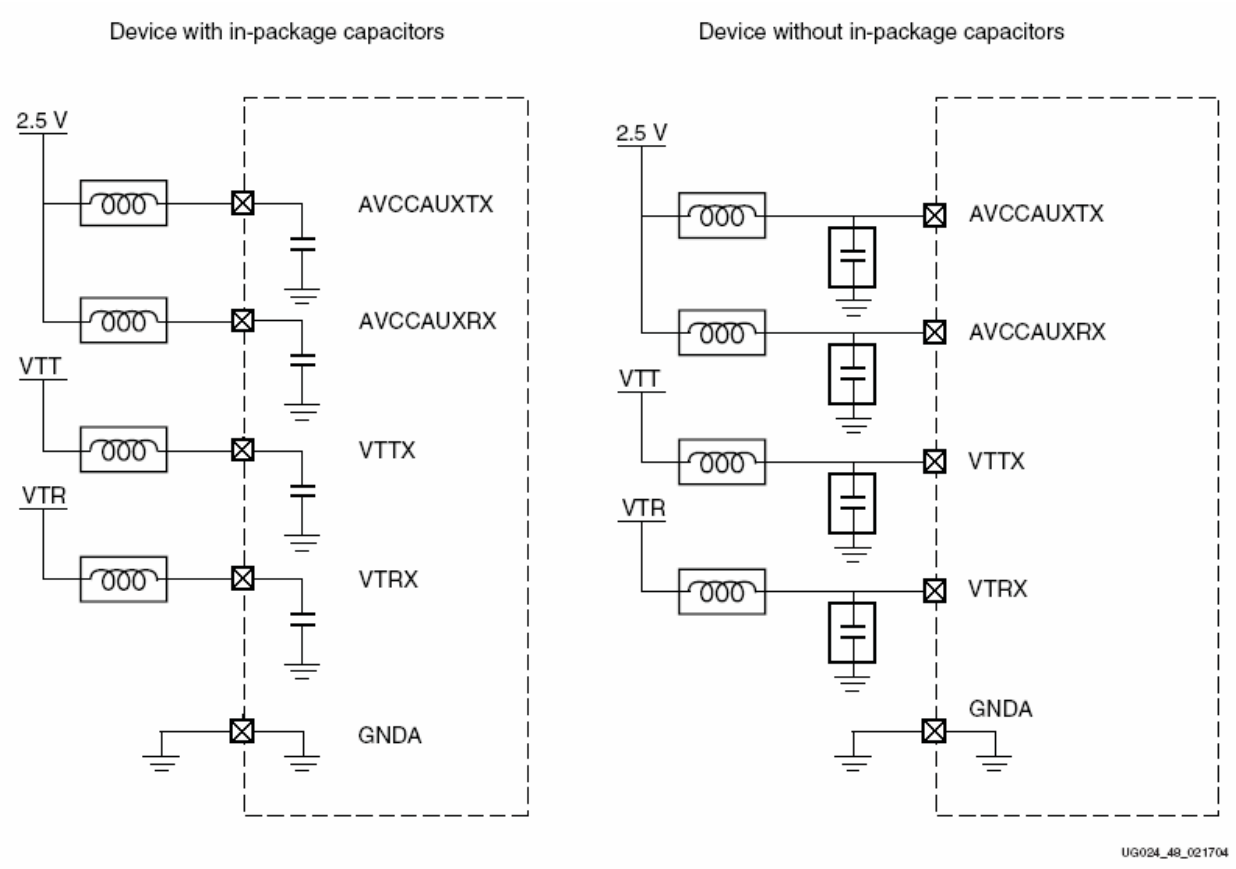
We don't fit the eight 1uF ones due to space restriction.



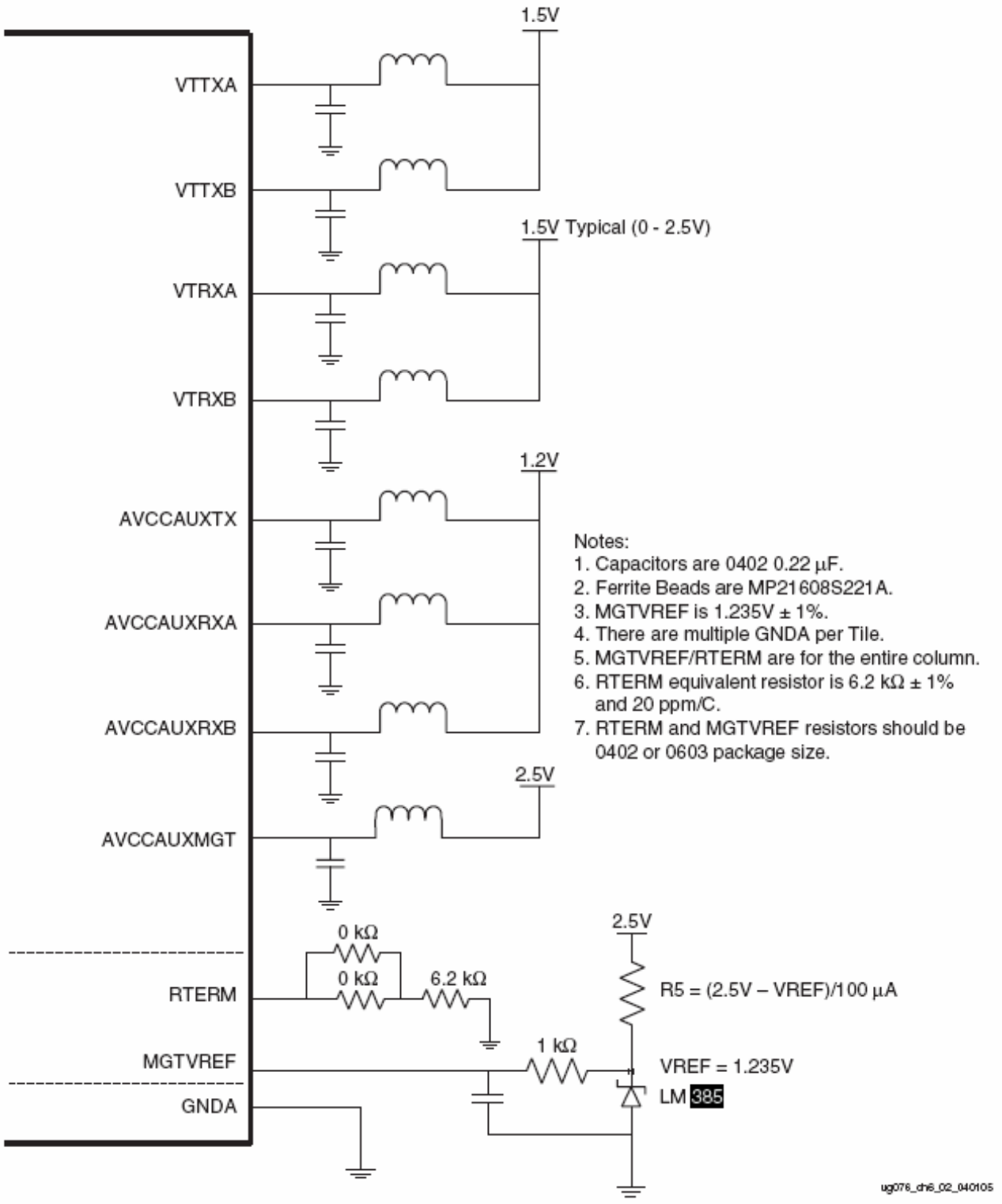
The filtering is made of a network of inductor and capacitor. Some might be internal to the chip. Check the datasheet to see if the capacitors are internal.

The capacitors must be of value 0.22 µF in an 0603 (EIA) SMT package of X7R or X5R dielectric material at 15% tolerance, rated to at least 5 V. The ferrite bead is either the Murata BLM18AG102SN1 or the Murata BLM15A6102SNID.

We use 220nF (>16V) 5% 0603 Ceramic capacitors and BLM18AG102SN1-0603 inductors.


Device with in-package capacitors
Device without in-package capacitors
2.5 V
AVCCAUXTX
AVCCAUXRX
VTT
VTTX
VTR
VTRX
GNDA
UG024_48_021704

For virtex4


1.5V
VTTXA
VTTXB
1.5V Typical (0 - 2.5V)
VTRXA
VTRXB
1.2V
AVCCAUXTX
AVCCAUXRXA
AVCCAUXRXB
2.5V
AVCCAUXMGT
Notes:
1. Capacitors are 0402 0.22 µF.
2. Ferrite Beads are MP21608S221A.
3. MGTVREF is 1.235V ± 1%.
4. There are multiple GNDA per Tile.
5. MGTVREF/RTERM are for the entire column.
6. RTERM equivalent resistor is 6.2 kΩ ± 1% and 20 ppm/C.
7. RTERM and MGTVREF resistors should be 0402 or 0603 package size.
0 kΩ
0 kΩ
6.2 kΩ
RTERM
2.5V
R5 = (2.5V – VREF)/100 µA
1 kΩ
MGTVREF
VREF = 1.235V
LM 385
GNDA
ug076_ch6_02_040105

6.1.1.4. Unused RSL power supply and filtering

Unused RSL always have to be powered but filtering is not required for V2PRO.

V4 do require filtering in some cases (Cf Xilinx record Number: 20816)

6.1.1.5. Common-mode voltage selection

The common mode voltage (1.8V) is set according to the VTRX. See table below.

A voltage divider is to be added to allow control over VTRX for AC coupling or in case V4 require it.

We only use DC coupling but a voltage divider is used so that VTRX can be adjusted for AC coupled environment (and maybe V4 compatibility) . (Cf Xilinx record Number: 17089)

Coupling	V_{TRX}	V_{TTX}
AC	1.6V to 1.8V	2.5V ±5%
DC	2.5V ±5%(1)	2.5V ±5%(1)

6.1.1.6. Oscillator

Check that the part belongs to the recommended one.

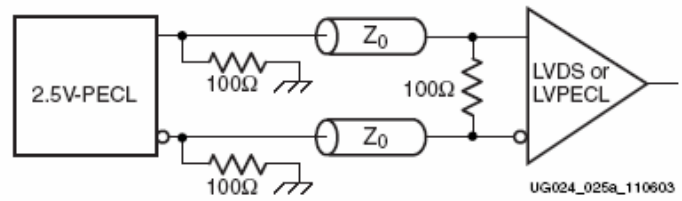
Check power supply requirement.

W*e are using EG-2121CA-2.5-PECL for V2Pro.*

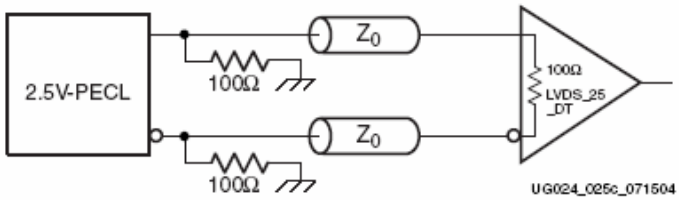
6.1.1.7. Standard and termination techniques

The termination can be internal or external.

LVPECL

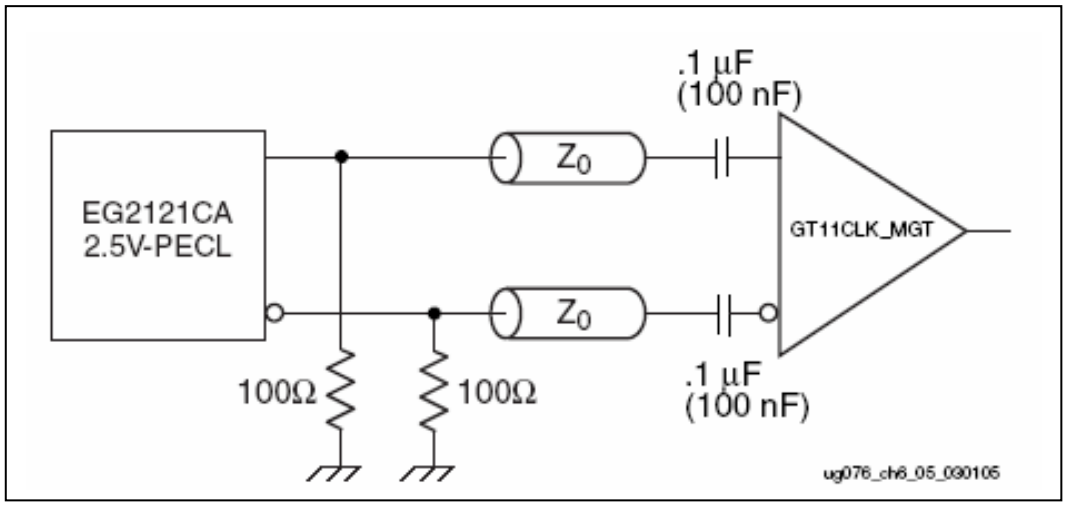


LVPECL Reference Clock Oscillator Interface

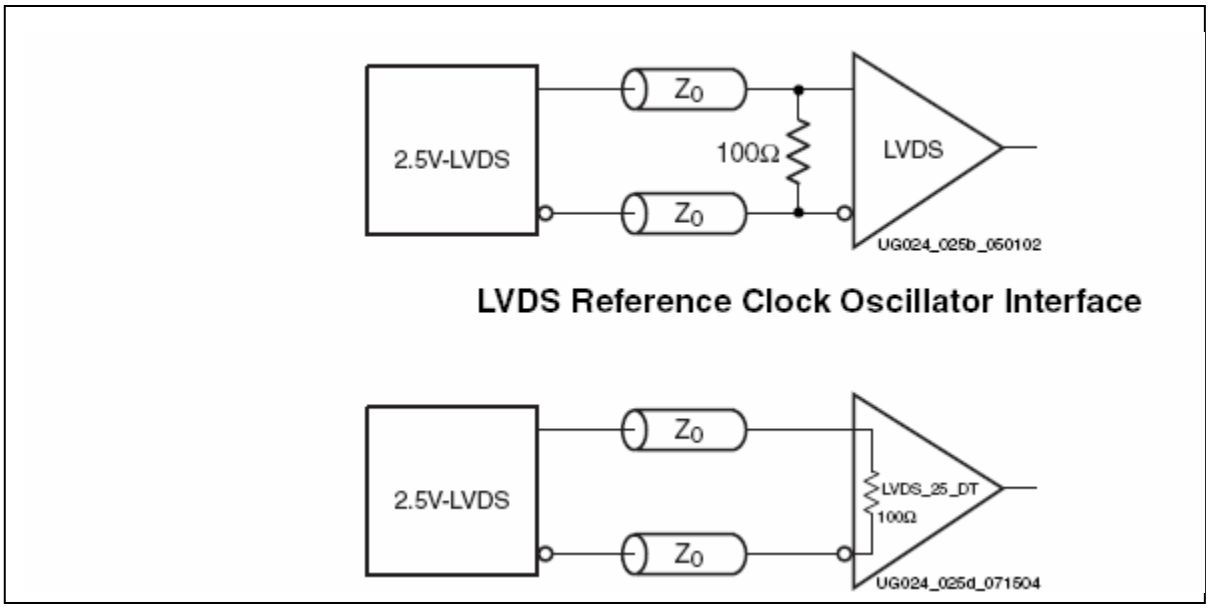


LVPECL Reference Clock Oscillator Interface (On-Chip Termination)

The recommendations for Virtex 4 are as follows



LVDS



6.1.1.8. Internal termination requirements

Always specify when internal terminations are to be used and check that the specific requirements can be met (For example Resistors connected to VRP and VRN pins and VCCO set to correct level).

6.1.1.9. FPGA clock pinout and polarity

Check the FPGA pinout. Under 100MHz single-ended clock can be used. If differential clocks are used check that they are connected to the dedicated clocks inputs and the clock should be provided to each side of the FPGA. Typically it would be BREFCLK_TOP and BREFCLK_BOTTOM (BREFCLK2_TOP and BREFCLK2_BOTTOM are also an option).

Top	BREFCLK	P	GCLK4S	Bottom	BREFCLK	P	GCLK6P
		N	GCLK5P			N	GCLK7S
	BREFCLK2	P	GCLK2S		BREFCLK2	P	GCLK0P
		N	GCLK3P			N	GCLK1S

6.1.1.10. Clock buffering

Clock buffering is used for clock tree. Check standard compatibility and termination techniques as mentioned above.

We use MC100LVEP11DT as a 1:2 buffer.

6.1.2. Connector

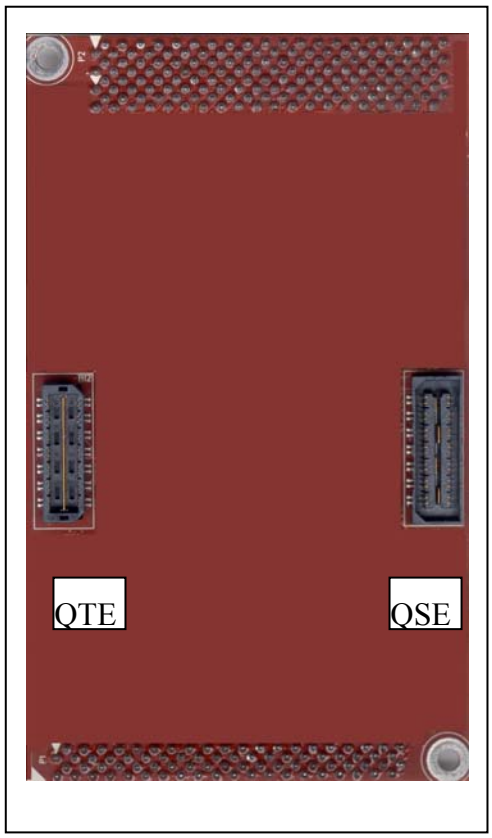
6.1.2.1. Connector types

Check connector parts and types.

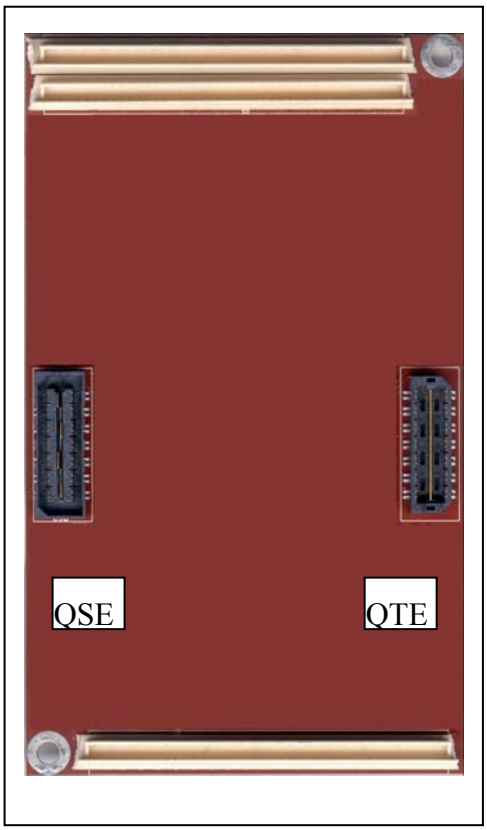
The RSL specification describes the parts to be used.

Typically QSE-014-01-F-D-DP-A and QTE-014-01-F-D-DP-A.

Pictures of top and bottom TIM show the connectors and their orientation.



Top



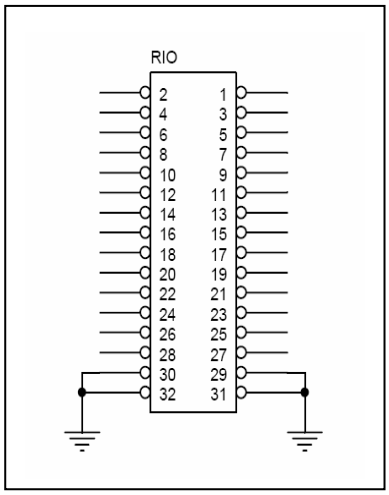
Bottom

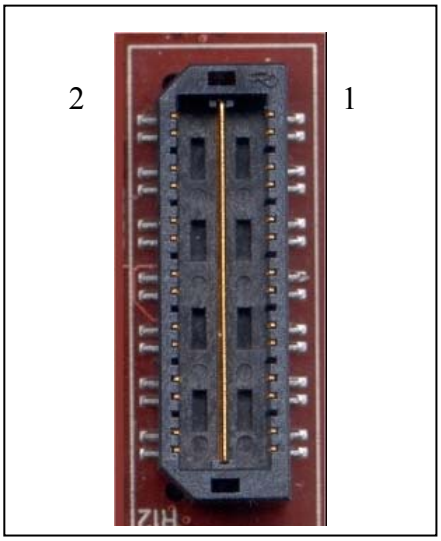
6.1.2.2. Connector symbol

Check matching between connector and FPGA pairs and polarity.

6.1.2.2.1. QTE top connector

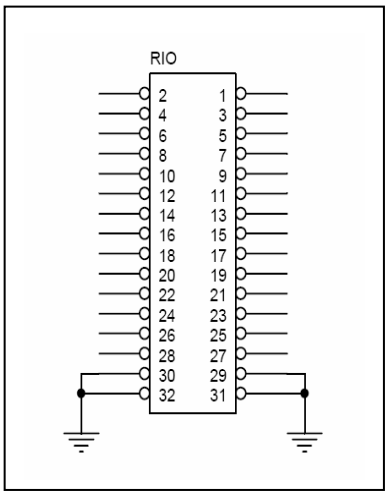
2	RX0P	TX0P	1
4	RX0N	TX0N	3
6	RX1P	TX1P	5
8	RX1N	TX1N	7
10	RX2P	TX2P	9
12	RX2N	TX2N	11
14	RX3P	TX3P	13
16	RX3N	TX3N	15
18	RX4P	TX4P	17
20	RX4N	TX4N	19
22	RX5P	TX5P	21
24	RX5N	TX5N	23
26	RX6P	TX6P	25
28	RX6N	TX6N	27

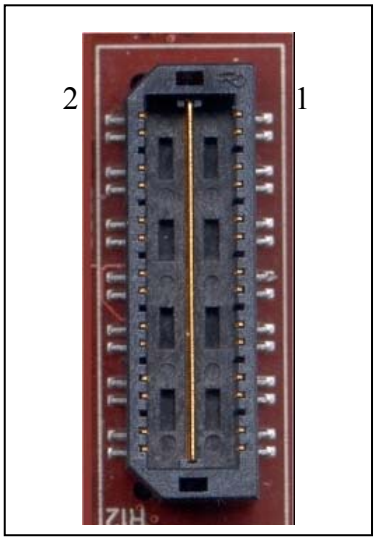




6.1.2.2.2. QTE bottom connector

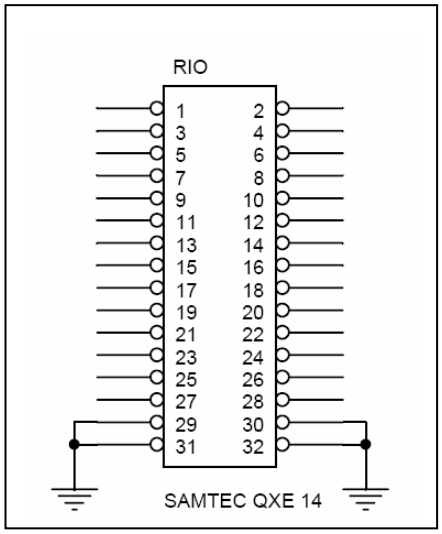
2	TX0P	RX0P	1
4	TX0N	RX0N	3
6	TX1P	RX1P	5
8	TX1N	RX1N	7
10	TX2P	RX2P	9
12	TX2N	RX2N	11
14	TX3P	RX3P	13
16	TX3N	RX3N	15
18	TX4P	RX4P	17
20	TX4N	RX4N	19
22	TX5P	RX5P	21
24	TX5N	RX5N	23
26	TX6P	RX6P	25
28	TX6N	RX6N	27

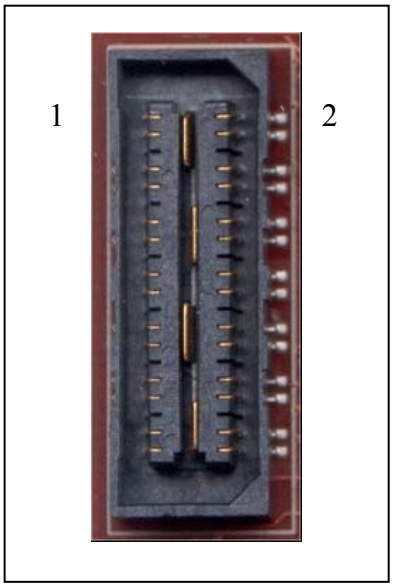




6.1.2.2.3. QSE top connector

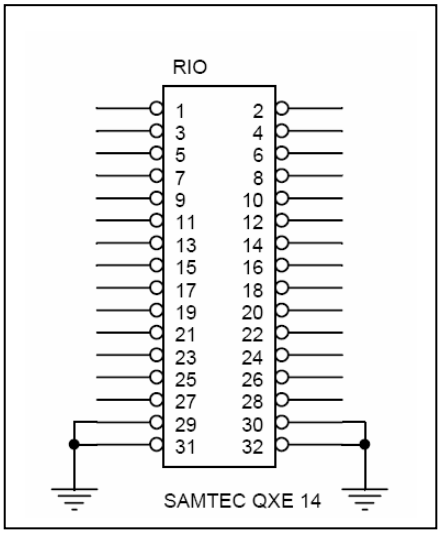
1	RX0P	TX0P	2
3	RX0N	TX0N	4
5	RX1P	TX1P	6
7	RX1N	TX1N	8
9	RX2P	TX2P	10
11	RX2N	TX2N	12
13	RX3P	TX3P	14
15	RX3N	TX3N	16
17	RX4P	TX4P	18
19	RX4N	TX4N	20
21	RX5P	TX5P	22
23	RX5N	TX5N	24
25	RX6P	TX6P	26
27	RX6N	TX6N	28

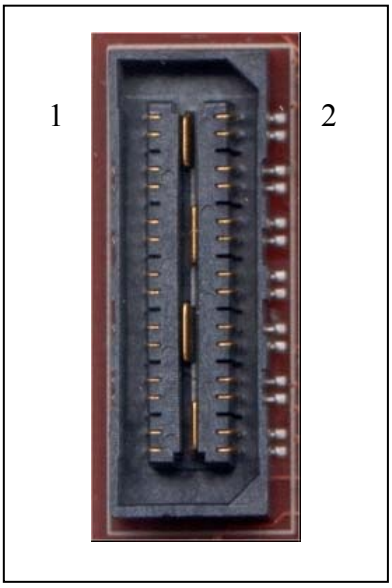




6.1.2.2.4. QSE Bottom connector

1	TX0P	RX0P	2
3	TX0N	RX0N	4
5	TX1P	RX1P	6
7	TX1N	RX1N	8
9	TX2P	RX2P	10
11	TX2N	RX2N	12
13	TX3P	RX3P	14
15	TX3N	RX3N	16
17	TX4P	RX4P	18
19	TX4N	RX4N	20
21	TX5P	RX5P	22
23	TX5N	RX5N	24
25	TX6P	RX6P	26
27	TX6N	RX6N	28





6.1.3. Differential pairs

6.1.3.1. Lane mapping on connectors

The mapping of the RSL links onto each connector depends on the number of lanes existing on the FPGA.

It has been decided that the lane should be routed to one connector only and that multiple connectors on the same lanes was not a viable solution.

The connector mapping should be

1. Four lanes per connector consisting of adjacent MGTs (Cf Summary table defined below includes MGT number).
2. First add 4 lanes to each of the top connectors.
3. Then add 4 lanes to each of the bottom connectors.
4. Top and bottom connector lane should be from the same FPGA side.
5. If additional lanes are available then they should be connected to the top connectors, then the bottom one.

6.1.3.2. Pair and polarity mapping

Check that FPGA TXz + pins are connected to connector TXy + pins.

Check that FPGA TXz - pins are connected to connector TXy - pins.

Check that FPGA RXz + pins are connected to connector RXy + pins.

Check that FPGA RXz + pins are connected to connector RXy + pins.

The polarity of the pins can be inverted for routing purposes but this has to be kept as a last resource.

6.1.3.3. Mapping summary

Create a table connector vs FPGA MGT (GT_X?_Y?)

You will need first to make the link between FPGA pin number and associated MGT (GT_X?_Y?). Either use the data-sheet if available or FPGA editor.

Then make the correspondence between FPGA pins and connector pins.

For example:

Connector xyz

Pins		RSL Number	MGT Location
1	2	RSL0	GT_X6_Y0
3	4		
5	6	RSL1	GT_X5_Y0
7	8		
9	10	RSL2	GT_X4_Y0
11	12		
13	14	RSL3	GT_X3_Y0
15	16		
17	18	RSL4	Unused
19	20		
21	22	RSL5	Unused
23	24		
25	26	RSL6	Unused
27	28		

6.2. PCB LAYOUT

6.2.1. Powering circuitry

6.2.1.1. Decoupling

Input and output decoupling should be located close to the regulator. Follow Xilinx recommendations.

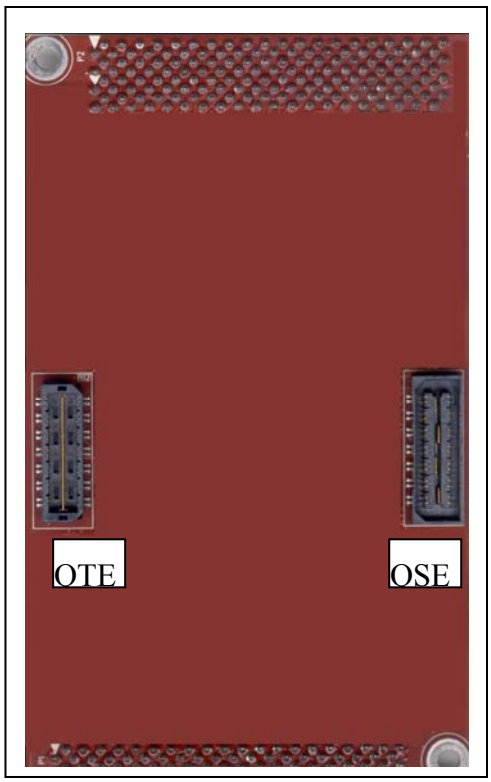
6.2.1.2. Filtering

Xilinx provides detailed information on how to position the power-filtering network.

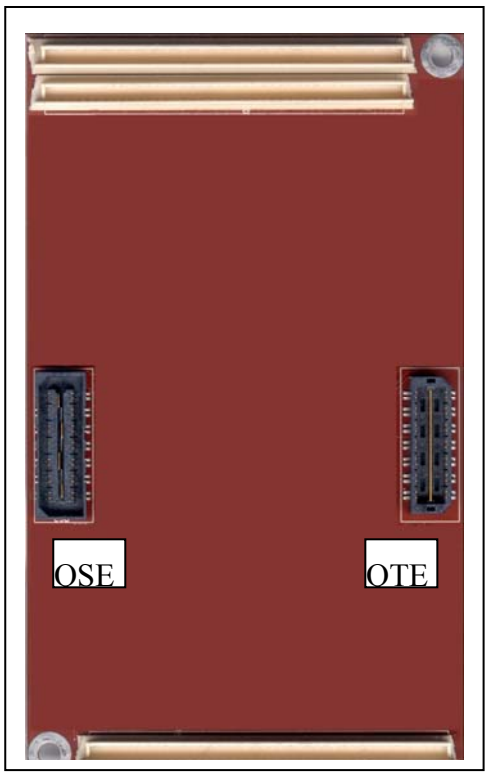
6.2.2. Connectors

6.2.2.1. Type, position and orientation top and bottom

Pictures of top and bottom TIM show the connectors and their orientation.



Top



Bottom

See exact positioning described in the RSL specifications.

6.2.2.2. Footprint

Detail can be obtained on the footprint.

6.2.2.3. Ground connection

Check middle ground connection of each connector.

6.2.3. Power Planes

The power plane should be designed to allow for minimal return current path. Wherever high-speed signal cross between two reference-planes with the same levels additional vias should be added between these planes. If crossing between different reference plane has to occur then decoupling between these plane should be added.

6.2.3.1. Power/Ground plane

Make sure that differential pairs and clocks have a ground reference plane on an adjacent layer.

A power reference plane is only acceptable when it runs all the way between the two components, which is not possible to guaranteed between TIMs.

Check that the pairs are not crossing any reference plane boundary.

6.2.3.2. Vias

Via on the pairs are to be avoided. If signals change planes (reference plane) make sure they have the same reference plane and proximity vias between these reference planes are added (one to three stitching via per differential pair).

If they have to jump from ground to power reference plane add 10nF decoupling capacitors between the two planes adjacent to the vias.

6.2.4. Differential oscillators

6.2.4.1. Differential routing

Pairs should start spread, watch for noise source. Do not route over long distances (TBD) in parallel with other signals. It is recommended that to control crosstalk, serial differential traces should be spaced at least five trace separation widths from all other PCB routes, including other serial pairs.

Try to only pair signals with the same phase (length),

Constant distance between pairs all the way. Check trace width, trace spacing and spacing between pairs and adjacent signals.

Avoid discontinuities, use teardropping, less than 45 degrees angles, via should not be used to change direction.

Trace should be point to point. Avoid stubs, branch with un-terminated ends, check the signal path through the via and minimize the left over (use blind via if possible). Always use as much of the via as possible.

6.2.4.2. Location of termination

Each standard has its own strict requirement in term of position of the external terminations. Always specify when internal terminations are to be used and check that the specific requirements can be met (For example Resistors connected to VRP and VRN pins and VCCO set to correct level).

6.2.5. Differential Trace

6.2.5.1. Differential routing

The signal should be hand routed. Xilinx has very good routing guidelines.

Pairs should start spread, watch for noise source. Do not route over long distances (TBD) in parallel with other signals. It is recommended that to control crosstalk, serial differential traces should be spaced at least five trace separation widths from all other PCB routes, including other serial pairs.

Try to only pair signals with the same phase (length),

To avoid stubs on the connector the trace should start from the outer edge of the connector footprint. The pair polarity can be inverted to make the routing easier. This is to consider very carefully and to document well as the board will not work without specific constraints added.

Constant distance between pairs all the way. Check trace width, trace spacing and spacing between pairs and adjacent signals and vias. In chip-to-chip PCB applications, 50 Ohms termination and 100 Ohms differential transmission lines are recommended.

Once the stack up has been defined PCB manufacturer should be contacted to know the appropriate track dimensions and spacing. Include that information in the report.

Avoid discontinuities, use teardropping, less than 45 degrees angles, via should not be used to change direction.

Trace should be point to point. Avoid stubs, branch with un-terminated ends, check the signal path through the via and minimize the left over (use blind via if possible). Always use as much of the via as possible.

Match pair length. The length matching recommended is 50 mils (1.27 mm), which is very small for most architecture. Get as close to that figure as you possibly can.
Return current imbalance fraction is = (Tp*Ldiff)/Rt
Tp : Propagation delay of media. Tp=180ps/inch or Tp= 7ps/mm
Ldiff : Length difference between trace.
Rt: Tising time of signals in ps. Typically ps for rocket io 100ps rise time at 2.5Gb/s 60ps for 3.125Gb/s.

Max tolerance is 7*1.27/60=0.15 <=> 15% equivalent to 2.1mm tolerance for 2.5Gb/s.
The tolerance has to be shared between boards so each board is allowed 1mm length difference between pairs.

Generate report on length => Highlight all of them for comparison. Check for length, vias and overall routing. Report should be available for future reference.

A ground reference should not be uninterrupted along the routing.

6.3. DESIGN VERIFICATION

6.3.1. Pre-build test

6.3.1.1. Test with BERT (Bit Error Rate Test) on itself.

This will show if the links are detected and the response of the link under various worse case data pattern.

A loopback is performed on the same board and the interconnected lanes are tested one after each other with a set of 12 different patterns to analyse the link sensitivity. It is expected to validate the link, check the clock quality and crosstalk.

The test results are logged into a file and can be provided with the test report.

The test should be also be performed between two different boards.

6.3.1.2. Test with interface inter-board communication.

This checks clock correction between modules and validate the interface provided.

6.3.1.3. Eye pattern diagram, clock jitter measurement.

Use Xilinx's RocketLab for eye pattern measurements. The measurements are performed on a blank pcb without FPGA but with connectors fitted and 100 ohms termination resistors added across balls corresponding to the receiving pairs.

7. DESIGN CHECKLIST

7.1. SCHEMATICS

7.1.1. Powering circuitry

Verification to perform	Yes	No
Regulator part is a recommended one		
Input decoupling follows full Xilinx spec 10uF		
Output decoupling follows full Xilinx spec 330uF + n x 1uF		
Active devices filtering inductor and capacitors (if not available in the package) connected as recommended		
Unused RSL powered and filtering requirement checked.		
Common-mode voltage can be set for AC and DC through VTRX circuitry		

7.1.2. Oscillator

Verification to perform	Yes	No
Part is a recommended one with less than 50ps jitter		
Termination techniques correspond to the standard		
Internal termination (if to be used) requirements checked. Add info to report.		
Oscillator mapping onto FPGA, location polarity checked		
Clock buffering used with the same standard		

7.1.3. Connectors

Verification to perform	Yes	No
Connector type QSE, QTE selected according to positioning		
Top and bottom symbol checked		
Differential pairs distribution onto connector checked		
Pair polarity checked		
Summary table added into report		

7.2. PCB LAYOUT

7.2.1. Powering circuitry

Verification to perform	Yes	No
Position of input and output powering circuitry checked		
Position of filtering circuitry checked		

7.2.2. Connectors

Verification to perform	Yes	No
Connector position and orientation checked		
Connector footprint checked		
Connector ground connection checked		

7.2.3. Power/ground reference planes

Verification to perform	Yes	No
A reference plane is on an adjacent layer to the differential clock routing		
A ground plane is on an adjacent layer to the differential pairs routing		
Differential signal have an uninterrupted reference plane on an adjacent layer and are not crossing a reference plane boundary		
Stitching vias between planes are present where pair changes to an identical reference plane.		
Decoupling capacitors (10nF) between planes are present where pair changes to a different reference plane		

7.2.4. Oscillator

Verification to perform	Yes	No
Oscillator routing is 100-ohm differential matched impedance		
Oscillator routing is matched in length between pairs (i.e. less than…)		
Report on differential traces length generated		
Routing follows guidelines (point to point, no stubs)		
Terminations (if any) are correctly positioned		

7.2.5. Differential pairs

Verification to perform	Yes	No
Differential pairs routing is 100-ohm differential matched impedance Add PCB manufacturer recommendations to report		
Differential pairs routing is matched in length between pairs (i.e. less than 1.27mm)		
Report on differential traces length generated		
Wide spacing with adjacent signals (5 x track width)		
Routing follows guidelines (point to point, no stubs)		
Terminations (if any) are correctly positioned		

7.3. DESIGN VERIFICATION

7.3.1. BERT

Verification to perform	Yes	No
BERT design generated for the chip		

7.3.2. Interface

Verification to perform	Yes	No
Interface design generated for the chip		

7.3.3. Eye pattern

Verification to perform	Yes	No
Eye pattern and clock jitter measurements made (to be added to the report)		

8. TEMPLATE FOR BOARD REPORT

8.1. CLOCK TERMINATIONS

The clock can be terminated internally or externally. Please specify the terminations techniques required.

Internal terminations are not to be used on this board external termination resistors are fitted

8.2. OSCILLATORS AND PINOUT

Describe which frequency is available to clock the design and the pins on which it is mapped.

For example:

Top	BREFCLK	P	GCLK4S	F16	LVPECL	125MHz
		N	GCLK5S	G16		
	BREFCLK2	P	GCLK2P		Unconnected	Unconnected
		N	GCLK3P			

Bottom	BREFCLK	P	GCLK6S	AH16	LVPECL	125MHz
		N	GCLK7S	AJ16		
	BREFCLK2	P	GCLK0P		Unconnected	Unconnected
		N	GCLK1P			

8.3. CONNECTOR MAPPING

For each connector provide a mapping between internal transceiver and connector pinout.

For example:

Connector RSLA:

Pins		RSL Number	MGT Location
1	2	RSL0	GT_X6_Y0
3	4		
5	6	RSL1	GT_X5_Y0
7	8		
9	10	RSL2	GT_X4_Y0
11	12		
13	14	RSL3	GT_X3_Y0
15	16		
17	18	RSL4	Unused
19	20		
21	22	RSL5	Unused
23	24		
25	26	RSL6	Unused
27	28		

8.4. POLARITY INVERSION

Report if any polarity inversion is required on a lane Rx or Tx.

8.5. CLOCK TRACKS LENGTH

Net name	Route Length (mm)	Total Connections	Total Vias
RCLK	45.338	3	3
NRCLK	40.323	3	3

8.6. DIFFERENTIAL PAIRS TRACK LENGTH CONNECTION AND VIAS

Example

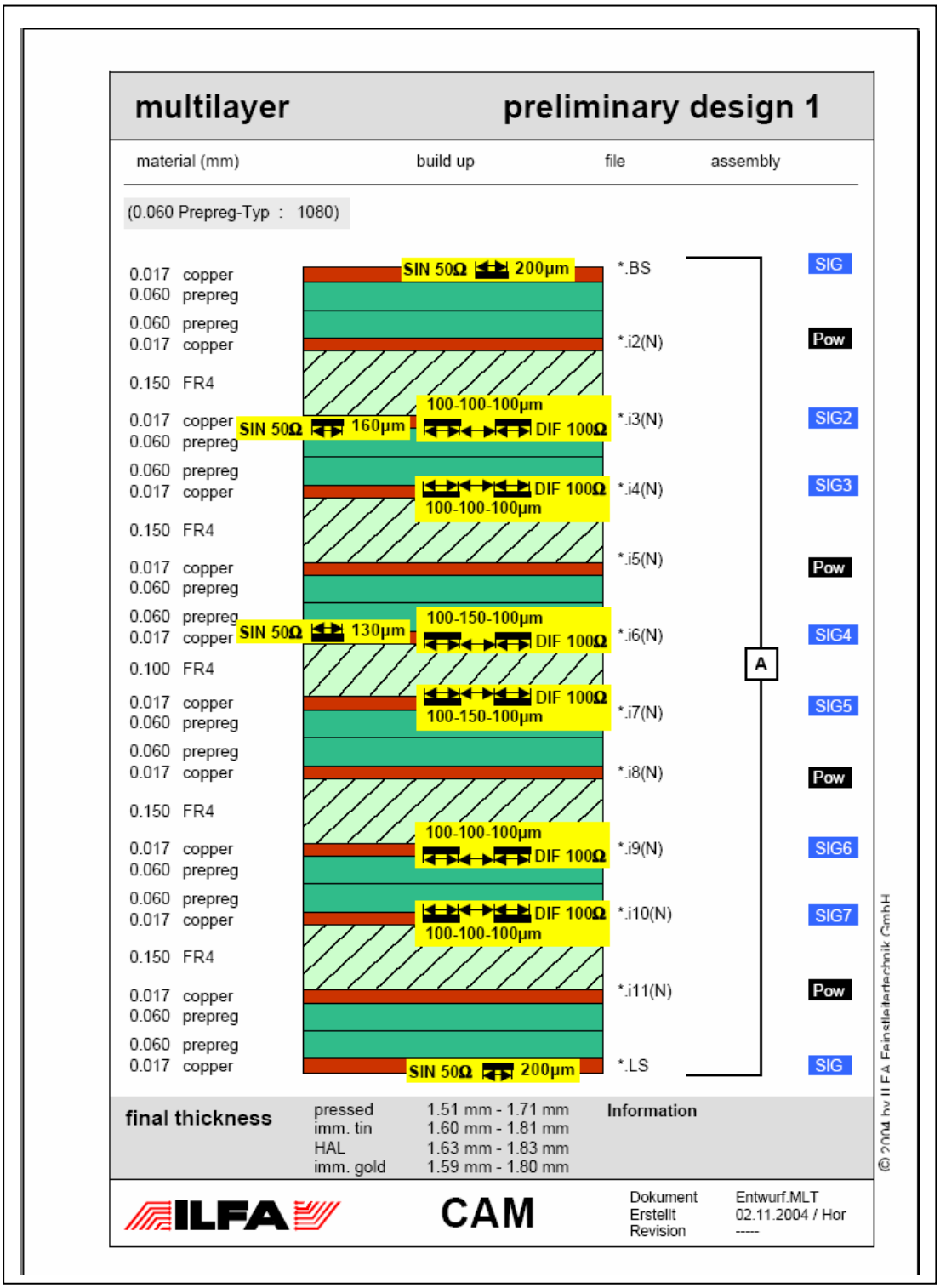
Net name	Route Length (mm)	Total Connections	Total Vias
RX0N	42.312	1	2
RX0P	44.216	1	2
RX1N	34.353	1	2
RX1P	36.818	1	2
TX0N	45.779	1	2
TX0P	45.760	1	2
TX1N	40.320	1	2
TX1P	39.877	1	2

A spreadsheet including all boards routing is available.

PCB stack up track dimension and spacing

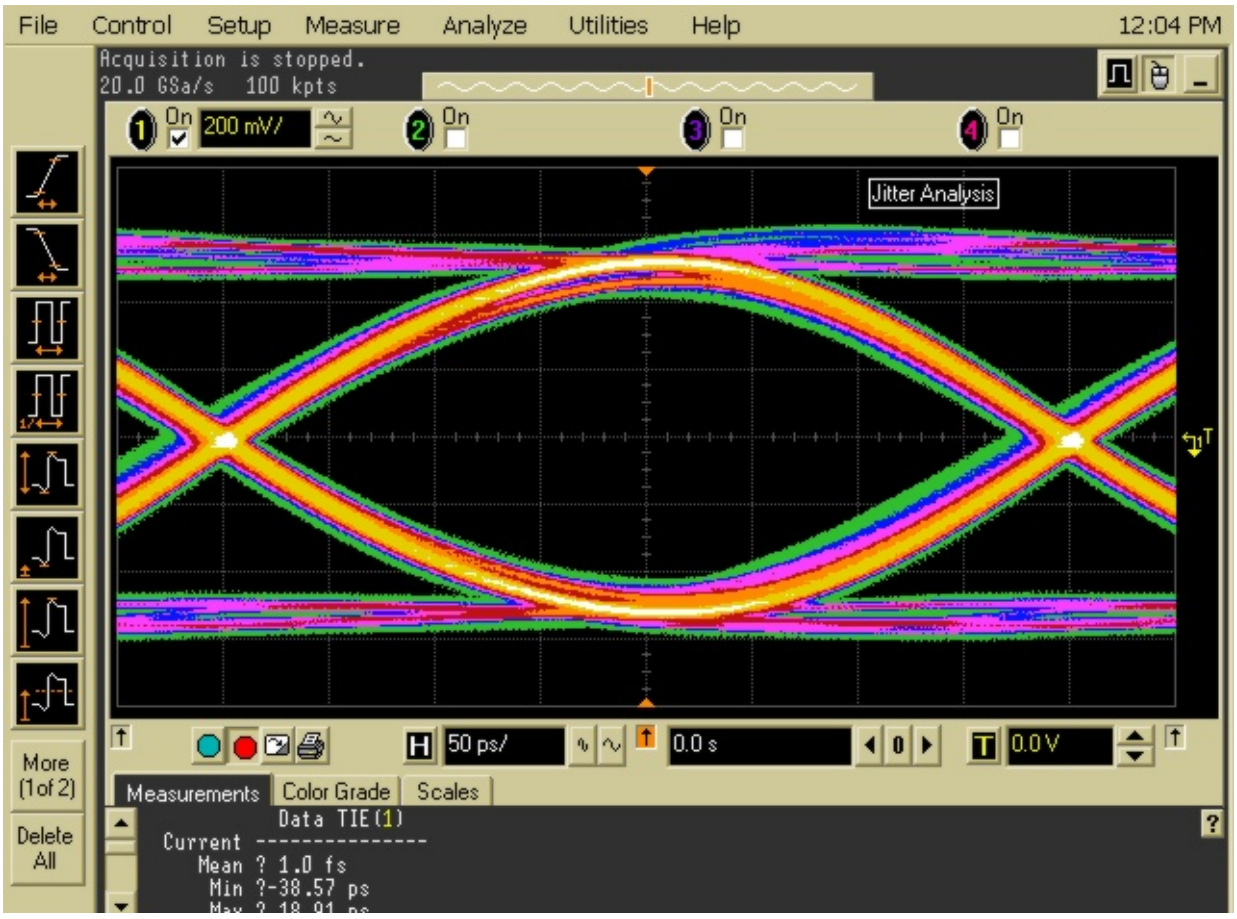
The pcb manufacturer is providing information on the pcb stack up and the track dimensions to get the recommended impedance. Please include the description for future reference.

For example



8.7. EYE PATTERN MEASUREMENT

Include results form eye pattern measurements in the report.



9. DOCUMENTATION

- Software Design Descriptions
- Software Source Code
- User Manual
- Hardware Verification containing:
    - Test Requirements
    - Test Procedures
    - Test Results

10.NOTES

None.