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Original Author:	F.SKWERES

User Manual for DVIP

Abstract

This document describes the system, the necessary tools and the examples provided to get started with the DVIP system.

Sundance Multiprocessor Technology Ltd, Chiltern House, Waterside, Chesham, Bucks. HP5 1PS.

Revision History

Issue	Changes Made	Date	Initials
1.0	Initial version	30/09/09	FS

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1 Introduction

The DVIP (Digital Video Infrastructure Platform) is based on the latest 1GHz TMS320C6455 DSP which offers the highest fixed-point processing of any commercial available TI DSPs and a scalable architecture that allows multiple DSP to be connected via a Serial Rapid I/O (SRIO) interface and this concept is well suited to the Sundance's Modular hardware concept that follows the TIM (Texas Instrument Module) standard. The basic configuration has a SMT362 Dual 'C6455 DSP Module and a SMT339 DM642 Image Module hosted on a SMT148-FX stand-alone carrier board. The DVIP can be upgraded with another 2x Modules from the range of over 40 different combinations, offering more processing-power, high-speed ADC/DAC interface, RF test-bed or custom-bespoke hardware.

DVIP is designed for high-performance, semi-rugged mobile and stationary deployment or for "Rapid Prototyping" of algorithms or hardware concepts. The SMT148-FX carrier board offers SATA, USB 2.0, FireWire, 1Gigabit Ethernet, RS485, RS232, LVDS interfaces. It also contains a Virtex-4 FX60 FPGA that includes two PowerPC cores and these can be used as controller for above interfaces, leaving the DSPs free for processing.

The DVIP is supported by TI's Code Composer Studio 3.3 and is required for any development of DSP code. No run-time licensees are required for the this OEM hardware platform and DVIP is furthermore Diamond® compatible and these tools offer a integrated development environment (IDE) for the DSP, FPGA and PowerPC based on the Eclipse front-end.

2 Related Documents

2.1 Referenced Documents

3L Diamond© User Guide

2.2 Applicable Documents

All the Sundance products User Guides are available from our website:

http://www.sundance.com/web/files/doc.asp

3 Acronyms, Abbreviations and Definitions

3.1 Acronyms and Abbreviations

TIM	Texas Instruments Module
DSP	Texas Instrument Digital Signal Processor
Comport	Communication Port. Standard communication interface developed by T.I
FPGA	Xilinx Field Programmable Gate Array.
SLink	Sundance link. High-speed Parallel port
CP	ComPort. Communication interface
RSL	Rocket Serial Link
SHB	Sundance High-Speed Bus. Communication interface
DDR	Dual Data Rate
TxCy	Denomination for TIM site x Comport y. x=1, 2, 3, 4 and y=0, 1, 2, 3, 4, 5 on a TIM carrier board.
VP	Video port
IP	Input port
OP	Output port

3.2 Definitions

DSP Module	Typically a TIM module hosting a TI DSP and, a Xilinx FPGA.
FPGA-only Module	A TIM with no on-board DSP, where the FPGA provides all functionality.
Firmware	A proprietary FPGA design providing some sort of functionality. Sundance Firmware is the firmware running in an FPGA on a DSP Module or on FPGA-only Module
Root	The starting point in every Diamond application is a processor (DSP or FPGA) called **root**. The root acts as the base of the network and a reference for locating all other processors.
Node	It is a processor (DSP or FPGA) that can be reached from the root by following wires through other processors

4 Tools Overview

4.1 Sundance Wizard

The Sundance Wizard (http://support.sundance.com/updates/Wizard/setup.exe.) will automatically install the latest version of the support packages required by your system.

In particular:

- SMT6002: Download Utility tool for the FPGA module.
- SMT6300: Drivers for Sundance PCI Hardware and server utility.

The Sundance help file (Sundance.chm) describes the hardware, firmware and software tools needed to use your Sundance Products. It is automatically installed by the “Sundance Wizard”, but can be downloaded separately from http://www.sundance.com/docs/Sundance.chm

5 Hardware Overview

5.1 Hardware Overview

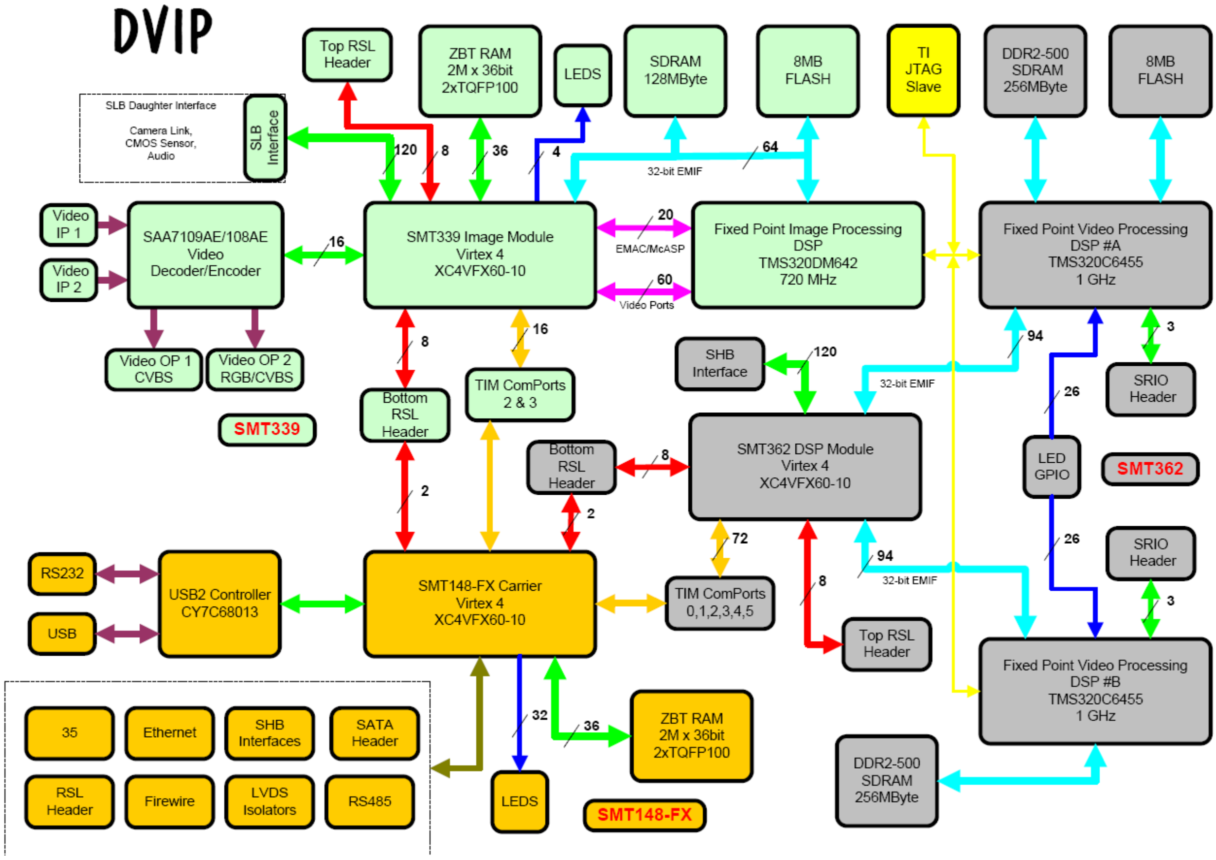

Figure 1: System Block Diagram

Figure 2: Top SMT339

Figure 3: Top SMT362

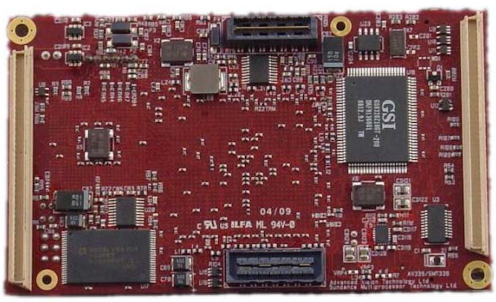

Figure 4: Bottom SMT339

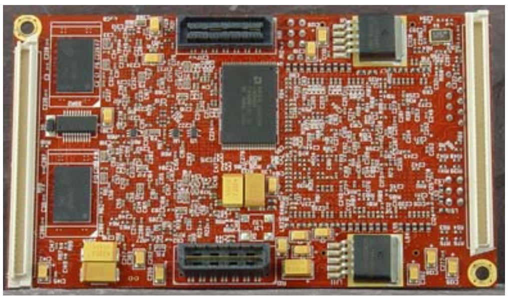

Figure 5: Bottom SMT362

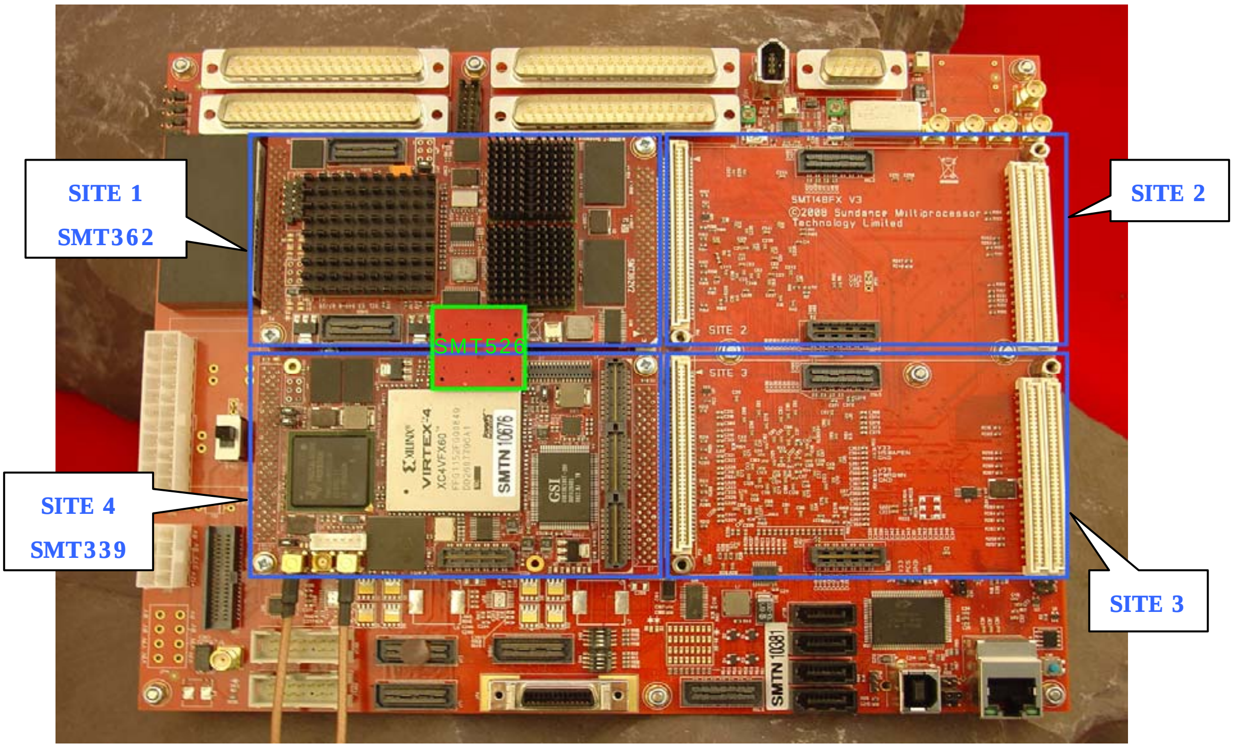

Figure 6: Top Hardware platform

The SMT339 can be use on SITE 2. Nevertheless, to use the RSL it's easier to use the SMT526 (RSL⇔RSL) with the SMT339 SITE 4 as shown figure 6.

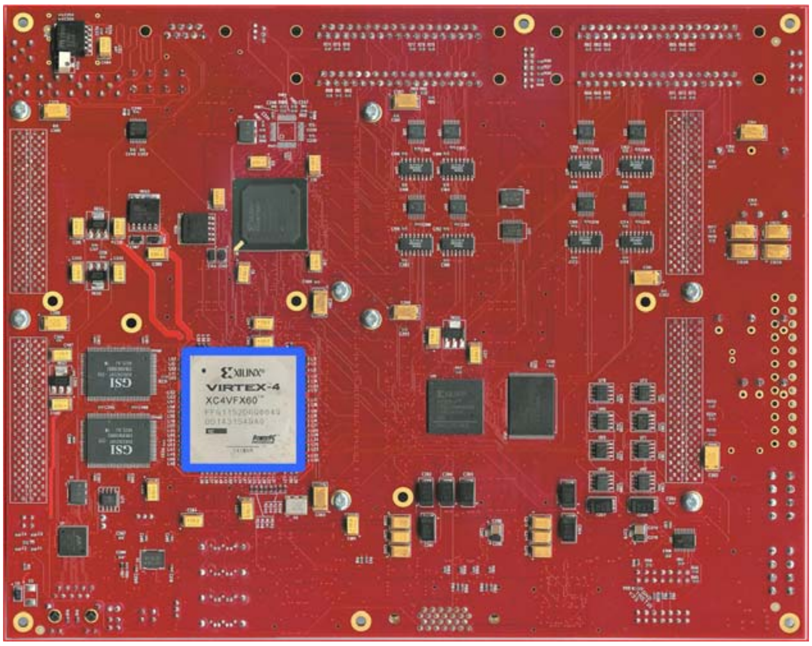

Figure 7: Bottom Hardware platform

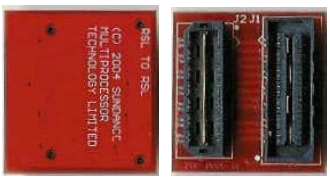

Figure 8: Bottom/Top SMT526

5.2 SMT148-FX comport firmware

The SMT148-FX uses a Xilinx Spartan 3 FPGA to drive most of the Comports between the different sites.

Each TIM site has 6 Comports.

Four of these are connected directly to the Spartan 3 FPGA. These are Comports 0, 1, 3 & 4.

Comports 2 & 5 are connected between TIM sites in a pipe configuration as follows;

All the Spartan firmware are available in the directory:

$\Program Files\Sundance\SMT6002\Firmware\Smt148FX\SPARTAN

A firmware has been developed for the DVIP system, that one allows you to use all the hardware capabilities and load all the bitstreams from the root.

"com.sundance.smt148-fx.sc3s1500.usb_default.DVIP.app"

Use the SMT6002 to change the Spartan firmware at the address 0x0.

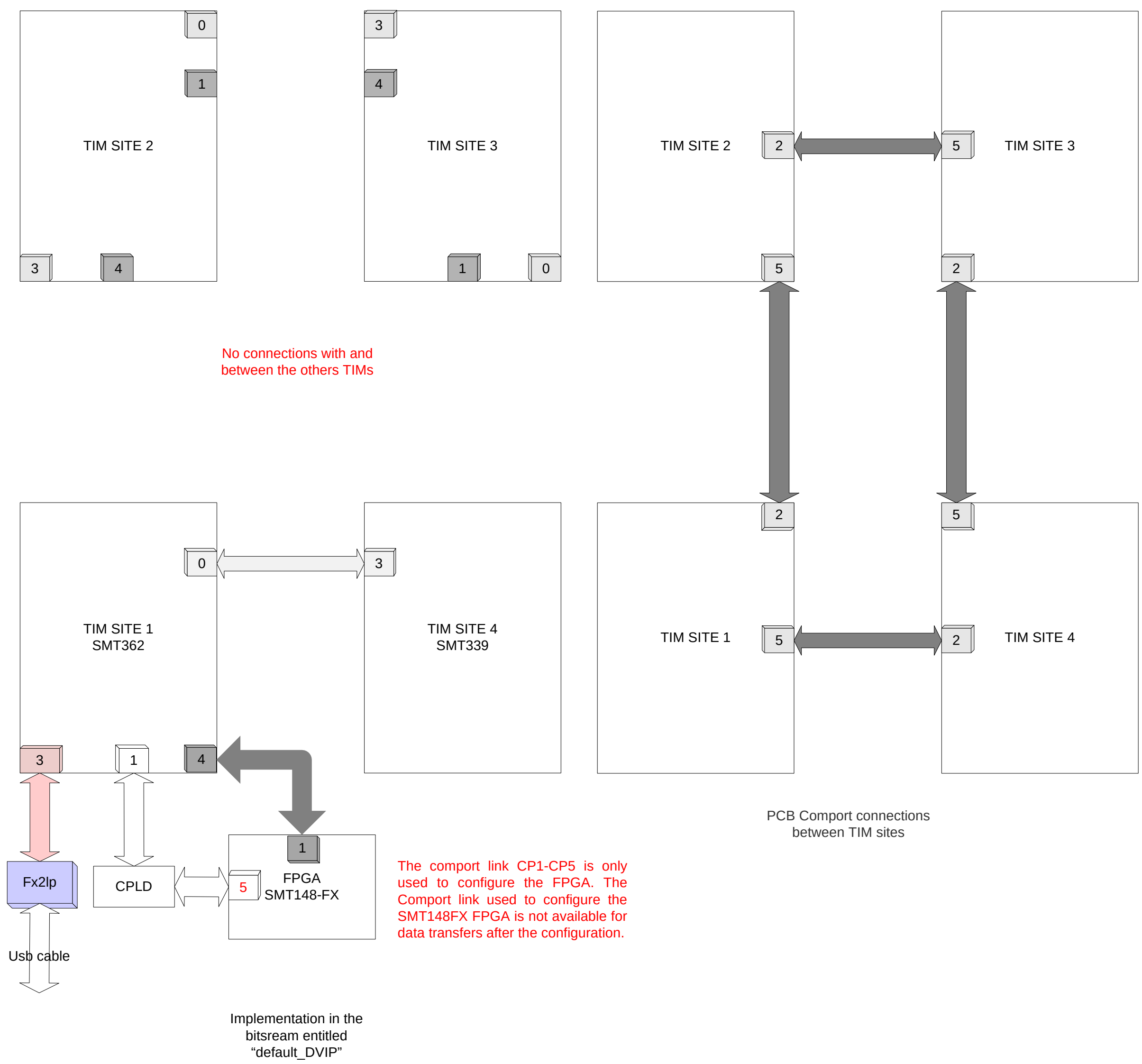

Figure 9 : DVIP bitstream comport configuration

6 Application

A demo system based on that setup has been developed to illustrate the hardware capabilities and to provide a starting point for developers.

6.1 Application explanation

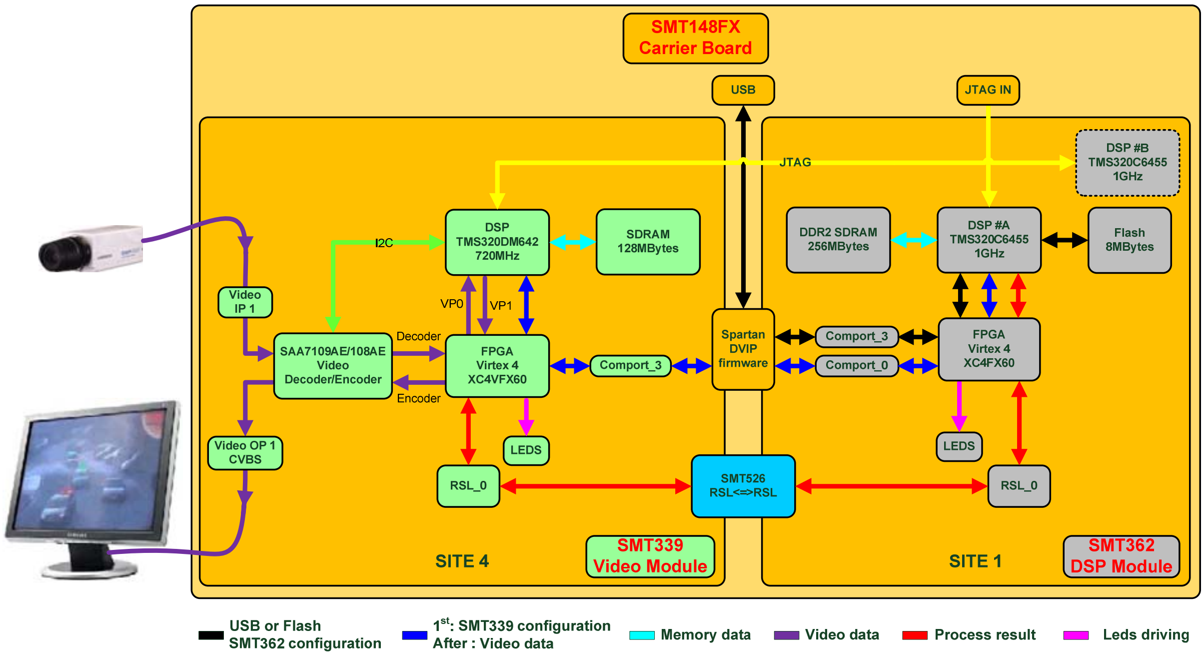

Figure 10: RSL application diagram

This application is a real time tracking demonstration that use a little part of the DVIP capability.

To begin, on the SMT339, the video from the camera is decode and send to the DM642 DSP through the Virtex 4 to allow some pre-processing in the FPGA and the image is save in the memory. The Sundance video library configures a DMA which will continuously send the image from the memory through the FPGA to the encoder, for post-processing, this time, and finally we get the video on the monitor.

In this demo there is no image processing in the SMT339 DSP, just two post-processing tasks, the location of the tracking objects (crosses and rectangles) and the Sundance logo which is saved in the Virtex 4 ROM is added to the video.

To find the objects which are moving, the SMT339 send the image from his memory to the SMT362 memory, through the comport or the RSL. Only one SMT362 DSP is used here. The algorithm in this DSP found the objects which move and send their locations to the SMT339 FPGA through the RSL.

The result is a real time video with in red the largest object which move, in green the second one and in blue the third one.

The Application note that describes the entire step to run and modify this tracking example will soon be available.