Unit / Module Name:	DSP Module
Unit / Module Number:	SMT362
Used On:	Sundance TIM Carrier Boards
Document Issue:	See revision history
Date:	See revision history

CONFIDENTIAL

Outline Description

The SMT362 is a dual processor module. Each TMS320C6455 processor runs at up to 1GHz. This provides a module performance of up to 16GIPS.

Each processor has independent access to 256Mbytes of DDR SDRAM.

A single 8Mbyte flash memory device is directly connected to the primary DSP (DSP A). This device contains the DSP boot code and FPGA (Virtex-4) configuration. The secondary DSP (DSPB) is booted by DSPA using the host port interface.

The FPGA provides 6 TIM compatible comm. ports, 2 Sundance SHBs, up to 16 RSLs, and other minor functions. The FPGA can be easily customised.

The SMT362 could be used in applications where the FPGA does the pre-processing, the first DSP the 'Input Signal Processing', the second DSP does 'Output Signal Processing', and the FPGA does the final post-processing.

Approvals		Date
Managing Director		
Software Manager		
Design Engineer		

Certificate Number FM 55022

Revision History

Date	Changes Made	Issue	Initials
28/1/05	First draft	1.0.0	GKP
16/8/05	Updates for TMS320C6455 DSP	1.1.0	PTM
16/9/05	Updates to match first schematics	1.2.0	PTM
19/1/05	Major update of all diagrams	1.3.0	GP
24/4/06	Added I2C boot mode for 2nd DSP	1.3.1	GP

Table of Contents

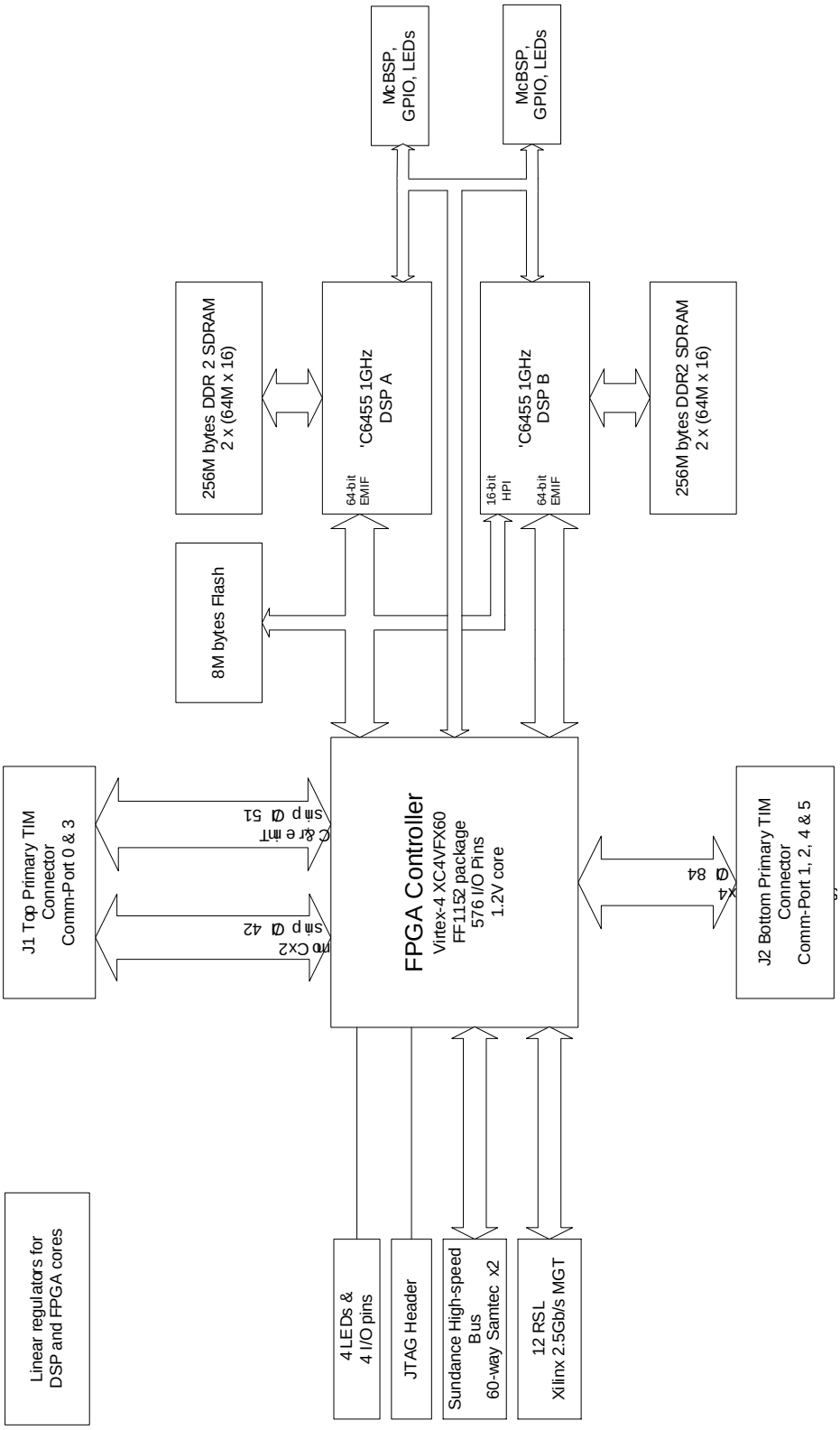
1 Introduction

1.1 Related Documents

TI TMS320C6455 data sheet and peripherals guide.
Sundance SHB specification.
Sundance RSL specification.
TI TIM specification & user's guide.

2 Functional Description

2.1 Block Diagram



2.2 Interface Description

2.2.1 Mechanical Interface

This module conforms to the TIM standard for single width modules. It requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards) which must be provided by the two diagonally opposite mounting holes.

2.2.2 Electrical Interface

2.2.2.1 Processor

The module incorporates two TMS320C6455 DSPs.
A JTAG interface is provided to enable application debugging via a suitable JTAG controller and software. Typically, this will be an SMT107 or 310 and TI Code Composer Studio. This is an invaluable interface which enables the application programmer to quickly debug a 'chain' of processors in single or multi-processor situations.
The DSPs have one External Memory Interface (EMIF) and one DDR2 Memory Interface. The DDR2 interface of each DSP is used to connect 256M of DDR2 SDRAM. This is implemented using two FBGA memory devices per DSP.
The EMIF is used to connect to the Virtex-4. The flash is connected as a 16 bit device to the EMIF. The EMIF supplies 4 'chip selects' which are used for these selections.
These chip selects provide this basic memory map:

Memory space EMIF	Resource DSP A	Resource DSP B	Address range
CE0	Not available	Not available	0x80000000 - 0x8FFFFFFF
CE1	Not available	Not available	0x90000000 - 0x9FFFFFFF
CE2	Virtex 4 FPGA	Virtex 4 FPGA	0xA0000000 - 0xAFFFFFFF
CE3	Flash	N/A	0xB0000000 - 0xB07FFFFF
CE4	DSPB host port interface	N/A	0xC0000000 - 0xC00000FF
CE5	Virtex 4 configuration	N/A	0xD0000000 - 0xD0000000

Memory space DDR2	Resource DSP A	Resource DSP B	Address range
CE0	DDR2 SDRAM	DDR2 SDRAM	0xE0000000 - 0xEFFFFFFF

2.2.2.2 Flash

An 8Mbyte flash memory is provided with direct access by DSPA. This device contains boot code for the DSP and the configuration data for the FPGA.
This device is directly connected to DSPA.
This is a 16-bit wide device.
The first few k bytes are used for DSP boot code. The remainder of the first 512k bytes is used for FPGA configuration data.

The flash device can be re-programmed by the DSP at any time. There is a software protection mechanism to stop most errant applications from destroying the device's contents. The CE3 memory space decode should be switched to 32-bit mode when writing to the flash, and the most significant 16 bits of data should always contain 0.

2.2.2.3 DSP Reset

The DSPs' configuration is determined during the reset process. The state of the EMIF address lines is examined, and this determines the on-chip peripheral status.
The following table details this;

EMIF A	Comment
0	Latched at reset. Not used on the 362.
1	Latched at reset. Not used on the 362.
2	Latched at reset. Not used on the 362.
3	Pull-up via 1k0.
4	GP01 function. Connected to CPLD via 1k0. A '0' (default) makes this an I/O pin. A '1' enables the SYSCLK3 signal to be output.
5	McBSP1 or GPIO selection. Connected to the CPLD via 1k0. A '1' enables the McBSP (default).
6	NC – PCI speed.
7	NC – internal pull-down.
8	NC – PCI auto-init.
9	Pull-up with 1k0. Used to select MAC with an RGMII interface.

EMIF A	Comment
10	Pull-up with 1k0. Used to select MAC with an RGMII interface.
11	Pull-up via 1k0.
12	UTOPIA or EMAC select. Internal pull-down selects EMAC.
13	Internal pull-up selects little endian operation.
14	Internal pull-down selects 16 bit HPI operation.
15	Connected to CPLD via 1k0. A '0' selects external clock for EMIF. A '1' selects SYSCLK3/8 as EMIF clock.
16	Internal pull-down. Set to '0' for DSPA. Set to '1' for DSPB. Together with EMIFA17-19, this sets the boot mode.
17	Internal pull-down.
18	Internal pull-down. Set to '1' for DSPA. Set to '0' for DSPB.
19	Internal pull-down.

Boot mode is the 4-bit value from EMIFA[19:16]. This is 0100 for DSPA (ROM boot) and 0001 for DSPB (HPI boot).

2.2.2.4 DSP Boot

When the module is reset DSPA will come out of its reset state and copy the first 1k bytes from flash into its internal program memory and then begin executing this code. This boot code (factory programmed by default) will then load the FPGA configuration (again from flash), perform any necessary initialisation and then enter a comm port boot sequence. The comm port boot involves polling the comm port status register(s) and downloading code from the first active port. The format of this data stream is as follows:

Header	Words 1 to 4 Word 5 Word 6	0, 0, 0, 0 start address 0
Load Block	Word 1	4*N: Length of load block (in bytes)
	Word 2	Destination address (external memory only)
	Next N words	N data words
0 or more Load Blocks		
Terminator	Word 1	0

1 A word is 32 bits.
2 The length of each block of data will be rounded up to a multiple of 4 bytes.

DSPB has a different boot sequence. Because it has no direct access to flash memory, it is booted by DSPA using the host port interface or I2C interface.

2.2.2.5 Virtex-4

This device, a Xilinx XC4VFX, is responsible for the provision of the two SHBs, the 6 comm ports, and the RSLs. On power-up, this device is un-configured (SRAM based FPGA technology). During the DSP boot process, the FPGA is configured for normal operation.
The standard configuration for the primary FPGA uses 500k (TBC) gates. The remainder can be used for additional functionality.

Interface	Total I/O	FX60
64-bit EMIF x2	186	186
SHBs x2	120	120
Comports x6	72	72
LEDs, GPIO, triggers	24	24
RGMII x2	32	52
Total		**538**
Available		**562**

2.2.2.5.1 Configuration

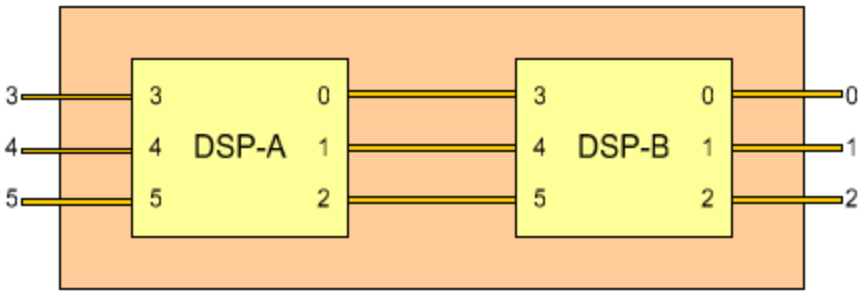
Before any functions of the FPGA can be used it must be configured. This is a process undertaken by DSPA during its boot procedure. The FPGA is configured via the slave select map mode (an 8 bit peripheral type mode).
First, the PROG pin must be asserted low, then high. this is accomplished by writing to DSPA's GP02 pin; first with this bit high, then low, and then high again.
Then 8 bit data must be read from the flash and written to the FPGA using EMIF memory space CE5.

2.2.2.6 Host Port Interface (HPI)

The HPI of DSPA is not connected, and DSPB's is connected to the EMIF of DSPA.

2.2.2.7 Comports

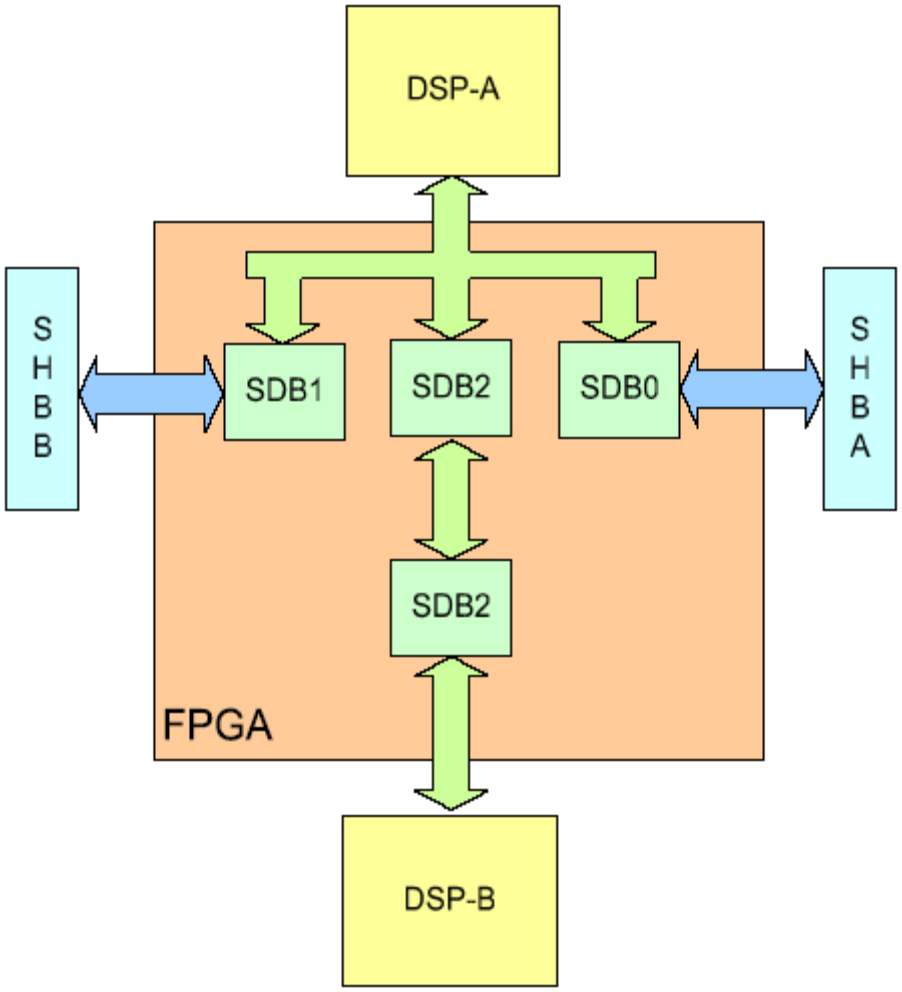
Both DSPA and DSPB have six Comports, numbered 0 to 5. Each DSP has three Comports connected to the other DSP and three connected to the TIM connectors, as shown in the following diagram:



See the general firmware description for more info.

2.2.2.8 SHB

The SMT362 has two SHB connectors, both of which are connected to DSPA to give 32-bit SDB interfaces.
SDB0 and SDB1 on DSPA are presented on the TIM's SHB connectors, SHBA and SHBB respectively. SDB0 and SDB1 on DSP-B are not connected. SDB2 of DSPA has a fixed internal connection to SDB2 of DSPB.



See the general firmware description for more info.

2.2.2.9 External Clock

An external clock input is provided to the FPGA. This signal is directly input via an MMCX(MMBX?) connector.

2.2.2.10 PXI Signals

An external PXI clock and 4 trigger signals are available on the user defined pins of the TIM connectors. These can be used for a variety of purposes, including synchronisation and triggering of data acquisitions, or for any user application specific function.

2.2.2.11 Serial Ports

Two serial ports are provided for each DSP. One of these (on each DSP) connects to the FPGA. This enables an extra 6 interrupt signals from the FPGA to the DSP. The other McBSPs are connected between the DSPs.

2.2.2.12 General Purpose I/O (GPIO)

All of the DSP's GPIO signals are described here;

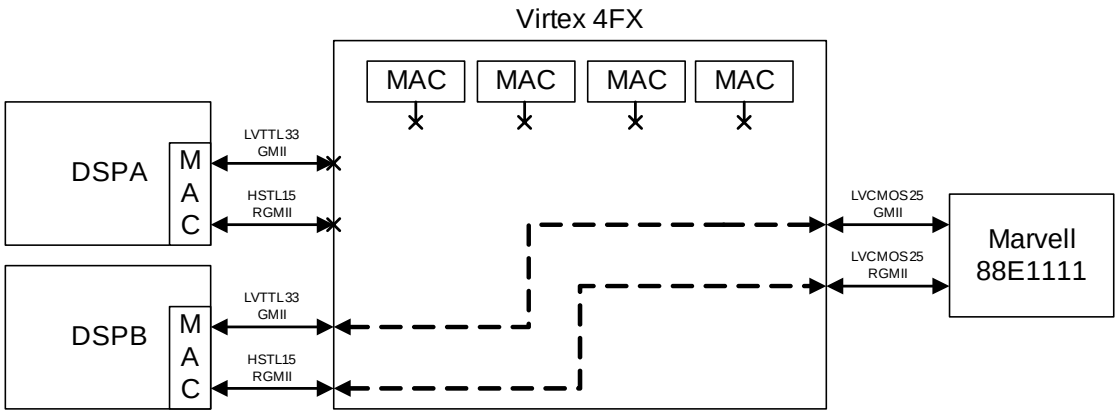
GPIO	Function
0	CLKR1 (to FPGA)
1	SYSCLK3
2	PROG
3	CLKX1 (to FPGA)
4	INT4 (to FPGA)
5	INT5 (to FPGA)
6	INT6 (to FPGA)
7	INT7 (to FPGA)

GPIO	Function
8	DR1 (to FPGA)
9	DX1 (to FPGA)
10	FSR1 (to FPGA)
11	FSX1 (to FPGA)
12	Flash A20
13	Flash A21
14	LED1
15	LED2

The McBSP signals (CLKR1, CLKX1, DR1, DX1, FSR1 and FSX1) are all connected to the FPGA. They are normally set to function as McBSP signals, but it is possible to enable these as GPIO and hence a source of a further 6 interrupts to the DSP.
The above signals are independent between DSPs.
GPIO2, 12 and 13 are connected to the FPGA on DSPB (DSPB does not have access to a flash memory and cannot configure the FPGA).

2.2.2.13 Gigabit Ethernet

The RGMII port of both DSPs is connected to the FPGA. A Gigabit Ethernet PHY (Marvell Alaska 88E1111) is connected to the FPGA will allow for the possibility of either DSP or Virtex 4 MACs having Ethernet connectivity.

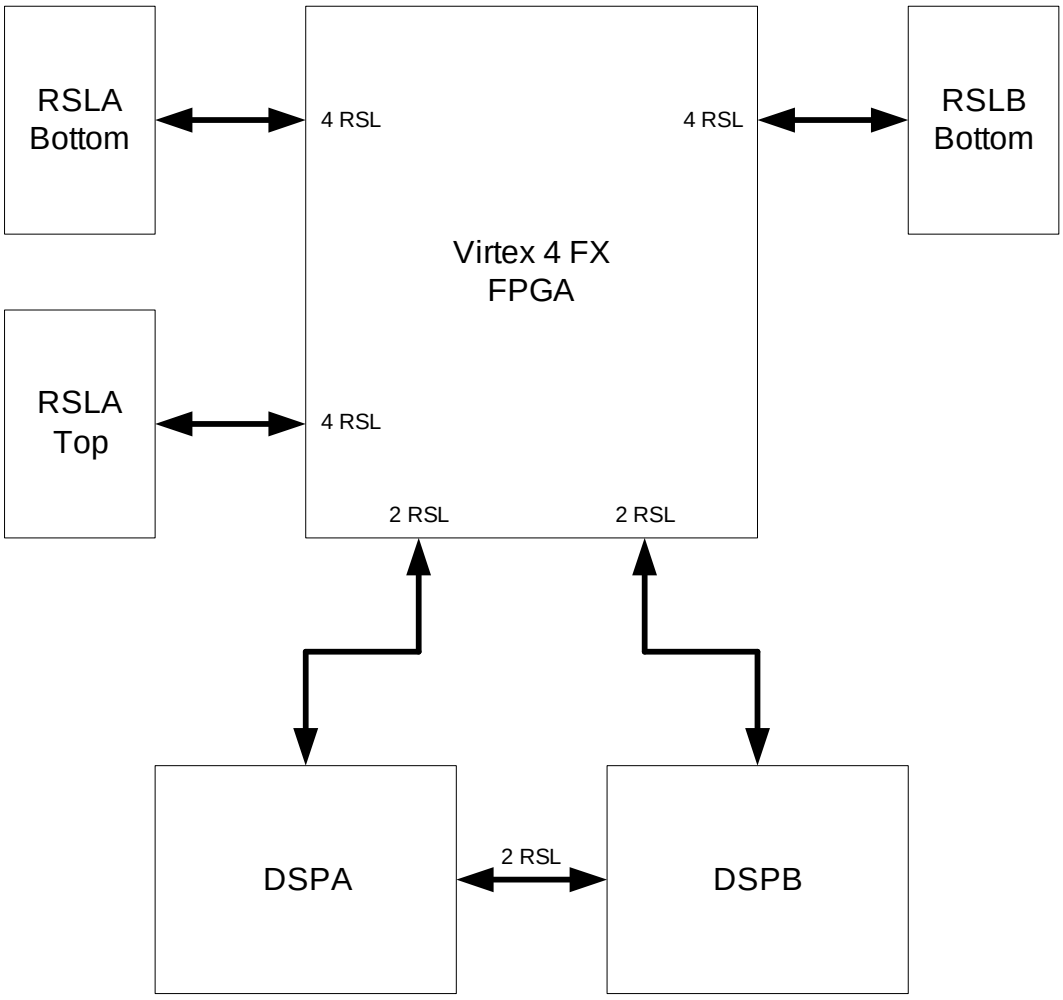


The default configuration of connecting DSPB's MAC directly to the 88E1111 PHY through the Virtex 4 is shown in the diagram above. In this configuration, the Virtex 4 is essentially acting as a voltage translator.

2.2.2.14 RapidIO and RSLs

The FPGA provides 16 RocketIO serial interfaces. These are normally run at 2.5Gbps.
Each DSP has 4 SRIO interfaces. Again, these are normally run at 2.5Gbps.
All of these serial interfaces are knows in Sundance as RSL (Rocket Serial Link).

The RSL connectivity is shown here;



2.2.2.15 Power Supplies

This module must have 5V supplied through the TIM connectors. In addition, a 3.3V supply is required and should be supplied through the TIM mounting holes. This is compatible with the all Sundance TIM carrier boards.
Contained on the module are switching regulators for the 'C6x, FPGA, and DDR2 SDRAM.
The RocketIO voltage is provided through a linear regulator from 3.3V.
All supplies a guaranteed to meet the worst possible requirements of the FPGAs.

Device	Supply	Voltage	Tolerance	Current (mA)	Description	Derived From
C6455	VREFHSTL	0.75	5.00%		Reference for HSTL buffer	Resistor divider from DVDD15
C6455	VREFSSTL	0.9	5.00%		Reference for SSTL buffer	Resistor divider from DVDD18
Virtex 4	VCCINT	1.2	5.00%		Internal supply voltage relative to GND, TJ = 0° C to +85°C	CVDD
C6455	CVDD	1.2	2.50%		Core supply	Switcher from 5V
Virtex 4	VBATT	1.2	5.00%		Battery voltage relative to GND, TJ = 0° C to +85°C	
Virtex 4	AVCCAUXTX	1.2	5.00%	190		AVCCAUXRX
Virtex 4	AVCCAUXRXA	1.2	5.00%	115	Auxilliary receive supply voltage relative to GNDA	Dedicated LDO
Virtex 4	AVCCAUXRXB	1.2	5.00%	125		
C6455	DVDD12	1.2	5.00%	2000	Main SRIO supply	Dedicated LDO
C6455	AVDDA	1.2	5.00%		SRIO analog supply	Filtered DVDD12
C6455	AVDDT	1.2	5.00%		SRIO termination supply	Filtered DVDD12
C6455	DVDD15	1.5	5.00%		EMAC RGMII I/O voltage	
Virtex 4	VTRXA	1.5		8	Terminal receive supply voltage relative to GND	Dedicated LDO
Virtex 4	VTRXB	1.5		8		
Virtex 4	VTTXA	1.5		35	Terminal transmit supply voltage relative to GND	
Virtex 4	VTTXB	1.5		35		
C6455	AVDD18	1.8			I/O supply	Filtered DVDD18?
C6455	DVDD18	1.8	5.00%		DDR2 EMIF I/O Voltage	

C6455	DVDDR	1.8	5.00%		SRIO regulator supply	Filtered DVDD18
C6455	BEVDDDLL0	1.8				Filtered DVDD18
C6455	BEVDDDLL1	1.8				Filtered DVDD18
C6455	PLLV1	1.8				Filtered DVDD18
C6455	PLLV2	1.8				Filtered DVDD18
Virtex 4	VCCAUX	2.5	5.00%		Auxiliary supply voltage relative to GND, TJ = 0° C to +85°C	Dedicated LDO
Virtex 4	AVCCAUXMGT	2.5	5.00%	2	Auxilliary management supply voltage relative to GNDA	VCCAUX?
C6455	DVDD33	3.3	5.00%		I/O supply voltage	External

Alternating shading indicates supplies connected together.

3 Verification Procedures

The specification (design requirements) will be tested using the following:

1) Running Code Composer Studio.
2) Running 3L Diamond.
3) SHB self-test.
4) Running RSL self-tests.
5) RapidIO test (TBD)
6) DSP Ethernet test (TBD)

4 Review Procedures

Reviews will be carried out as indicated in design quality document QCF14 and in accordance with Sundance's ISO9000 procedures.

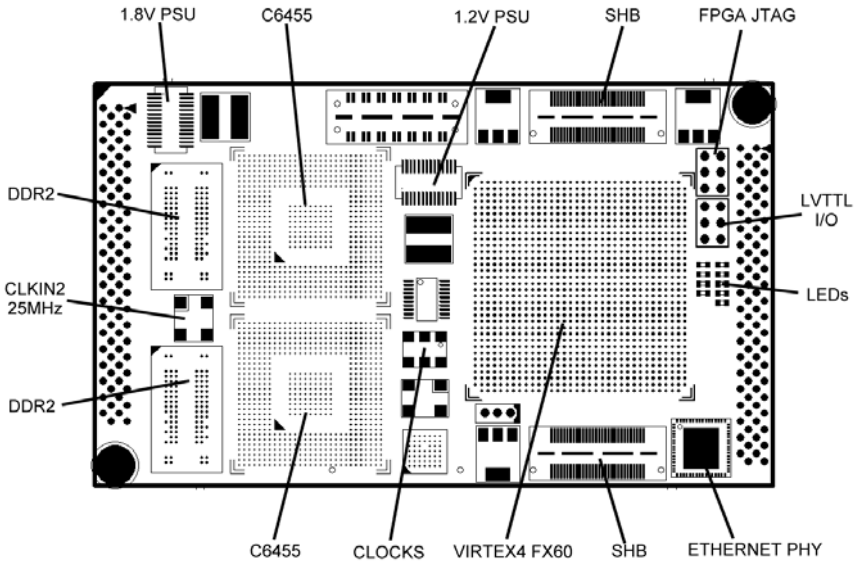
5 Validation Procedures

6 Timing Diagrams

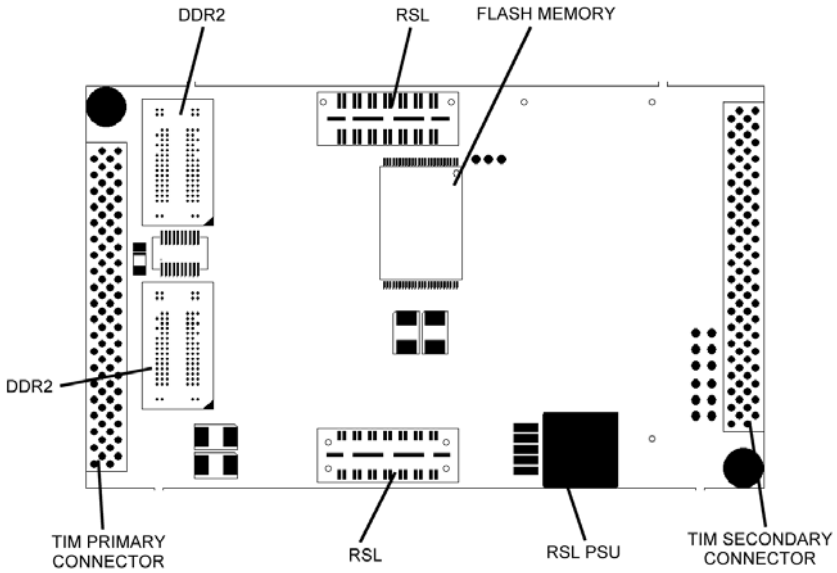
7 Circuit Diagrams

8 PCB Layout Details

8.1 Component Side



8.2 Solder Side



9 Safety

This module presents no hazard to the user.

10 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.
This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.
Short circuiting any output to ground does not cause the host PC system to lock up or reboot.