iUnit / Module Description:	Dual C6472 EVM
Unit / Module Number:	SMT372T
Document Issue Number:	1.10
Issue Date:	20th January 2011
Original Author:	Graeme Parker

Product Specification for SMT372T

Sundance Multiprocessor Technology Ltd, Chiltern House, Waterside, Chesham, Bucks. HP5 1PS.

Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	12th May 2009	GKP
1.1	Update.	14th May 2009	GKP
1.2	Added top RSL connector.	14th May 2009	GKP
1.3	Added FPGA I/O table.	19th May 2009	GKP
1.4	Corrected number of McBSPs, and their connectivity. Changed the Ethernet PHY model. Commented that the DSPs' GPIO driver LEDs.	26th May 2009	GKP
1.5	Removed reference to 16 GTX on FX70.	16th July 2009	GKP
1.6	Updated board layout drawing.	8th Sept 2009	GKP
1.7	Corrected McBSP references to UTOPIA	11th March 2010	GKP
1.8	Added JP4 detail	4th May 2010	GKP
1.9	Added DSP GPIO section	7th July 2010	GKP
1.10	Added RJ45 pin-out detail and link the SMT562E. Corrected part number typo.	20th January 2011	GKP

Table of Contents

1 Introduction / Description

The SMT372T is a dual C6472 single width TIM comprising:

- 2 TI C6472 6-core DSPs
- Xilinx Virtex5 FXxxT FPGA
- Two x16 DDR2 devices per DSP
- 10/100/1000 Ethernet PHY
- RSL connectors
- 64MByte flash memory

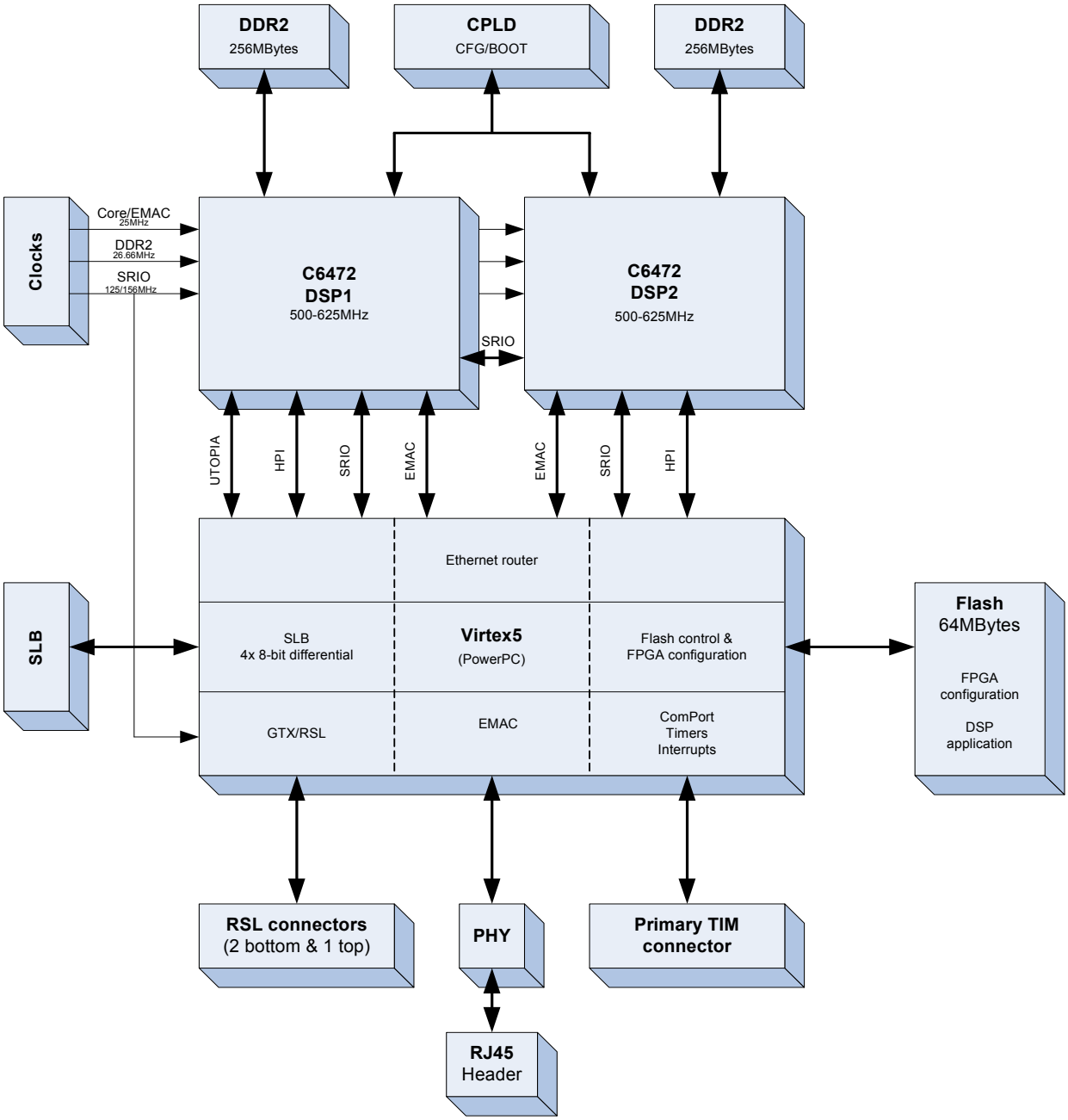
2 Related Documents

Xilinx Virtex5 documentation:
http://www.xilinx.com/support/documentation/virtex-5.htm

3 Acronyms, Abbreviations and Definitions

A list of acronyms etc: http://www.sundance.com/web/files/static.asp?pagename=acc

4 Block Diagram



5 Module Description

5.1 TI C6472 DSP

The SMT372T module includes two TI C6472 DSP devices.
Each C6472 incorporates 6 cores running at 500-625MHz.

5.1.1 DSP Clock

A 25MHz oscillator is buffered and routed to the DSPs' PLL1 and PLL2 inputs. These are used to generate the core and EMAC clocks.
The core clock multiplier can be selected to operate the device at 500-625MHz.
The EMAC always runs with a x20 PLL multiplier.

5.1.2 DSP Boot

Upon power-up or soft reset, the FPGA will configure itself from the byte-wide flash memory.
After configuration, the FPGA will load the DSPs' megamodules' boot code using HPI.
The megamodules will then be released from reset and further application loading can be either from flash or from an interface provided by the FPGA (RSL, ComPort).

5.1.3 GPIO

DSP1 has a single GPIO connection made available on the TIM connector. GP04 is connected to UDP1 (TIM pin 1).
DSP2 has two GPIO connections to the TIM connector. GP04 is connected to UDP2 (TIM pin 3), and GP03 is connected to UDP6 (TIM pin 9).

5.1.4 SRIO

Each DSP has 2 SRIO interfaces.
One SRIO from each DSP is connected together.
The second SRIO from each DSP is connected to the FPGA.
The SRIO external clock speed is 125MHz allowing operation at 1.25 and 2.5Gbps.
This is the same speed as the Sundance RSL implementation.

5.1.5 I2C

Each DSP has an I2C connection to the FPGA.
This is a slow serial interface running at up to 400kHz.
This is the simplest mechanism for the DSP to access the FPGA.

5.1.6 UTOPIA

Each DSP has a single 16-bit UTOPIA port.
The UTOPIA from DSP1 is connected to the FPGA. The remaining UTOPIA is un-connected.

A total of 50 FPGA I/O pins are needed for this interface.

5.1.7 HPI

A 16-bit interface exists from the DSPs to the FPGA using 26 I/O pins.
This is a DSP slave interface with the FPGA as the master. This interface is the mechanism by which the DSPs' boot code is loaded.
Access to all of the DSPs' resources can be made through the HPI.
The HPIs to the DSPs are independent.

5.1.8 DDR2 Memory (DDR533)

Two 16-bit wide devices are used for each DSP. Using 2G bit devices provides for 256Mbytes of memory per DSP.
The memory clock speed is 266MHz.

5.2 FPGA

A Xilinx Virtex-5 FXT device interfaces to both DSPs, the Ethernet PHY, flash memory, external GTX/RSL connectors, and other TIM resources.

The FPGA is set to master slave map configuration. Upon reset or power-up, the FPGA will configure itself from the flash memory.

5.2.1 JTAG

A 6-pin header is provided to enable programming and debugging of the CPLD and FPGA. The location of this header, JP4, is shown on the board layout drawing.

The pin-out is as follows;

TMS	TDI	TDO
4	5	6
1	2	3
VCC (3.3V)	GND	TCK

5.2.2 SLB (Sundance Local Bus)

A full implementation of the SLB is provided.
This interface incorporates 4 8-bit differential LVDS buses, general purpose LVTTL I/O, differential clocks and triggers. This interface uses 109 FPGA I/O pins.
The LVDS ports of this bus can operate at 2.5V or 3.3V; determined by a jumper position.

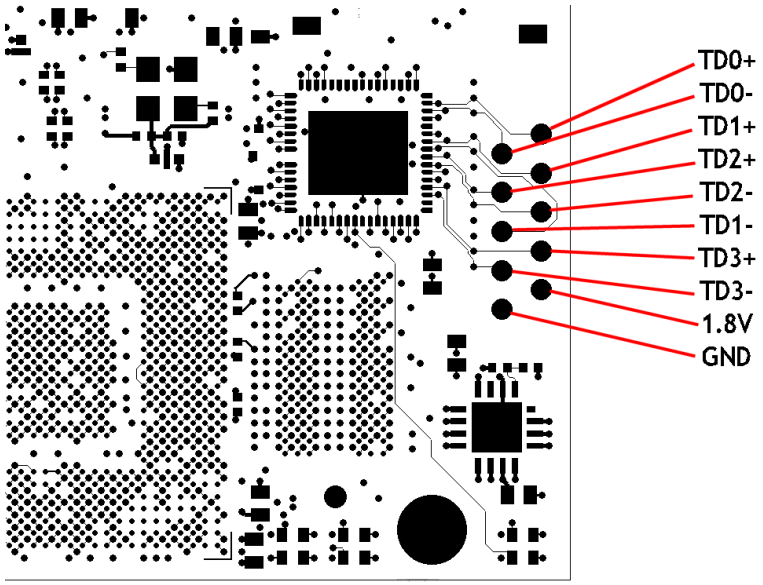
5.2.3 ComPort

A single byte-wide ComPorts is be provided through the primary TIM connector.
An interface within the FPGA translates ComPort traffic into SRIO data. This interface requires 12 FPGA I/O pins.

5.3 Ethernet PHY

A single Ethernet PHY (Marvell 88E1116) is connected to an FPGA MAC.
The DSPs' EMAC interfaces connect directly to the FPGA, and a soft router provides connectivity to the PHY and RJ45 connector/header. [Note: That a full RJ45 connector is not provided, but the signals are presented on a header.]

The pin-out of the Ethernet header is shown here:



There are three EMAC interfaces to the FPGA which requires 39 I/O pins, and a further 2 for the MDC/MDCIO interface.

It is recommended that the SMT562E be used for Ethernet connectivity (http://www.sundance.com/web/files/productpage.asp?STRFilter=SMT562E).

5.4 CPLD

A small Xilinx CPLD is provided which determines the DSPs' configuration after reset.

5.5 DIP Switch

A 4-way DIP switch is used to select module operating modes. These modes include DSP core frequency, and FPGA configuration bit-stream select.

The DIP switch is connected directly to the FPGA. The status of the switch is visible in a read-only register by the DSPs.

5.6 LEDs

Each DSP has direct connection to two LEDs. These are for general purpose use and are driven by the GP(11:10)/CFGGP(1:0) pins.

The FPGA has direct connection to 4 LEDs. These are for general purpose use.

5.7 RSL

The Virtex5FXT device in the FF665 package provides 8 lanes of GTX high-speed serial interfaces. Two are used to connect to the DSPs. The remaining 6 lanes are routed to the RSL connectors. Two lanes to each of the 3 connectors.

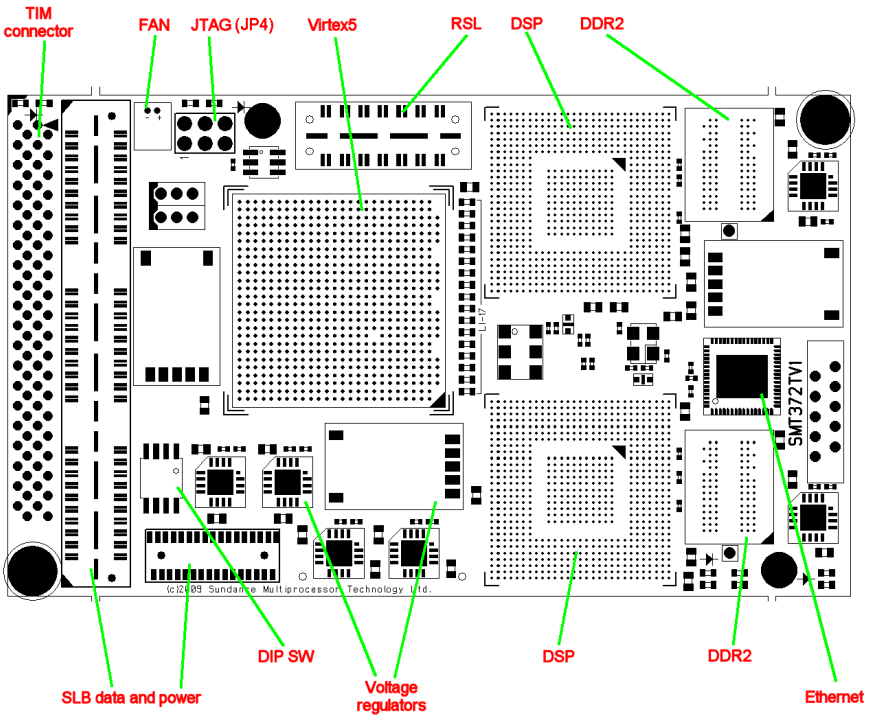
RSL communication can be routed to the DSPs' SRIO, or HPI interfaces.

5.8 Flash

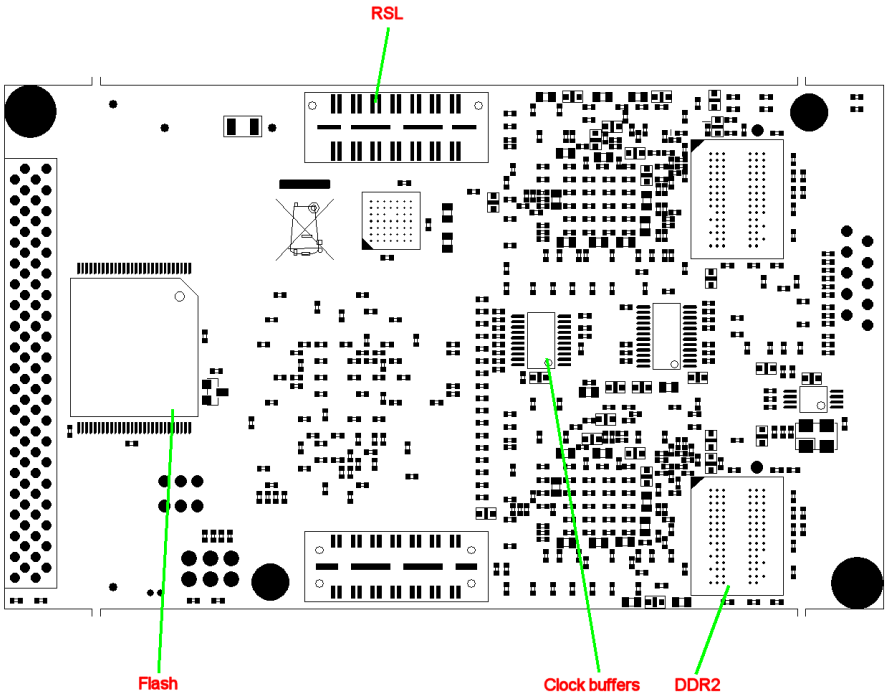
A byte-wide flash of 64M bytes provides storage for the FPGA configuration and DSP application.
The flash cannot be accessed directly from the DSP as the DSP does not have an external parallel memory interface.
Flash access by the DSP is implemented using SRIO or I2C cores within the FPGA.
It is suggested that an area of flash can be reserved to store a default FPGA configuration. This area should not be modified by the user.
[Alternatively, a slow I2C command sequence could be initiated to the FPGA that signals the start of an HPI transfer of data to flash.]

This parallel flash requires 39 FPGA I/O pins.

6 Board Layout



Top view



Bottom view

7 FPGA I/O Allocation

Sub-system	Pin name	Pin count	Instances	Sub-total	Total
SLB	Data	64	1		109
	Control	21			
	Clocks	16			
	Misc	8			
Comm ports	Data	8	1	8	12
	Control	4		4	
Clock	All	3		3	3
Flash	Add	26	1	26	38
	Data	8		8	
	Ctrl	4		4	
UTOPIA	All	25	2	50	50
HPI	All	26	2	52	52
TTL & LEDs	All	8		8	8
TIM Interrupts	NMI/IACK/IIOF/RST	7		7	7
TIM timers	TCLK	2		2	2
DSP Timers	All	3	2	6	6
TIM reset	RESET	1		1	1
DSP reset	RESET	2		2	2
TIM C4x	CONFIG	1		1	1
EMAC	All	13	3	39	39
	Other	2		2	2
DIP Switch	All	4		4	4

8 Support Packages

TBA.

9 Physical Properties

Dimensions (approx.)	4.2”	2.5”

Weight	

Voltage	Current
+12V	TBD
+5V	TBD
+3.3V	TBD
-12V	0

MTBF	

10 Verification, Review & Validation Procedures

To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

11 Safety

This module presents no hazard to the user when in normal use.

12 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.
This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.
Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

13 Ordering Information

SMT372T-30	Virtex5 FX30T.
SMT372T-70	Virtex5 FX70T.