Unit / Module Name:	1GHz DSP Module
Unit / Module Number:	SMT395
Used On:	All TIM carriers, or stand-alone
Document Issue:	1.2
Date:	10/12/2003

CONFIDENTIAL

The SMT395 is Sundance's 4th generation of Texas Instruments 'C6000 DSP TIM (Texas Instruments Module). This module uses the TMS320C6416 DSP which has a clock speed of up to 1GHz, and a 64 bit external data bus.

The module also includes a Xilinx VirtexII-Pro FPGA which is configured to provide 'C4x style Comm ports or alternatively the Sundance Digital Link (SDL), a TIM compatible enhanced global bus, Sundance High-speed Bus (SHB), Sundance RSL (RocketIO) interfaces and other control functions.

All external interfaces (global bus, comm-ports etc) are fully compatible with 5V systems including the C40 based modules and carrier boards.

The SMT395 is, from the user's perspective, a faster version of the SMT335 'C6201 based Module and an improved version of the SMT365.

The SMT395 is supported by the T.I. Code Composer Studio and 3L Diamond RTOS to enable full MultiDSP systems with minimum efforts by the programmers.

Sundance Multiprocessor Technology Ltd, Chiltern House, Waterside, Chesham, Bucks. HP5 1PS.

Revision History

Issue	Changes Made	Date	Initials
1.0	First draft (based on smt365)	22/9/03	GKP
1.1	Updated DSP speed to 1GHz. Updated component placement drawing.	9/12/03	GKP
1.2	Typos and detail corrected. Hyperlinks added.	10/12/03	GKP

Table of Contents

1 Introduction

1.1 Related Documents

TI TMS320C641x data sheet and peripherals guide.

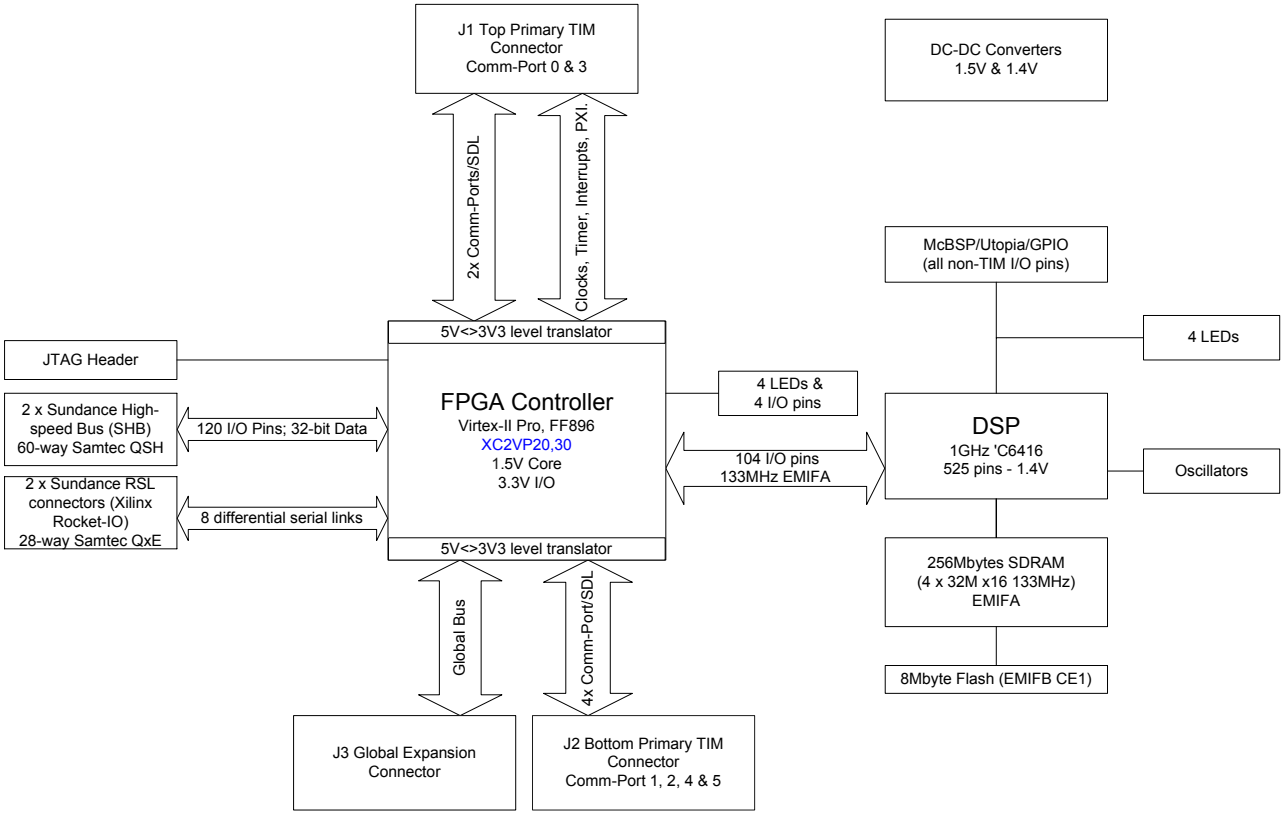
Sundance SHB specification.

Sundance SDB specification.

TI TIM specification & user's guide.

2 Functional Description

2.1 Block Diagram



2.2 Module Description

2.3 Interface Description

2.3.1 Mechanical Interface

This module conforms to the TIM standard for single with modules. It requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards) which must be provided by the two diagonally opposite mounting holes.

2.3.2 Electrical Interface

2.3.2.1 Processor

The module is fitted with a TMS320C6416DSP.

The following table shows the main DSP characteristics.

Feature	C6416
DMA / McBSP / Timer	64/3/3
On-chip memory	1056k bytes
Speed	1GHz
Others	UTOPIA Viterbi and Turbo decoders

The SMT395 implementation using this DSP provides interfaces using the EMIFs (External Memory Interfaces A & B), timers and JTAG.

The JTAG interface is provided to enable application debugging via a suitable JTAG controller and software. Typically, this will be an SMT310 and TI Code Composer Studio. This is an invaluable interface which enables the application programmer to quickly debug a 'chain' of processors in single or multi-processor situations.

The EMIFA is used to connect to a 133MHz, 256Mbyte bank of SDRAM (4 devices of 64M bytes, Samsung K4S511632M-TC75), and the VirtexII-Pro. The flash is connected via EMIFB as a 16 bit device. The EMIFA supplies 4 'chip selects' which are used for these selections. These chip selects provide this basic memory map:

Memory space (EMIFA)	Resource	Address range
	Internal program memory (1M)	0x00000000 - 0x000FFFFF
CE0	SDRAM (256M)	0x80000000 - 0x8FFFFFFF
CE3	Virtex	0xB0000000 - 0xB00FFFFF

Memory space (EMIFB)	Resource	Address range
CE1	8Mbyte flash	0x64000000 – 0x647FFFFF

2.3.2.2 Flash

An 8Mbyte flash memory is provided with direct access by the DSP. This device contains boot code for the DSP and the configuration data for the FPGA.

This is a 16-bit wide device.

The first few k bytes are used for DSP boot code. This is shown in the table below:

Flash Address	Contents
6400 0000 - 6400 1FFF	Boot code.
6400 2000 - 6407 FFFF	FPGA configuration (4M bits)
6408 0000 - 647F FFFF	Application storage.

The flash device can be re-programmed by the DSP at any time. There is a software protection mechanism to stop most errant applications from destroying the device's contents.

Note that the flash memory is connected as a 16 bit device, but during a C6x boot (internal function of the C6x) only the bottom 8 bits are used.

2.3.2.3 Virtex-II Pro (FPGA)

This device, either a Xilinx XC2VP20 or 30, is responsible for the provision of the SHBs, RSLs, 6 comm ports and the global bus. On power-up, this device is un-configured (SRAM based FPGA technology). During the DSP boot process, the FPGA is configured for normal operation.

The standard configuration for the primary FPGA uses approximately 500k gates. The remainder can be used for additional functionality.

Note that the ComPorts and global bus interfaces provided by the FPGA are 5V tolerant and can thus be interfaced with older systems using the 'C40 based modules and TIM carriers.

All of the external interfaces provided by the FPGA are fully described in the External Interface User Manual.

The Sundance High-speed BUS (SHB) specification can be found here.

The SDL specification can be found here.

The RSL specification (Xilinx Rocket IO) can be found here.

2.3.2.3.1 External Clock

An external clock input is provided to the FPGA. This signal is directly connected to the secondary TIM connector user defined pin 12.

2.3.2.4 Power Supplies

This module must have 5V supplied through the TIM connectors. In addition, a 3.3V supply is required and should be supplied through the TIM mounting holes. This is compatible with the SMT320, SMT327 and future Sundance TIM carrier boards.

Contained on the module are linear regulators for the 'C6x and FPGA.

The 'C6x's core voltage is provided through a linear regulator from 3.3V.

All supplies a guaranteed to meet the worst possible requirements of the FPGAs.

3 Verification Procedures

The specification (design requirements) will be tested using the following:

1) Running Code Composer Studio.
2) Running 3L Diamond to test ComPorts and Global bus.
3) SHB loop-back tests.
4) RSL loop-back tests.

4 Review Procedures

Reviews will be carried out as indicated in design quality document QCF14 and in accordance with Sundance's ISO9000-2000 procedures.

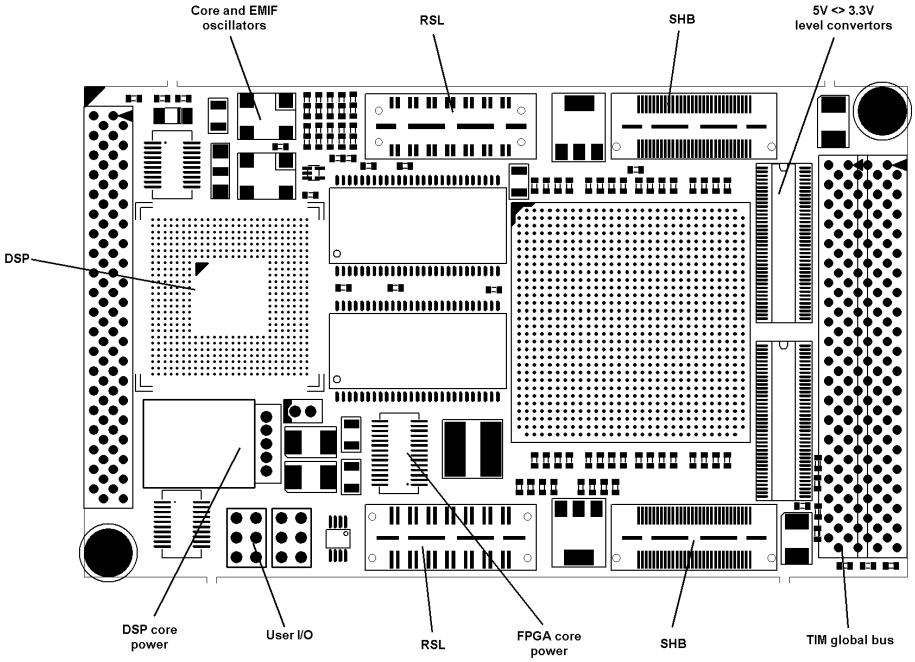
5 Validation Procedures

6 Timing Diagrams

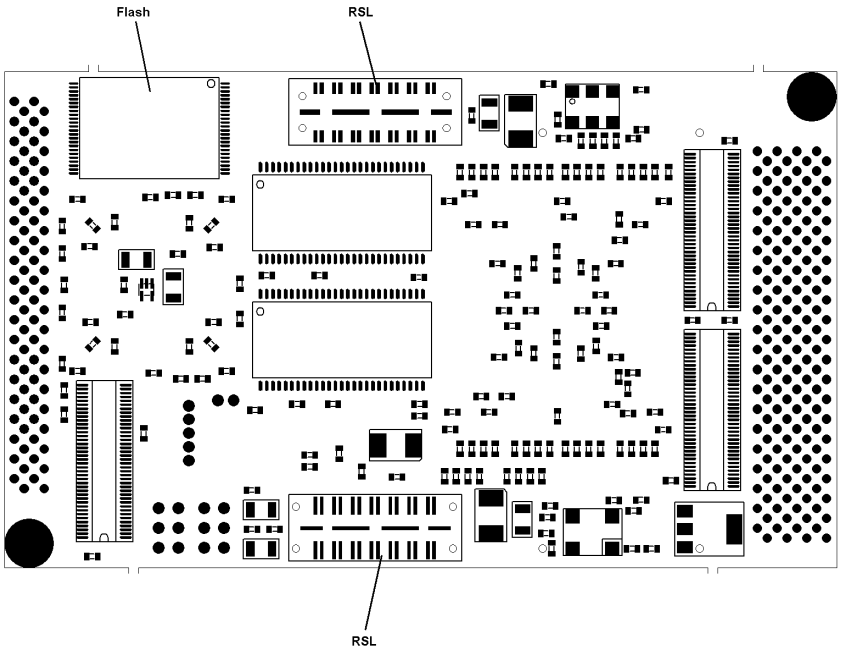
7 Circuit Diagrams

8 PCB Layout Details

8.1 Component Side



8.2 Solder Side



9 Connector Pinouts

The Sundance High-speed BUS (SHB) pinout can be found in this specification.

The RSL pinout (Xilinx Rocket IO) can be found in this specification.

10 VirtexII-Pro Pinout

TBD

11 Safety

This module presents no hazard to the user.

12 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.