

SMT395

User Manual



Certificate Number FM 55022

Revision History

Date	Comments	Engineer	Version
19/04/04	First rev, based on 365	J.V.	1.0.0
26/04/04	Update typos	J.V.	1.1.0
26/05/04	Connector JP1 and JP3 inverted	J.V.	1.1.1
13/08/04	Reference to general firmware updated RSL section added	J.V.	1.1.2
28/09/04	Corrected: CCS 2.0 to CCS 2.20 in section Code Composer (p.16/25)	S.M.	1.1.3
05/04/05	Updated <i>EMIF Control Registers</i> section	JP.A	1.1.4
12/09/05	Added: picture of top view for JP1, JP2, JP3	S.M.	1.1.5
22/09/05	JP1 and JP3 description updated	J.V.	1.1.6
24/11/05	Corrected JPx description	S.M.	1.1.7

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Contacting Sundance

You can contact Sundance for additional information by login onto the support system support.sundance.com

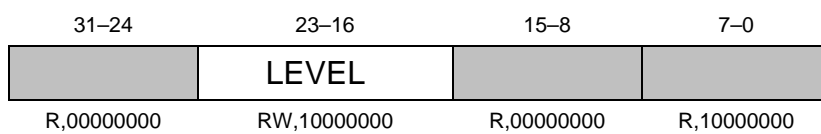
Notational Conventions

C60

The terms C60, C64xx and TMS320C64xx will be used interchangeably throughout this document.

Register Descriptions

The format of registers is described using diagrams of the following form:



The digits at the top of the diagram indicate bit positions within the register and the central section names bits or bit fields. The bottom row describes what may be done to the field and its value after reset. Shaded fields are reserved and should only ever be written with zeroes.

- R Readable by the CPU
- W Writeable by the CPU
- RW Readable and writeable by the CPU

Binary digits indicate the value of the field after reset.

Outline Description

The SMT395 is Sundance's 4th generation of Texas Instruments 'C6000 DSP [TIM](#) (Texas Instruments Module). This module uses the [TMS320C6416](#) DSP which has a clock speed of up to 1GHz, and a 64 bit external data bus.

The module also includes a [Xilinx VirtexII-Pro](#) FPGA which is configured to provide 'C4x style Comm ports or alternatively the [Sundance Digital Link](#) (SDL), a TIM compatible enhanced global bus, [Sundance High-speed Bus](#) (SHB), [Sundance RSL](#) (RocketIO) interfaces and other control functions.

All external interfaces (global bus, ComPorts etc) are fully compatible with 5V systems including the C40 based modules and carrier boards.

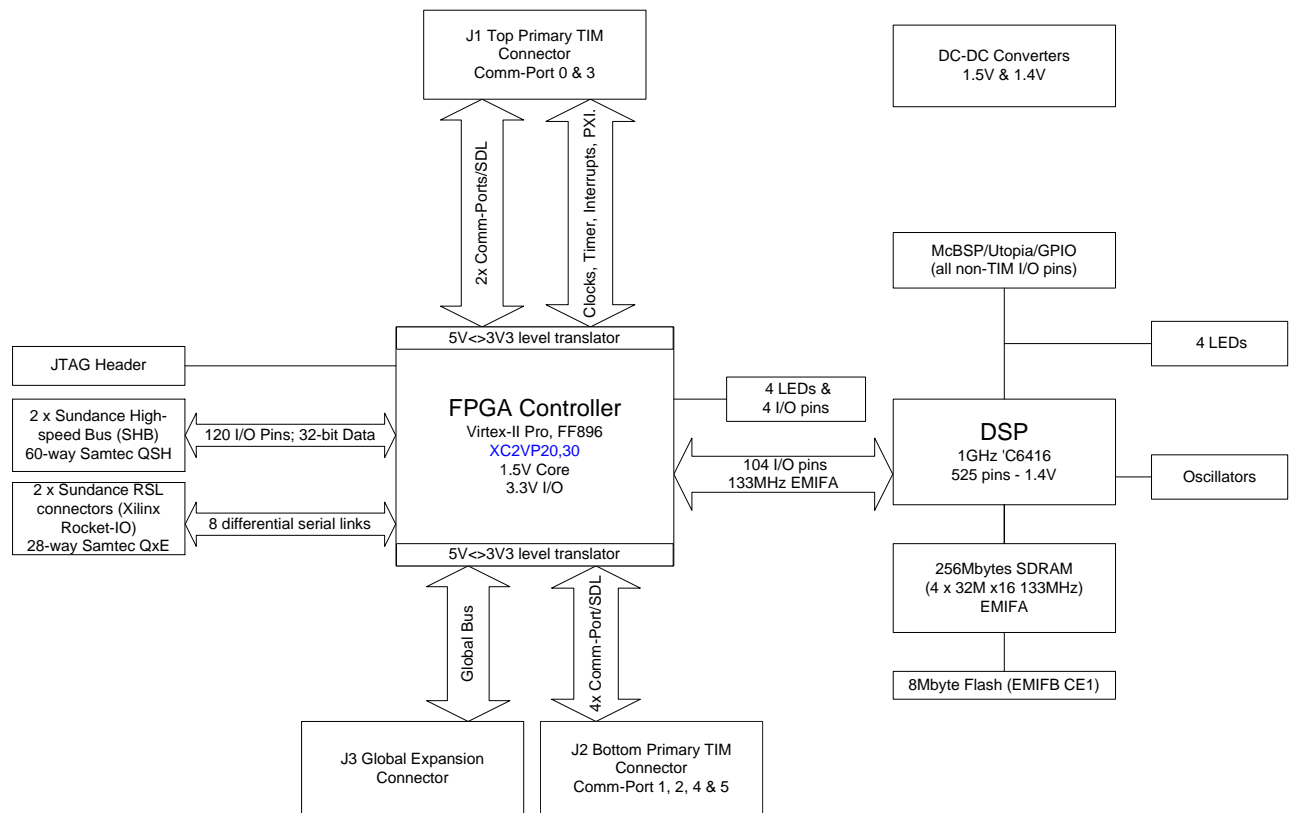
The SMT395 is, from the user's perspective, a faster version of the [SMT335](#) 'C6201 based Module and an improved version of the [SMT365](#).

The SMT395 is supported by the T.I. [Code Composer Studio](#) and [3L Diamond](#) RTOS to enable full MultiDSP systems with minimum efforts by the programmers.

The SMT395 is a C64xx-based size 1 TIM offering the following features:

- ❑ TMS320C6416T processor running at 1GHz
- ❑ Six 20MB/s communication ports (ComPorts)
- ❑ 256MB of SDRAM (133MHz)
- ❑ 8MByte Flash ROM for boot code and FPGA programming
- ❑ Global expansion connector
- ❑ High bandwidth data I/O via 2 Sundance High-speed Buses (SHB)
- ❑ Eight 2.5Gbit/sec Rocket Serial Links (RSL) for intermodule communications
- ❑ 5V tolerant pins

Block Diagram



Architecture Description

The SMT395 TIM consists of a Texas Instruments TMS320C6416T running at up to 1GHz. Modules are populated with 256MBytes of SDRAM.

A Field Programmable Gate Array (FPGA) is used to manage global bus accesses and implement six communication ports and two Sundance High Speed Buses. This is a Xilinx VirtexII-Pro device.

TMS320C6416T

The processor will run with zero wait states from internal SRAM.

An on-board crystal oscillator provides the clock used for the C60, which then multiplies this by 12 internally.

The following table shows the main DSP characteristics.

Feature	C6416T
DMA / McBSP / Timer	64/3/3
On-chip memory	1056k bytes
Speed	1GHz
Others	UTOPIA Viterbi and Turbo decoders

The SMT395 implementation using this DSP provides interfaces using the EMIFs (External Memory Interfaces A & B), timers and JTAG.

The JTAG interface is provided to enable application debugging via a suitable JTAG controller and software. Typically, this will be an [SMT310](#) and TI Code Composer Studio. This is an invaluable interface which enables the application programmer to quickly debug a 'chain' of processors in single or multi-processor situations.

The EMIFA is used to connect to a 133MHz, 256Mbyte bank of SDRAM (4 devices of 64M bytes, Samsung K4S511632M-TC75), and the VirtexII-Pro.

The flash is connected via EMIFB as a 16 bit device. The EMIFA supplies 4 'chip selects' which are used for these selections.

Boot Mode

The SMT395 is configured to boot from flash after a reset

Flash Boot

1. The processor copies a bootstrap program from the first part of the flash memory into internal program RAM starting at address 0.
2. Execution starts at address 0.

The standard bootstrap supplied with the SMT395 then performs the following operations:

1. All relevant C60 internal registers are set to default values;
2. The FPGA is configured from data held in flash memory and sets up the communication ports, the global bus and the Sundance High-speed Buses. This step must have been completed before data can be sent to the ComPorts from external sources such as the host or other TIMs;
3. A C4x-style boot loader is executed. This will continually examine the six communication ports until data appears on one of them. The bootstrap will then load a program in boot format from that port; the loader will not read data arriving on other ports. See "Application Development" for details of the boot loader format;
4. Finally, control is passed to the loaded program.

The delay between the release of the board reset and the FPGA configuration is around 1s for a SMT395.

A typical time to wait after releasing the board reset should be in excess of this delay, but no damage will result if any of the I/Os are used before they are fully configured. In fact, the comm. Ports will just produce a not ready signal when data is attempted to be transferred during this time, and then continue normally after the FPGA is configured.

EMIF Control Registers

The C6416 has two external memory interfaces (EMIFs). One of these is 64 bits wide, the other 16 bits.

The C60 contains several registers that control the external memory interfaces (EMIFs). A full description of these registers can be found in the *C60 Peripherals Reference Guide*[0].

The standard bootstrap will initialise these registers to use the following resources:

Memory space (EMIFA)	Resource	Address range
	Internal program memory (1M)	0x00000000 - 0x000FFFFFF
CE0	SDRAM (256M)	0x80000000 - 0x8FFFFFFF
CE1	Virtex	0x90000000 - 0x900FFFFFF

Memory space (EMIFB)	Resource	Address range
CE1	8Mbyte flash in 4 pages. Page selected with GPIO9 and GPIO10	0x64000000 – 0x641FFFFFF
CE2	Any access asserts FPGA PROG line	0x68000000 – 0x641FFFFFF
CE3	A write programs data bit D0 serially in the FPGA and make a CCLK edge.	0x68000000 – 0x641FFFFFF

The boot code sets-up the EMIF as follows:

GBCTLA = 0x0001277C ;

CECTL0A = 0x000000D0;

CECTL1A = 0x000000A0;

SDCTRLA = 0x6A227000;

CECTL1B = 0xFFFFFFFF13;

CECTL2B = 0xFFFFFFFF23;

CECTL3B = 0x105FFF23;

SDEXTA = 0x00017F3F

SDRAM

256Mbytes of SDRAM is available (4 devices of 64M bytes, Samsung K4S511632M-TC75) The SDRAM operates at EMIF clock speed. It is typically 133MHz for the SMT395.

FLASH

An 8Mbyte flash memory is provided with direct access by the DSP. This device contains boot code for the DSP and the configuration data for the FPGA.

This is a 16-bit wide device.

The flash device can be re-programmed by the DSP at any time. There is a software protection mechanism to stop most errant applications from destroying the device's contents.

Note that the flash memory is connected as a 16 bit device, but during a C6x boot (internal function of the C6x) only the bottom 8 bits are used.

As the C60 only provides 20 address lines on its EMIFB, two GPIO lines (9 and 10) are used to access this device. So the device should be seen as divided in 4x 2MBytes pages.

FLASH Paging

Selecting the visible flash memory page (4 pages of 2Mbytes) involves setting up the GPIO registers bit 9 and 10. Make sure that the setup of the other GPIO is kept untouched as they are used for external interrupt and leds.

Virtex-II Pro FPGA

This device, either a Xilinx XC2VP20 or 30, is responsible for the provision of the SHBs, RSLs, 6 comm ports and the global bus. On power-up, this device is un-configured (SRAM based FPGA technology). During the DSP boot process, the FPGA is configured for normal operation.

The standard configuration for the primary FPGA uses approximately 3800 slices and 128 dual port rams. The remainder can be used for additional functionality.

Note that the ComPorts and global bus interfaces provided by the FPGA are 5V tolerant and can thus be interfaced with older systems using the 'C40 based modules and TIM carriers.

All of the external interfaces provided by the FPGA are fully described in the [SMT6400](#) help file.

The Sundance High-speed BUS (SHB) specification can be found [here](#).

The SDL specification can be found [here](#).

The RSL specification (Xilinx Rocket IO) can be found [here](#).

The FPGA configuration is done in two steps:

First asserting the prog line clears the FPGA configuration. This is simply done by an access in EMIFB CE2.

Then after the FPGA configuration has cleared the FPGA configuration is programmed serially by writing the data from the flash in EMIFB CE3.

At the end of the programming a register is polled to wait until the FPAG is configured and proceed with the application loading process.

External Clock

An external clock input is provided to the FPGA. This signal is directly connected to the secondary TIM connector user defined pin 12.

Version control

Version number for FPGA firmware and boot code is stored in the Flash ROM during programming as zero-terminated ASCII strings. These are displayed when using the SMT6001 utility.

Reprogramming the firmware and boot code

The reprogramming of the module is done using the SMT6001.

It contains the latest boot code and FPGA firmware for it and allows storing a user application in it.

FPGA resources

Interrupts

See [SMT6400 help file](#)

Communication ports

The SMT395 provides 6 ComPorts. They are ComPort 0, 1, 2, 3, 4 and 5.

See [SMT6400 help file](#)

SDB

The SMT395 provides two SHB which are 32-bit SDB.

They are numbered SDB0 for SHBA, SDB1 for SHBB.

See [SMT6400 help file](#)

SDB Clock selection

The SDB clock selection is not implemented. The clock is running at the EMIF speed i.e. 133MHz.

RSL

This interface is still under test. It needs to be standardized across the Sundance module range.

The status so far:

-5 FPGA are limited to 2Gbit/s serial links (see Xilinx datasheet).

-6 FPGA theoretical limit is 3.125Gb/s. This hasn't been verified on the hardware yet.

Tests have been performed with aurora protocol with on-board 100MHz clock. A single lane solution gives around 170MB/s between DSPs. The first tests on the 4 lanes interface have been performed and we are evaluating the best architecture.

The board also includes a differential oscillator (EG-2121CA LV-PECL) for faster speed rate.

The interface is not fixed and not provided yet.

Global bus

The SMT395 provides one global bus interface.

See [SMT6400 help file](#)

CONFIG & NMI

See [SMT6400 help file](#)

Timer

See [SMT6400 help file](#)

IIOF interrupt

The firmware can generate pulses on the external interrupt lines of the TIM.

See [SMT6400 help file](#)

LED

The SMT395 has 7 LEDs.

The LED on the top right corner of the module (above P3 label) always displays the state of the FPGA DONE pin. This LED is off when the FPGA is configured (DONE=1) and on when it is not configured (DONE=0).

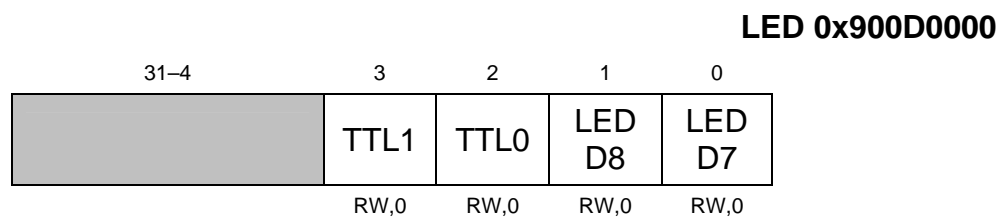
This LED should go on when the board is first powered up and go off when the FPGA has been successfully programmed (this is the standard operation of the boot code resident in the flash memory device). If the LED does not light at power-on, check that you have the mounting pillars and screws fitted properly. If it stays on, the DSP is not booting correctly, or is set to boot in a non-standard way.

Two of the LEDs (D7-D8) can be controlled with the LED register.

Writing 1 will illuminate the LED; writing 0 will turn it off.

Two of the LEDs (D9-D10) can be controlled by the FPGA but their use hasn't been allocated yet.

LED Register



The four remaining LEDs (D11-14) are connected to the C60's GPIO pins 12-15.

TTL

The SMT395 has 4 TTL (TTL0, TTL1, TTL2 and TTL3) signals available on connector JP3.

TTL0 and TTL1 have been mapped in the LED register and TTL2 and TTL3 are left unconnected for future use.

Code Composer

This module is fully compatible with the Code Composer Studio (CCS) debug environment (version 2.20 or later). This extends to both the software and JTAG debugging hardware.

The name of the C64xx CCS device driver is `tixds64xx_11.dvr`, and should be obtained from Texas Instruments. In case of difficulty please ask assistance via our [online support forum](#).

Operating Conditions

Safety

The module presents no hazard to the user.

EMC

The module is designed to operate within an enclosed host system that provides adequate EMC shielding. Operation within the EU EMC guidelines is only guaranteed when the module is installed within an appropriate host system.

The module is protected from damage by fast voltage transients introduced along output cables from outside the host system.

Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.

General Requirements

The module must be fixed to a TIM40-compliant carrier board.

The SMT395 TIM is in a range of modules that must be supplied with a 3.3v power source. In addition to the 5v supply specified in the TIM specification, these new generation modules require an additional 3.3v supply to be presented on the two diagonally-opposite TIM mounting holes. The lack of this 3.3v power supply should not damage the module, although it will obviously be inoperable; prolonged operation under these circumstances is not recommended.

The SMT395 is compatible with all Sundance TIM carrier boards. It is a 5v tolerant module, and as such, it may be used in mixed systems with older TIM modules, carrier boards and I/O modules.

Use of the TIM on SMT327 (cPCI) motherboards may require a firmware upgrade. If the top right LED on the SMT395 remains illuminated once the TIM is plugged in and powered up, the SMT327 needs the upgrade. The latest firmware is supplied with all new boards shipped. Please contact Sundance directly if you have an older board and need the upgrade.

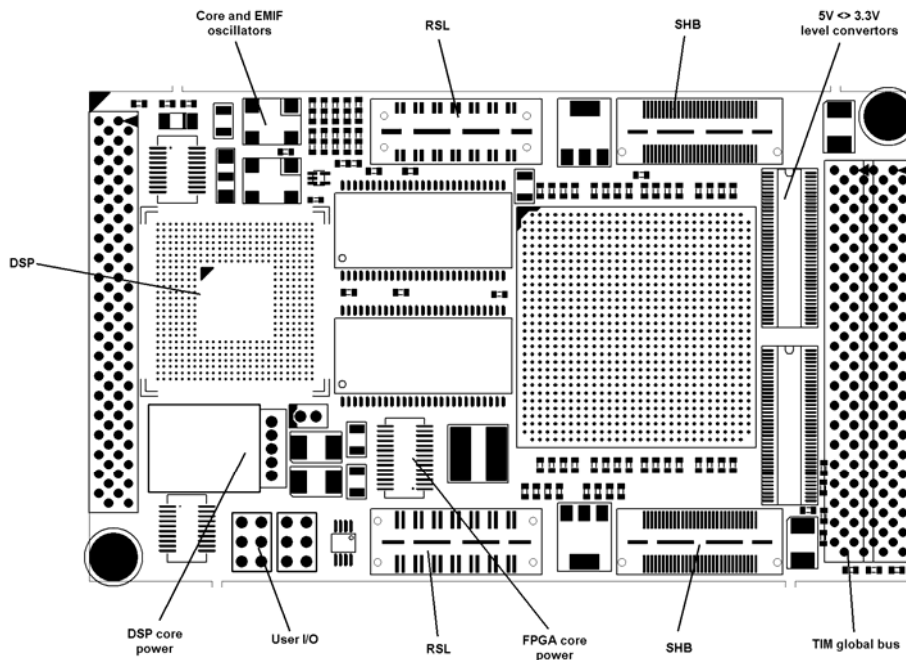
The external ambient temperature must remain between 0°C and 40°C, and the relative humidity must not exceed 95% (non-condensing).

Power Consumption

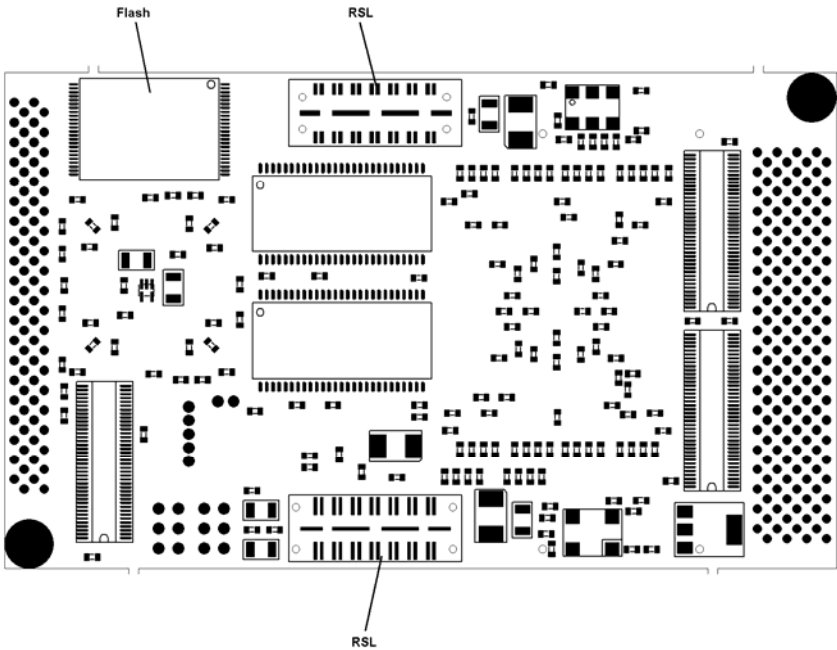
The power consumption of this TIM is dependent on the operating conditions in terms of core activity and I/O activity. The maximum power consumption is 10W.

PCB description

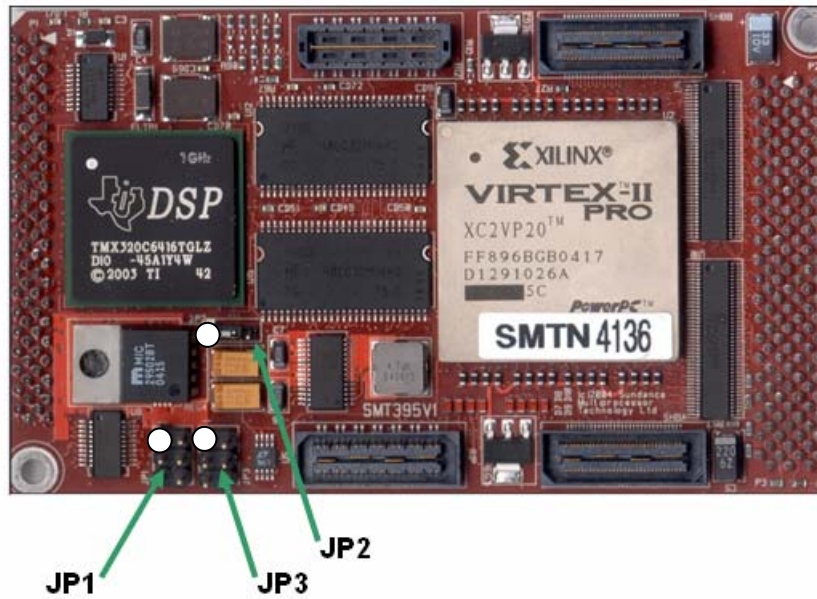
Component Side



Solder Side



Connector Pinouts



FPGA JTAG (JP1)

The following shows the pin-outs for JP1 (FPGA) JTAG connector:

Signal	Pin	Pin	Signal
V33	1	4	TDI
TMS	2	5	TDO
TCK	3	6	GND

Note: The Pin 1 is marked by a white mark on the silkscreen (see white spot on the previous picture).

FPGA PROG Pin Control (JP2)

The FPGA PROG pin is used to clear the FPGA configuration.

It is to be used as a safety in case the FPGA has been programmed with a bad bitstream that corrupts the dsp external bus and prevents which any further programming. Changing the jumper allows the user to clear the FPGA configuration and reprogram the FPGA.

1-2	PROG under control of DSP
2-3 or out	PROG asserted

Note: The Pin 1 is marked by a white mark on the silkscreen (see white spot on the previous picture).

TTL (JP3)


The following shows the pin-outs for JP3 TTL connector:

Signal	Pin	Pin	Signal
V33	1	4	TTL2
TTL0	2	5	TTL3
TTL1	3	6	GND

Note: The Pin 1 is marked by a white mark on the silkscreen (see white spot on the previous picture).

SHB pin-out

Pin	Signal	Signal	Pin
1	SHB_CLK	SHB_D0	2
3	SHB_D1	SHB_D2	4
5	SHBL_D3	SHB_D4	6
7	SHB_D5	SHB_D6	8
9	SHB_D7	SHB_D8	10
11	SHB_D9	SHB_D10	12
13	SHB_D11	SHB_D12	14
15	SHB_D13	SH_D14	16
17	SHB_D15	SHB_U0	18
19	SHB_U1	-	20
21	-	SHB_WEN	22
23	SHB_REQ	SHB_ACK	24
25	-	-	26
27	-	-	28
29	-	-	30
31	-	-	32
33	-	-	34
35	-	-	36
37	SHB_CLK	SHB_D16	38
39	SHB_D17	SHB_D18	40
41	SHB_D19	SHB_D20	42
43	SHB_D21	SHB_D22	44
45	SHB_D23	SHB_D24	46
47	SHB_D25	SHB_D26	48
49	SHB_D27	SHB_D28	50
51	SHB_D29	SHB_D30	52
53	SHB_D31	SHB_U0	54
55	SHB_U1	-	56
57	-	SHB_WEN	58
59	SHB_REQ	SHB_ACK	60

 Not implemented

RSL pin-out

The RSL pinout (Xilinx Rocket IO) can be found in this [specification](#).

The board has 4 RSL pairs per connectors (8 Links).

Virtex Memory Map

See general firmware description.

The memory mapping is as follows:

```
#define CP0                (volatile unsigned int *)0x90000000
#define CP1                (volatile unsigned int *)0x90008000
#define CP2                (volatile unsigned int *)0x90010000
#define CP3                (volatile unsigned int *)0x90018000
#define CP4                (volatile unsigned int *)0x90020000
#define CP5                (volatile unsigned int *)0x90028000
#define CP0_STAT          (volatile unsigned int *)0x90004000
#define CP1_STAT          (volatile unsigned int *)0x9000C000
#define CP2_STAT          (volatile unsigned int *)0x90014000
#define CP3_STAT          (volatile unsigned int *)0x9001C000
#define CP4_STAT          (volatile unsigned int *)0x90024000
#define CP5_STAT          (volatile unsigned int *)0x9002C000
#define GB_STAT           (volatile unsigned int *)0x90034000
#define SDB_STAT         (volatile unsigned int *)0x90038000
#define STAT              (volatile unsigned int *)0x9003C000
#define SDBA              (volatile unsigned int *)0x90040000
#define SDBB              (volatile unsigned int *)0x90050000
#define SDBC              (volatile unsigned int *)0x90060000
#define SDBD              (volatile unsigned int *)0x90070000
#define SDBA_STAT        (volatile unsigned int *)0x90048000
#define SDBB_STAT        (volatile unsigned int *)0x90058000
#define SDBA_INPUTFLAG   (volatile unsigned int *)0x90044000
#define SDBB_INPUTFLAG   (volatile unsigned int *)0x90054000
#define SDBA_OUTPUTFLAG  (volatile unsigned int *)0x9004C000
#define SDBB_OUTPUTFLAG  (volatile unsigned int *)0x9005C000
#define GLOBAL_BUS       (volatile unsigned int *)0x900A0000
#define GLOBAL_BUS_CTRL  (volatile unsigned int *)0x90080000
#define GLOBAL_BUS_START (volatile unsigned int *)0x90088000
#define GLOBAL_BUS_LENGTH (volatile unsigned int *)0x90090000
#define TCLK              (volatile unsigned int *)0x900C0000
#define TIMCONFIG         (volatile unsigned int *)0x900C8000
#define LED               (volatile unsigned int *)0x900D0000
#define INTCTRL4         (volatile unsigned int *)0x900E0000
```

```
#define INTCTRL4_EXT      (volatile unsigned int *)0x900E4000
#define INTCTRL5         (volatile unsigned int *)0x900E8000
#define INTCTRL5_EXT     (volatile unsigned int *)0x900EC000
#define INTCTRL6         (volatile unsigned int *)0x900F0000
#define INTCTRL6_EXT     (volatile unsigned int *)0x900F4000
#define INTCTRL7         (volatile unsigned int *)0x900F8000
#define INTCTRL7_EXT     (volatile unsigned int *)0x900FC000
```


FPGA Pin-Out

See board schematics.

Bibliography

1. Peripherals Reference Guide (literature number SPRU190)
<http://www.ti.com/>
Describes common peripherals available on the TMS320C6x digital signal processors. This book includes information on the internal data and program memories, the external memory interface (EMIF), the host port, multichannel-buffered serial ports, direct memory access (DMA), clocking and phase-locked loop (PLL), and the power-down modes.
2. TIM-40 MODULE SPECIFICATION Including TMS320C44 Addendum
ftp://ftp2.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf
3. SDB Technical Specification
ftp://ftp2.sundance.com/Pub/documentation/pdf-files/sdb_tech_spec.pdf
4. SHB Technical Specification
ftp://ftp2.sundance.com/Pub/documentation/pdf-files/SHB_Technical_Specification_v1_0.pdf
5. TMS320C4x User's Guide (literature number SPRU063)
<http://www-s.ti.com/sc/psheets/spru063c/spru063c.pdf>
Describes the C4x 32-bit floating-point processor, developed for digital signal processing as well as parallel processing applications. Covered are its architecture, internal register structure, instruction set, pipeline, specifications, and operation of its six DMA channels and six communication ports. Software and hardware applications are included.
6. Xilinx Virtex-II Pro data sheet:
<http://www.xilinx.com/>
7. General firmware description:
ftp://ftp2.sundance.com/Pub/documentation/pdf-files/External_Interface_User_manual.pdf

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