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| **Unit / Module Name:** | |
| **Unit / Module Number:** | SMT395E |
| **Used On:** | |
| **Document Issue:** | 1.1 |
| **Date:** | 22nd February 2005 |

# CONFIDENTIAL

The SMT395E is Sundance's 4th generation of Texas Instruments 'C6x DSP TIM (Texas Instruments Module). This module uses the TMS320C641x DSP which has a clock speed of 1GHz, and a 64 bit external data bus.

The module also includes a Xilinx VirtexII-Pro FPGA which is configured to provide 'C4x style Comm ports or alternatively the Sundance Digital Link (SDL), a TIM compatible enhanced global bus, Sundance High-speed Bus (SHB), Sundance RSL (RocketIO) interfaces and other control functions.

The SMT395E is supported by the T.I. Code Composer Studio and 3L Diamond RTOS to enable full MultiDSP systems with minimum efforts by the programmers.

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# Revision History

| Issue | Changes Made | Date | Initials |
|---|---|---|---|
| 1.0 | First draft (based on smt395) | 12/8/04 | GKP |
| 1.1 | Major revision | 11/2/05 | GKP |
| | | | |

# Table of Contents

# 1 Introduction

## 1.1 Related Documents

TI TMS320C641x data sheet and peripherals guide.

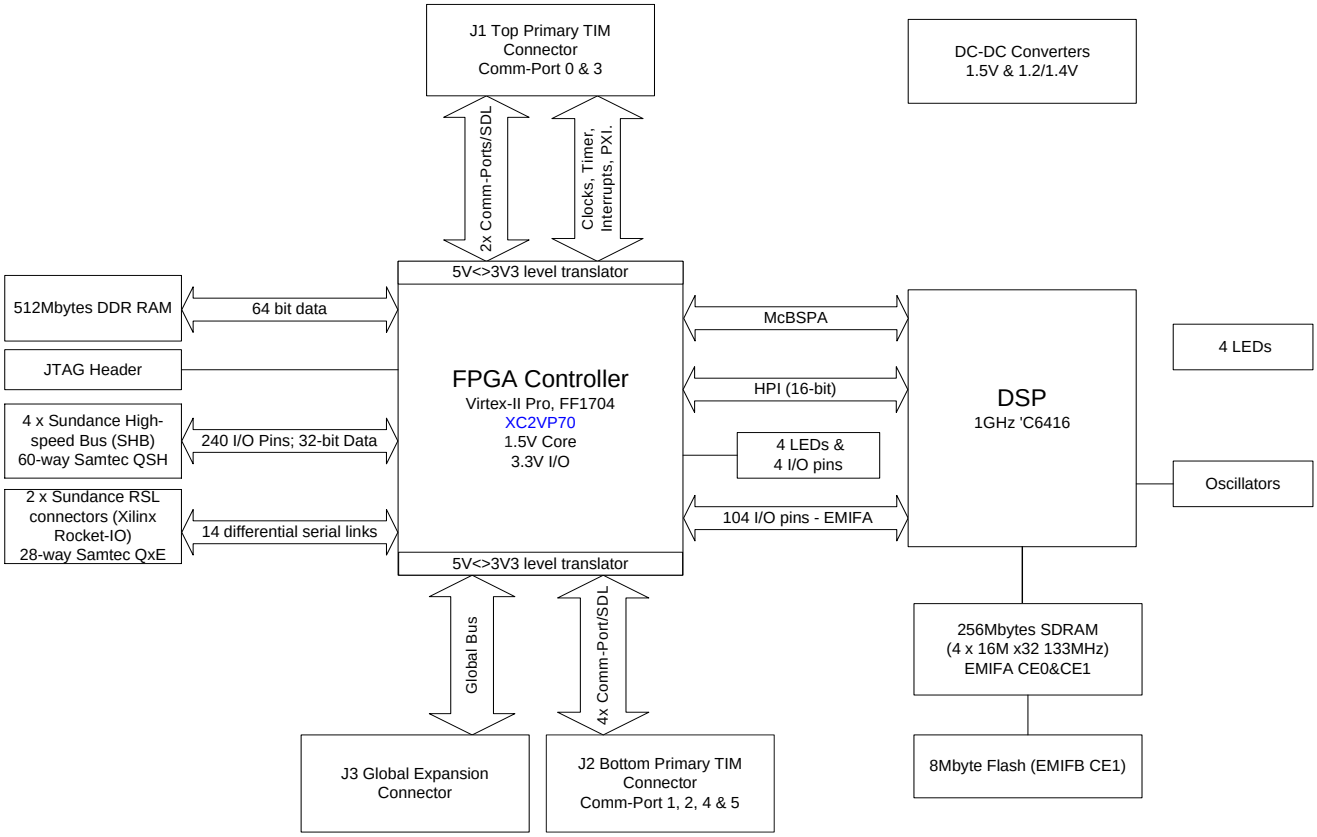
Sundance SHB specification.

Sundance SDB specification.

TI TIM specification & user's guide.

# 2 Functional Description

## 2.1 Block Diagram



## 2.2 Module Description

## 2.3 Interface Description

### 2.3.1 Mechanical Interface

This module conforms to the TIM standard for single with modules. It requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards) which must be provided by the two diagonally opposite mounting holes.

### 2.3.2 Electrical Interface

#### 2.3.2.1 Processor

The module is fitted with a TMS320C6416DSP.

The following table shows the main DSP characteristics.

| Feature | C6416 |
|---|---|
| DMA / McBSP / Timer | 64/3/3 |
| On-chip memory | 1056k bytes |
| Speed | 1GHz |

The SMT395E implementation using this DSP provides interfaces using the EMIFs (External Memory Interfaces A & B), timers and JTAG.

The JTAG interface is provided to enable application debugging via a suitable JTAG controller and software. Typically, this will be an SMT310 and TI Code Composer Studio. This is an invaluable interface which enables the application programmer to quickly debug a ‘chain’ of processors in single or multi-processor situations.

#### 2.3.2.1.1 EMIFA

The EMIFA is used to connect a 512Mbyte bank of SDRAM (8 devices of 64M bytes), and the VirtexII-Pro. The flash is connected via EMIFB as a 16 bit device. The EMIFA supplies 4 'chip selects' which are used for these selections. These chip selects provide this basic memory map:

| Memory space (EMIFA) | Resource | Address range |
|---|---|---|
| | Internal program memory (1M) | 0x00000000 - 0x000FFFFF |
| CE0 | SDRAM (128M) | 0x80000000 - 0x8FFFFFFF |
| CE1 | SDRAM (128M) | 0x90000000 - 0x9FFFFFFF |
| CE3 | Virtex | 0xB0000000 - 0xB00FFFFF |

| Memory space (EMIFB) | Resource | Address range |
|---|---|---|
| CE1 | 8Mbyte flash | 0x64000000 – 0x647FFFFF |

#### 2.3.2.1.2 Host Port Interface (HPI)

The HPI is connected (via a 16 bit data bus) directly to the FPGA.

#### 2.3.2.1.3 McBSP

A single McBSP is connected directly to the FPGA.

### 2.3.2.2 Flash

One 8Mbyte flash memory is provided with direct access by the DSP. This contains boot code for the DSP and the configuration data for the FPGA.

It is a16-bit wide devices.

The flash device can be re-programmed by the DSP at any time. There is a software protection mechanism to stop most errant applications from destroying the device's contents.

Note that the flash memory is connected as a 16 bit device, but during a C6x boot (internal function of the C6x) only the bottom 8 bits are used.

#### 2.3.2.3 Virtex-II Pro (FPGA)

This device, a Xilinx XC2VP70, is responsible for the provision of the SHBs, RSLs, 6 comm ports and the global bus. On power-up, this device is un-configured (SRAM based FPGA technology). During the DSP boot process, the FPGA is configured for normal operation.

The standard configuration for the primary FPGA uses approximately 500k gates. The remainder can be used for additional functionality.

Note that the ComPorts and global bus interfaces provided by the FPGA are NOT 5V tolerant and can thus NOT be interfaced with older systems using the 'C40 based modules and TIM carriers.

##### 2.3.2.3.1 ComPorts

These communication links follow Texas Instrument C4x standard. They are 8-bit parallel inter-processor ports of the 'C4x processors.

The 395E follows the C40 TIM standard and as such provides 6 links. These are given the numbers 0, 1, 2, 3, 4 and 5.

A connection can only be established between comm-ports with a different reset state. On each TIM the links 0, 1 and 2 are set to transmit at reset and the links 3, 4 and 5 are set to receive at reset. Never connect two comm-ports of the same category together.

| Always connect any one of comm-port 0, 1, 2 to any one of comm-port 3, 4, 5. |
|---|

The transfer can start in any direction.

Additional information on the standard is available in the TMS320C4x User's Guide chapter 12: Communication ports and the Texas Instrument Module Specification.

Each of the comm ports is associated with two 16x32 bit unidirectional FIFOs (input and output) to be able to maintain a maximum bandwidth and to enable parallel transfer. They are guaranteed for a transfer rate of 20MB/s, which could lead, using the 6 comm ports available to a 120MB/s transfer rate.

##### 2.3.2.3.2 SHB

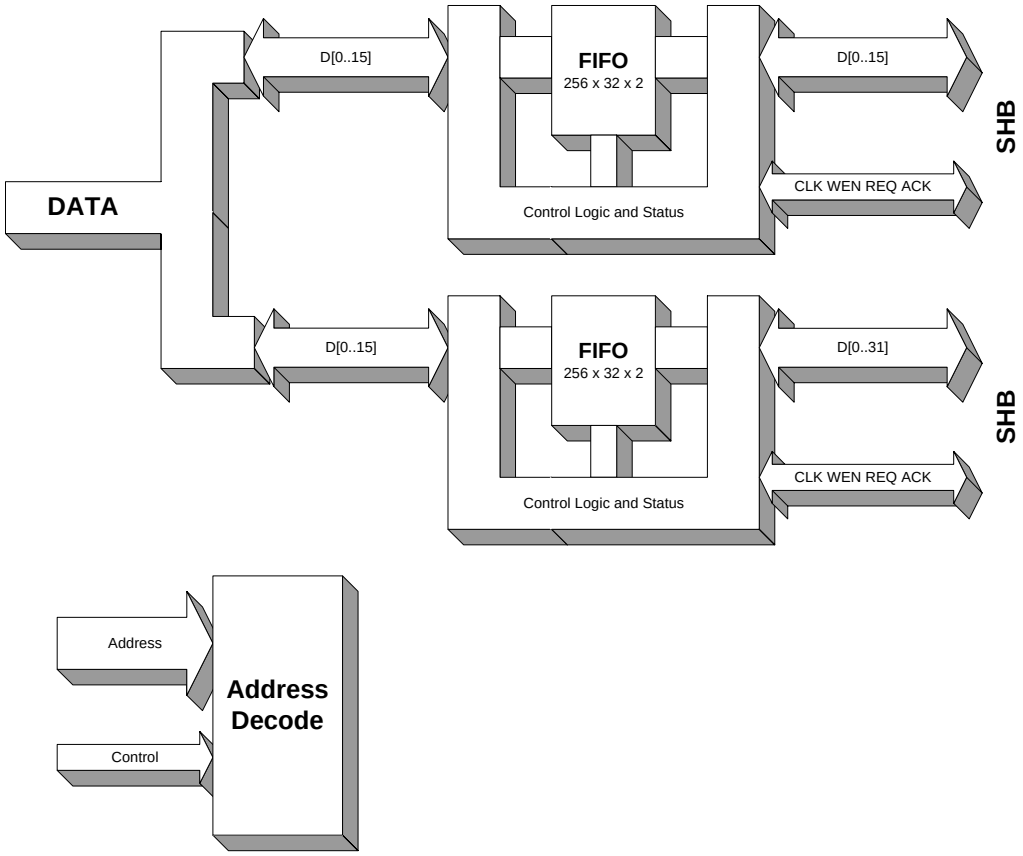
The SHB communication link (standard core) is 16 bits but can run at up to 200MHz. The SHB connector pin-out defines other bus widths (8 and 32) and also enables the use of several buses using the same connector.

The SMT395E includes two Sundance High-speed Buses (SHB). These are connected directly to the Virtex-II Pro device. Each SHB connector can support a 32 bit and two 16 bit SHBs so, by running both buses together a data rate of 1.2Gbytes/s is achieved. All signal pins of the SHB connector are routed to the Virtex-II Pro.

This SHB high-speed data transfer can be achieved thanks to the use of a 60-way flat micro-coax ribbon cable (Ref. SMT3xx-SHB-CAB).

The SHBs integrate two 256 words deep unidirectional FIFO (input and output).

Both the SHBs drive at 3.3v signal levels.


DATA
D[0..15]
FIFO
256 x 32 x 2
D[0..15]
CLK WEN REQ ACK
Control Logic and Status
SHB
D[0..15]
FIFO
256 x 32 x 2
D[0..31]
CLK WEN REQ ACK
Control Logic and Status
SHB


Address
Control
Address Decode

#### 2.3.2.3.3 Global bus

The global bus is compatible with the TIM standard.

A global bus start address register needs to be programmed, together with a transfer length. When the length register has been set, the Virtex device will automatically perform the requested transfer between the global bus and a dual port memory (DPR).

The C64 has direct random access to a 256x32 dual port RAM (DPR) located in the FPGA. The other port of this RAM is addressed by an 8 bit binary counter (GBFA[7:0]).

In order to initiate a global bus transfer the following procedure is needed;

1 The C60 writes data to the DPR (if the access is to be a write).

2 The global bus start address is loaded.

3 The transfer size is loaded.

4 At the end of the transfer an interrupt is generated.

The global bus start address is loaded into a 31-bit counter. For each word of the transfer this counter is incremented.

When the transfer size is loaded, the DPR counter (GBFA) is reset to zero. This counter value is compared with the transfer size register. If the two values are different, then global bus accesses are performed.

If a write is performed the DSP needs to store the data to send in the RAM. The bottom 8 address lines are used (A9:A2) (this gives random access to the RAM).

The type of global bus operation is included within bit 8 of the word setting the transfer count amount. The write operation to this register starts the transfer.

### 2.3.2.4 Power Supplies

This module must have 5V supplied through the TIM connectors. In addition, a 3.3V supply is required and should be supplied through the TIM mounting holes. This is compatible with the SMT310/Q, SMT327 and future Sundance TIM carrier boards.

Contained on the module are linear regulators for the ‘C6x and FPGA.

The ‘C6x’s core voltage is provided through a linear regulator from 3.3V.

All supplies a guaranteed to meet the worst possible requirements of the FPGAs.

# 3 Verification Procedures

The specification (design requirements) will be tested using the following:

1) Running Code Composer
2) Running 3L Diamond
3) SHB and RSL loop-back tests
4) DSP and FPGA memory tests

# 4 Review Procedures

Reviews will be carried out as indicated in design quality document QCF14 and in accordance with Sundance's ISO9000 procedures.

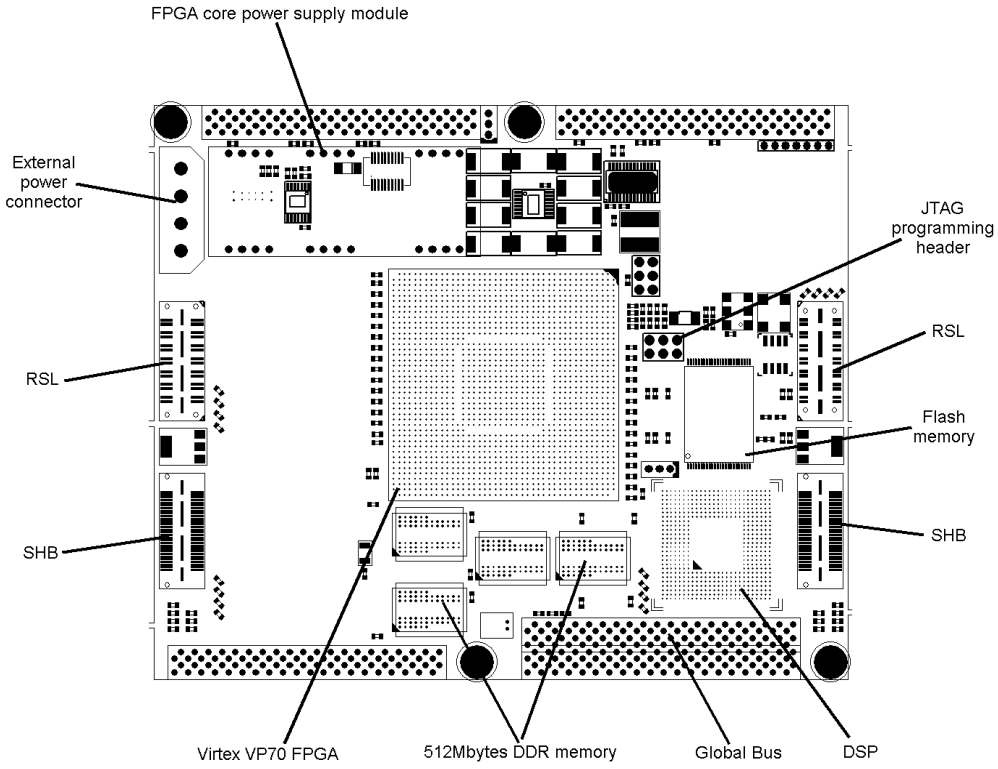
# 5 Validation Procedures

# 6 Timing Diagrams

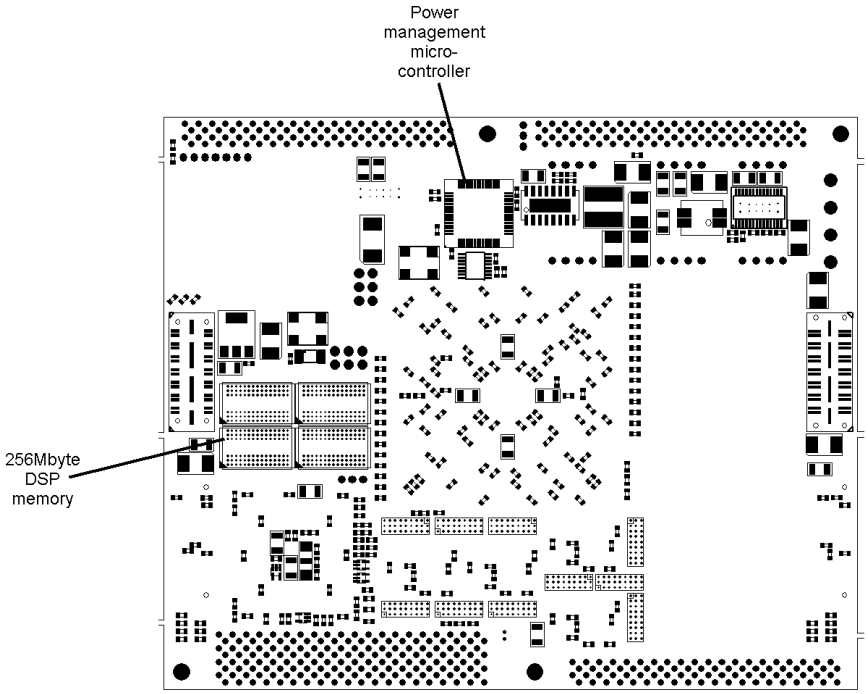
# 7 Circuit Diagrams

# 8 PCB Layout Details

## 8.1 Component Side




## 8.2 Solder Side



# 9 Pinout and Package Requirements

## Virtex-II Pro Pin-Out

TBD

## 10 Safety

This module presents no hazard to the user.

## 11 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.