USER GUIDE

FOR

SMT417

Note:

If this copy is no longer in use, return to sender.

APPROVAL PAGE

Name	Signature	Date
Managing Director		
Software Manager		
Design Engineer		

AUTHOR/S

Name	Signature	Date

DOCUMENT HISTORY

Date	Changes Made	Issue	Initials
14-Feb-07	Consolidated from Design Specification, work-in-progress.	0.1	BV
25-Feb-07	Complete Draft Revision, for internal review	0.2	BV
27-Feb-07	Repair issues in .pdf translation, fix some cross-references, update ordering information section	0.3	BV

LIST OF ABBREVIATIONS

Abbreviation	Explanation
ASIC	Application Specific Integrated Circuit
CMC	Common Mezzanine Card
CP	Communications Port
DSP	Digital Signal Processor
FMS	Trade name for a flat-ribbon cable family from JST Mfg. Inc.
FPGA	Field Programmable Gate Array
NA	Not Applicable
OTP	One-Time Programmable
PC	Personal Computer
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PMC	PCI Mezzanine Card
PrPMC	Processor PMC
RF	Radio Frequency
RSL	RocketIO Serial Link
SDB	Sundance Digital Bus
SDRAM	Synchronous Dynamic Random Access Memory
SHB	Sundance High-speed Bus
SMA	Trade name for a threaded RF co-axial connector family
SMT	Sundance Multiprocessor Technology, LTD.
TBD	To Be Determined
TI	Texas Instruments
XMC	Switched Mezzanine Card

TABLE OF CONTENTS

TABLE OF FIGURES and TABLES

1. INTRODUCTION

1.1. OVERVIEW

This document describes the features and operations of a PMC module with two fixed-point DSPs, one large FPGA, and several external I/O interfaces.

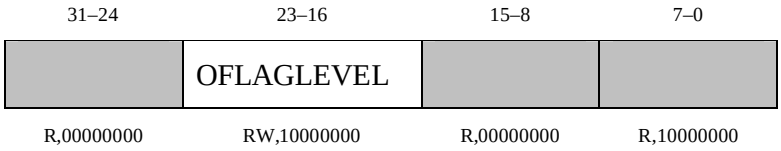
1.2. NOTATIONAL CONVENTIONS

DSP

The term DSP will be used throughout this document in place of TMS320C6416T.

Register Descriptions

The format of registers is described using diagrams of the following form:



The digits at the top of the diagram indicate bit positions within the register and the central section names bits or bit fields. The bottom row describes what may be done to the field and its value after reset. Shaded fields are reserved and should only ever be written with zeroes.

R	Readable by the CPU
W	Writeable by the CPU
RW	Readable and writeable by the CPU
W1TC	Write 1 to Clear
	Binary digits indicate the value of the field after reset

1.3. INTENDED AUDIENCE

This document describes all interfaces available based on the design specification of the SMT417. SMT417 boards with the following PCB versions have the following restrictions:

PCB	Markings	QL/CD Version	Restrictions
V1	Red Solder Mask, Merix Label	N/A	No PMC/PCI, No XMC (stand-alone use only)
V2	Green Solder Mask, Sierra Label	0xB0102	No XMC, CPLD bit swizzle required

1.4. RELATED DOCUMENTS

[1] PCI **M**ezzanine **C**ard (*PMC*) Specification – IEEE 1386-2001.

http://standards.ieee.org/reading/ieee/std/busarch/1386-2001_and_1386.1-2001.pdf

[2] Sundance **H**igh-speed **B**us (*SHB*) Specification – Sundance.

http://sundance.com/docs/SHB%20Technical%20Specification.pdf

[3] External Interface User Manual – Sundance.

http://sundance.com/docs/Firmware.pdf

[4] Rocket **S**erial **L**ink (*RSL*) Specification – Sundance.

http://www.sundance.com/docs/Specification_RSL.pdf

[5] Processor **PMC** (PrPMC) Specification – VITA 32.

http://www.vita.com/specifications.html

[6] (FMS) Specification - Sundance

ftp://ftp2.sundance.com/Pub/documentation/pdf-files/comm-port.pdf

[7] Switched **M**ezzanine **C**ard (XMC) Specification- VITA 42

http://www.vita.com/specifications.html

2. BLOCK DIAGRAM

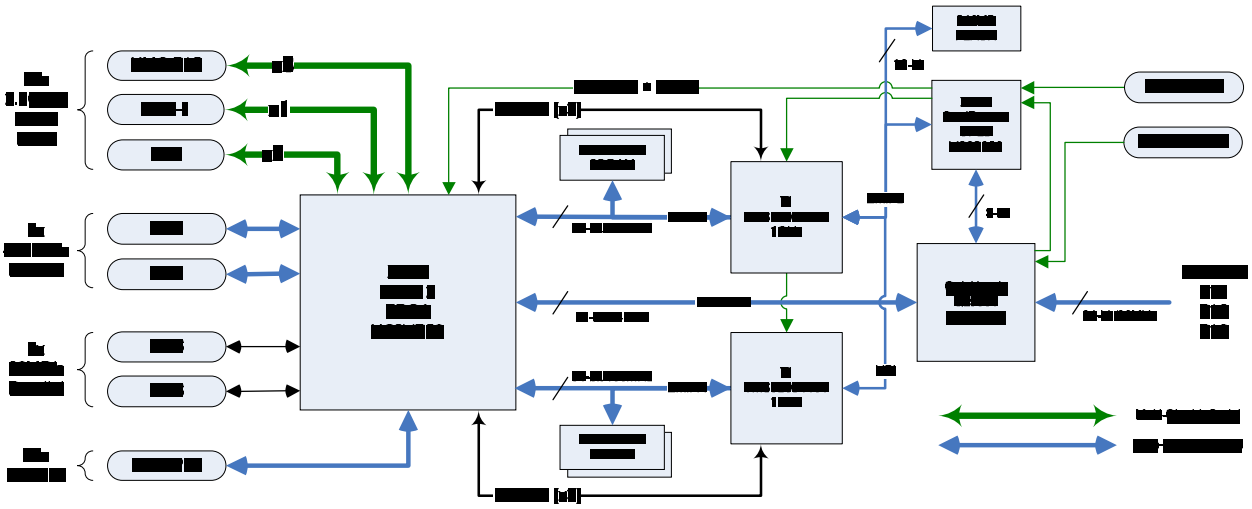


Figure 1 - Block diagram of the SMT417.

The SMT417 enables hybrid DSP/FPGA computation on digital data acquired from PCI, SHB or RSL interfaces while conforming to a single-sized PMC form factor.

2.1. FEATURES

The main features of the *SMT417* are listed below:

§ Two TI 6416T DSPs with independent SDRAM

§ Xilinx Virtex II Pro (FF1152 package)

§ Provision for data processing in FPGA

§ One XMC connector with 8 RSL data links

§ Two FMS connectors

§ Standard single-size PMC module

§ 66MHz 64-bit PCI interface with over 500MB/s data rate

§ Standard Sundance software interface

Additional features meeting ANSI/VITA 32 (PrPMC) spec for tall modules:

§ Two SHB *AND* one RSL (7x bidirectional RocketIO) interface for easy interconnection to Sundance products.

§ One (1x bidirectional RocketIO) to a Samtec GRF1-J connector for interfacing to Xilinx RocketIO connectivity boards and other custom multi-gigabit serial interface hardware.

3. MECHANICAL INTERFACES

3.1. PMC

PMC is a variant of CMC that uses PCI to communicate over the backplane. The IEEE CMC standard describes both single- and double-size mezzanine cards. The SMT417 is a single-size card.

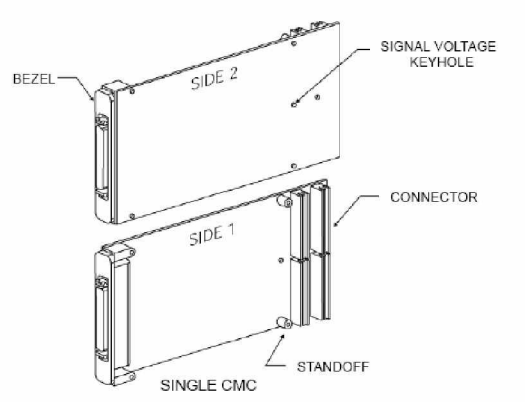


Figure 2 - Single-size PMC card (from IEEE *1386-2001*)

Dimensions of the single-size CMC are 74.0mm wide by 149.0mm deep. *Note that the SMT417 does not provide any front panel connectors or ports, as per the ANSI/VITA 20 (conduction cooled specification).*

3.1.1. Voltage keying

The QuickLogic QL5064 bridge is both 3.3V and 5V compliant. Both keying holes are provided. *Note that the SMT417 requires **both** 3.3V and 5V power to function.*

3.1.2. Connectors

P11 through P13 are required for 64-bit PCI connectivity. Connector P14 is provided for 64 user-defined I/O.

3.1.3. Component Height

Heights of components on PMC Side 1 (see Figure 2) are limited to 4.7mm except in the I/O Area (where they may extend to the host module surface). Components on PMC Side 2 are limited to 3.5mm minus PCB thickness, or about 2.0mm (assuming 1.5mm PCB thickness).

The SMT417 has build options which place certain external I/O connectors onto Side 2. When ordered in this way, the SMT417 conforms to ANSI/VITA 32 (PrPMC), which allows 10mm to 20mm of height above the PCB for components on Side 2.

3.1.4. Power Consumption

Based on the IEEE 1386-2001 specification, the total consumption for Side 1 and Side 2 of the module shall not exceed 7.5W. Depending on the operating frequency and user-defined FPGA designs implemented, the SMT417 is easily capable of exceeding the recommended power dissipation limits. Careful planning at both the software and firmware levels is required when integrating the SMT417 into end-user systems.

3.1.5. Cooling

The SMT417 is designed to be used with conduction-cooled PMC carriers and systems. The specifications governing this are defined by ANSI/VITA 20-2001. The specification defines certain areas on the PMC board to be reserved free of components, to contain significant amounts of metal for thermal conductivity and to provide numerous through-hole terminals for attaching thermal and stiffening components.

3.1.6. Grounding

Per section 4.14 of IEEE 1386-2001.

3.1.7. PMC JTAG

The ANSI/VITA 42 specification governs how the JTAG signals are to be treated. The SMT417 does not attach any devices to the PMC JTAG pins, but routes TDI->TDO to maintain integrity of any chains on the carrier boards. All manufacturing tests of the SMT417 are performed using the dedicated JTAG header.

3.1.8. PMC P14 Connector

The SMT417 provides a P14 connector for user defined I/O. All signals are brought to the FPGA to allow customer defined functionality to be implemented. The signals are +5V tolerant[1] by way of a pair of QS34X245Q3 'quick switches'.

3.1.9. Compliance

The SMT417 conforms to EN61000-4-2 for EMC and ANSI/VITA 47-2005 for other mechanical and environmental requirements.

3.2. XMC

XMC is an extension of CMC that uses implements multi-gigabit switched serial connections to the backplane. The ANSI/VITA 42 standard describes both single- and double-size mezzanine cards. The SMT417 is a single-size card implementing an 8-lane interface to the XMC connector.

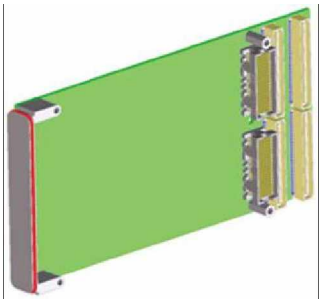


Figure 3 - Single-size XMC card (from ANSI/VITA 42)

[1] The XC2VP50 FPGA does ***not*** have 5V tolerant I/O.

3.2.1. ANSI/VITA 42.2 Serial RapidIO

ANSI/VITA 42.2 defines requirements and considerations for implementing Serial RapidIO over XMC to switched serial carriers. The SMT417 ***is*** electrically compatible with this standard. Two x4 links are available to the connector. A user will have the option of introducing a Serial RapidIO core to the FPGA on the SMT417 to allow it to interact with the fabric.

3.2.2. ANSI/VITA 42.3 PCI Express

ANSI/VITA 42.3 defines requirements and considerations for implementing PCI Express over XMC to switched serial carriers. The SMT417 ***is***[2] electrically compatible with this standard. One x8 link is available to the connector. A user will have the option of introducing a PCI Express core to the FPGA on the SMT417 to allow it to interact with the fabric.

3.2.3. XMC Connector

The SMT417 implements a primary (P15) interface only. The 8 lanes are routed as differential pairs directly to the FPGA according to ECMA-342, "Partition VI - Physical Layer 1x/4x LP-Serial Specification". AC coupling is used on the receivers.

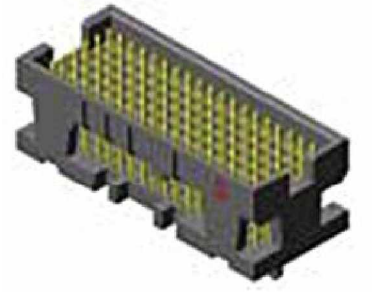


Figure 4 - XMC Connector Outline

3.2.4. XMC JTAG

The ANSI/VITA 42 specification governs how the JTAG signals are to be treated. The SMT417 does not attach any devices to the XMC JTAG pins, but routes TDI->TDO to maintain integrity of any chains on the carrier boards. All manufacturing tests of the SMT417 are performed using the dedicated JTAG header.

3.2.5. XMC IPMI

The SMT417 conforms to ANSI/VITA 42 Sec 5.4 by providing an I2C interface from the XMC connector to the CPLD. Contact Sundance DSP for details on CPLD revisions needed to support this part of the specification.

[2] The PCIe reference clock (REFCLK+/-) needs to be handled by a PLL:

http://www.xilinx.com/xlnx/xil_ans_display.jsp?BV_UseBVCookie=yes&getPagePath=18329

The SMT417 design uses a single ICS874005 to perform the 100MHz -> 125MHz conversion:

http://www.icst.com/icscs/SiteSearch.aspx?q=ICS874005

3.2.6. XMC VPWR

The ANSI/VITA 42 specification allows "Variable Power" to be applied at either +5V or +12V. The SMT417 is designed to accommodate one ***or*** the other according to build option. ***It is important to know whether your carrier board is configured for +5V VPWR or +12V VPWR and order the SMT417 appropriately***.

Do not connect an SMT417 incorrectly!

3.3. FMS

2 FMS connectors are provided on side 1 of the board. They are present on all build options.

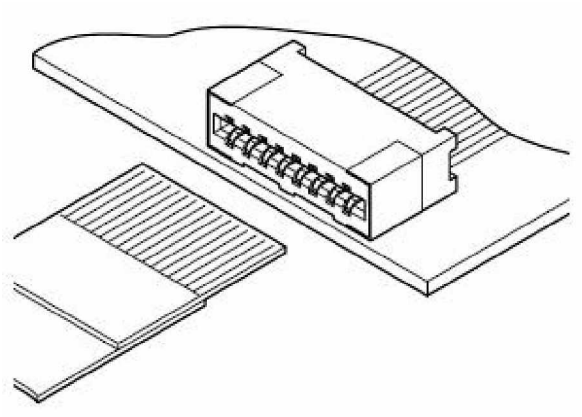


Figure 5 - FMS Connector Outline

An FMS connector provides 14 signal lines that typically implement an 8-bit digital link port according to the TI C40 comport link specification. The signal lines are connected directly to the FPGA, and can support typical signalling rates of 20MHz per bit. These are provided to make simple integration with other boards to create multiprocessor systems. The default FPGA design implements the Sundance Digital Link[3] (SDL/Comport) interface to allow simple connectivity between other Sundance carrier boards such as the SMT300 (Q) and SMT310 (Q).

3.4. SHB

The SMT417 can (optionally) include two Sundance High-speed Bus (SHB) interfaces, both on side two of the board. These are only populated if option 'E' is ordered.

[3] http://www.sundance.com/docs/SDL%20Technical%20Specification.pdf

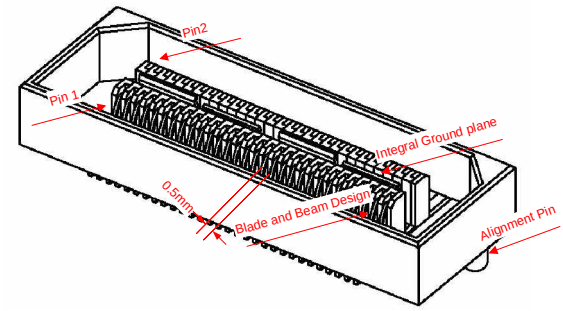


Figure 6 - SHB Connector Outline

An SHB connector provides 60 signal lines that typically implement the 16-bit Sundance Digital Bus (SDB) or 32-bit Sundance High Speed Bus[4] (SHB) interface. The signal lines are connected directly to the FPGA, and can support signalling rates of at least 133MHz per bit.

Please note that if the SHB connectors are mounted (a build-time option), the module becomes governed by the ANSI/VITA 32 specification (PrPMC). This may preclude spacing the PMC carrier boards in adjacent slots. Interfacing between SHB connectors on boards can be done by using Sundance SMT511-320, SMT512-DD, or SMT512-DA cables. See Section 9.2. below for additional details on cabling options.

3.5. RSL

The SMT417 can (optionally) include one Sundance RocketIO Serial Link (RSL) interface, present on side two of the board. These are only populated if option 'E' is ordered. This interface is connected directly to the MGT pairs of the FPGA and can support clock rates of up to 3.125GHz, depending on the speed grade of the FPGA that is ordered and the frequency of the reference clock oscillator fitted.

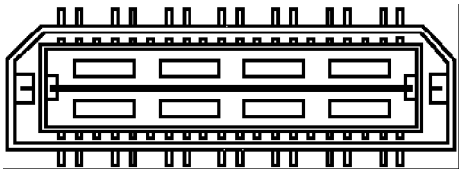


Figure 7 - RSL QTE-014-xx-DP Type Connector

The SMT417 implements a 7-lane interface to a "Type A" RSL connector. Interfacing to Sundance TIM modules can be accomplished using SMT522-RSL10 cables[5]. Interfacing to another SMT417 requires an SMT522-320-HE or SMT522-320-EH cable[6]. See Section 9.6. below for details on cabling options.

3.6. GRF

The SMT417 can (optionally) include one GRF1-J connector, present on side two of the board and populated with the 'E' option of the board. The connector provides 4 separate coaxial connector ports in

---

[4] ftp://ftp2.sundance.com/Pub/documentation/pdf-files/SHB_Technical_Specification.pdf

[5] http://www.sundance.com/web/files/productpage.asp?STRFilter=SMT522-RSL10

[6] http://www.precisionint.com/tdibrsb/images/drawings/D023850NNNLLLHE00.pdf

http://www.precisionint.com/tdibrsb/images/drawings/D023850NNNLLLEH00.pdf

a very small space. Each coaxial port is connected to one MGT signal, thus with 4 ports, a single lane (bidirectional) interface is exposed.

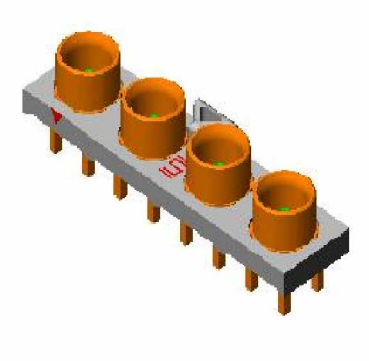


Figure 8 - GRF1-J Connector Outline

The GRF connector is provided to allow customers to convert MGT signals to individual coaxial cables, with standard ends, such as SMA, using the mating GRF1-C from Samtec.

Figure 9 - HW-AFX-SMA-SATA

Figure 10 - HW-AFX-SMA-SFP

These and many other conversion modules can be used to enable the SMT417 to connect its MGT signals to a wide variety of interfaces. See Section 9.7. below for details on cabling options.

3.7. JTAG

The SMT417 provides in-circuit debugging of its programmable DSP and FPGA devices. The JTAG chains for DSP and FPGA are electrically separate, allowing them to be used independently and concurrently. A small 20-pin header (J2) is fitted on side 1 under all build options. The header allows a ribbon cable to connect to an outboard JTAG adapter board.

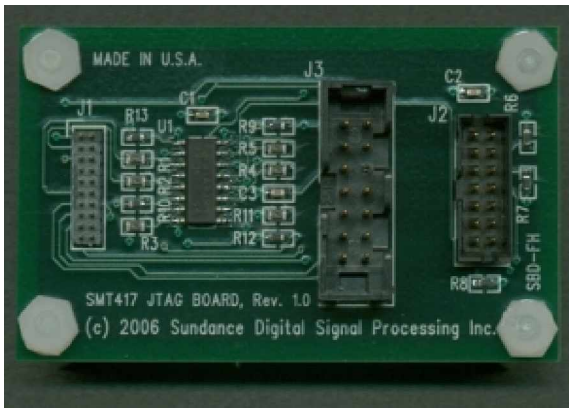


Figure 11 - Outboard JTAG adapter for SMT417

The JTAG adapter for the SMT417 provides a standard XDS510 JTAG port for the DSP. The adapter board also provides a standard Xilinx Parallel Cable IV port for the FPGA.

3.8. GPIO

The SMT417 can (optionally) be configured to provide several general purpose I/O (GPIO) signals, populated with the 'E' build option. 8 signal pins, two +3.3V pins and 6 GND pins are provided on a 16-pin header. See Section 9.9. below for pinout details.

3.9. EXTERNAL POWER

The SMT417 can (optionally) be configured to operate outside of a PMC/XMC system. In order to do this, +5V and +3.3V power needs to be supplied to the SMT417. A connector is populated for this purpose, once again under the 'E' build option.

Sundance provides a small outboard adapter board with power supply that is fitted onto this connector to provide a single (+5V) external supply input using a standard Molex (PC disk drive) connector. See section 9.10. below for pinout details.

4. DEVICES

4.1. QL5064 PCI BRIDGE

The PCI interface is implemented by a QuickLogic QL5064[7]. The QL5064 includes a hard PCI ASIC as well as an OTP fabric. In the SMT417, the QL5064 is preconfigured with the "Companion Design" logic from QuickLogic. This device bridges the PCI bus to a "Local Bus" on the SMT417 that connects the QL5064 with the XC2VP50 FPGA and the XC2C256 CPLD.

The QL5064 implements a 64-bit bus interface to the FPGA and allows the FPGA full access to the DMA controllers, the single-access PCI controller, and the target read/write buffers.

The QL5064 implements a simple 8-bit bus interface to the CPLD which has the ability to configure the FPGA, control system reset state and access the DSP JTAG chain.

In either case, the FPGA and CPLD devices appear in a PCI HOST memory mapped region, and control operations are effected by reading/modifying/writing registers on either the QL5064, CPLD or the FPGA.

4.2. CPLD

The CPLD on the SMT417 implements system reset control, FPGA SelectMAP programming and DSP JTAG interface functions. The CPLD is addressable by the PCI as well as by DSPA. The PCI side provides full access to the CPLD registers, while the DSP side provides access to a sub-set of them.

From the PCI side, the board can be reset as a whole, or just the FPGA or the DSPs can be reset.

Both sides can access the FPGA (re-)configuration interface allowing either the DSP or the PCI to update the FPGA design. As the FPGA is separated from the PCI via the (unchanging) QL5064 bridge, a variety of FPGA interfaces can be presented to the PCI bus without restarting the driver or the HOST operating system.

The PCI side also enables access to the DSP JTAG chain. If suitable host-side support is provided, this allows users to control the DSP via JTAG for debugging without the need of an external emulator[8].

4.3. FPGA

The FPGA on the SMT417 implements the connectivity between ***all*** the external interfaces on the board and the DSPs. The FPGA can be reconfigured by the customer to provide any manner of connectivity within the system.

The following description of the FPGA functionality describes the default implementation that is provided by Sundance DSP upon initial delivery of the SMT417 Board Support package.

---

[7] http://www.quicklogic.com/home.asp?menuID=110&PageID=319

[8] See also SMT6012, the support package for CCS for Sundance carrier boards and modules.

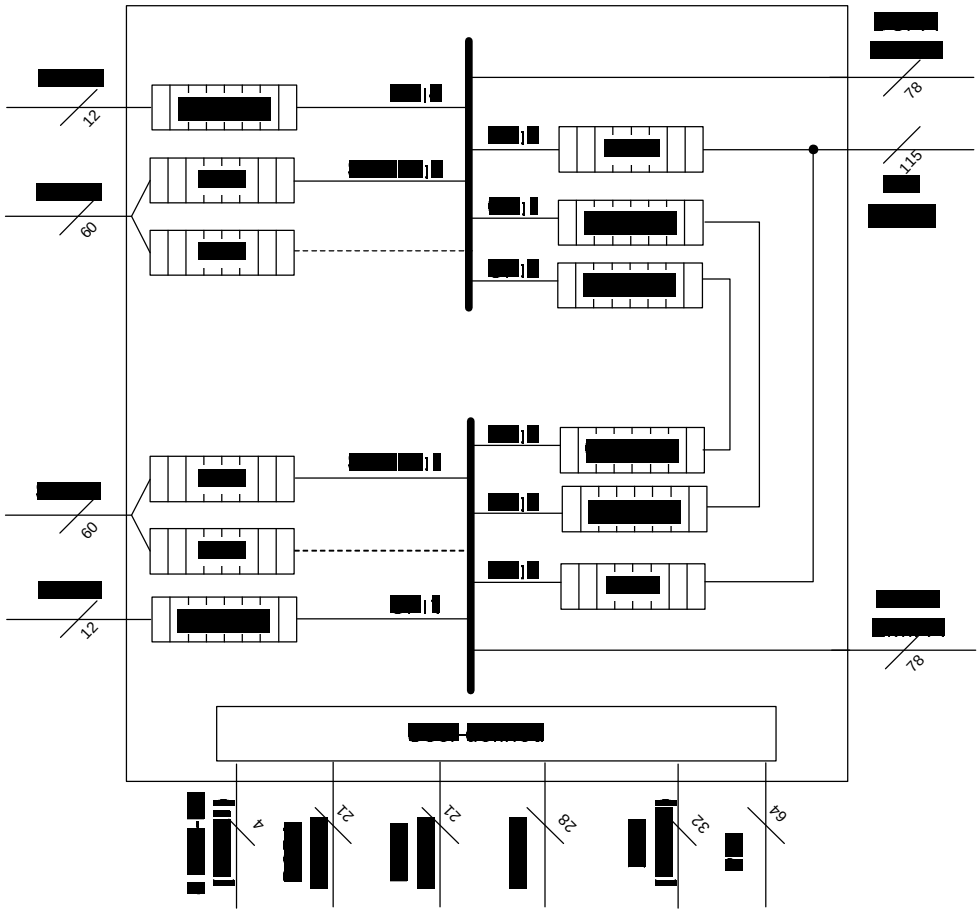


Figure 12 - Block diagram of SMT417 FPGA (v0.1)

The basic architecture implements an EMIF target interface to each of the DSPs. Each DSP accesses its resources independently and concurrently of the other. Resources such as comports, SDBs, the PCI interface and the user-defined blocks are memory mapped into the DSPs EMIF. The DSP's DMA engines and device drivers are responsible for pushing or pulling data to and from the resources respectively.

User-defined resources can be mapped into the EMIF as appropriate and necessary for the customer application. The most efficient way to do this is to "present" either a CP, SDB or RSL interface to the DSP's EMIF, and take advantage of existing software drivers on the DSP for this purpose.

The SMT417 Board Support Package provides the firmware sources (`.vhd`) for the basic architecture, as well as a means of customizing it under 3L Diamond/FPGA.

4.4. DSP

Two TMS320C6416T signal processors are available on the SMT417. The TMS320C64x™ (C64x™) device is based on the second-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture (VelociTI.2™) developed by Texas Instruments (TI). The C64x™ is a code-compatible member of the C6000™ DSP platform[9].

[9] http://focus.ti.com/docs/prod/folders/print/tms320c6416t.html

The DSP processors are excellent for performing image/signal processing, communications and implementing multiple-instruction, multiple-data (MIMD) algorithms.

The C64x™ DSP core processor has 64 general-purpose registers of 32-bit word length and eight independent functional units. This includes two multipliers for a 32-bit result and six arithmetic logic units. The C64x™ can produce four 16-bit multiply-accumulates (MACs) per cycle. The C6416T device has two high-performance embedded coprocessors [Viterbi Decoder Coprocessor (VCP) and Turbo Decoder Coprocessor (TCP)] that significantly speed up channel-decoding operations on-chip.

The C64x™ uses a two-level cache-based architecture. The Level 1 program cache (L1P) is a 128-Kbit direct mapped cache and the Level 1 data cache (L1D) is a 128-Kbit 2-way set-associative cache. The Level 2 memory/cache (L2) consists of an 8-Mbit (1M byte) memory space that is shared between program and data space. L2 memory can be configured as mapped memory or combinations of cache (up to 256K bytes) and mapped memory.

4.4.1. EMIF Interface to FPGA

High-bandwidth connectivity between the DSP and the FPGA uses the same 64-bit, 133MHz EMIF signalling as on the DSP/SDRAM interface.

4.4.2. FLASH

A single 512MB NAND FLASH memory device is attached to DSPA/EMIFB. This device enables the system bootstrap, default (or custom) FPGA bitstreams, and custom DSP application programs to be stored and executed on power-up or reset.

4.4.3. HPI

The SMT417 implements the Host Port interface in the following way: One of DSPAs EMIFB regions is mapped to DSPBs HPI. This enables DSPA to access any register/memory region of DSPB. This is typically used for bootloading DSPB at system reset.

4.4.4. McBSP

Each DSP has 3 multi-buffered serial ports. These are electrically connected to the FPGA and may be used by customers in any manner they wish. The default software interfaces provided by the SMT417 do not interface to these ports.

4.4.5. PCI Interface

The built-in PCI interface on the DSP is *not implemented* on the SMT417.

4.4.6. SDRAM

Each DSP has separate banks of SDRAM for local processing on EMIFA. 128MB of 64-bit SDRAM per DSP is populated on the board, based on two 512Mbit x32 parts per DSP (total of 256MB on board). The SDRAM is clocked at 133MHz.

4.4.7. UTOPIA

The built-in UTOPIA (Level 2 Slave ATM) interface on the DSP is *not implemented* on the SMT417.

5. OPERATION

This section describes the operation of the various functions that can be used to control the SMT417. Note that all of these operations are handled by the device drivers, software and firmware that is distributed with the SMT417 Board Support Package.

From a HOST-Centric point of view, there are two non-volatile interfaces present at power-up. The QL5064 Bridge registers and the CPLD registers which are accessible after the QL5064 Bridge is setup. The CPLD provides access to basic board control as well as programming the FPGA.

5.1. QL5064 BRIDGE SETUP

The SMT417 implements the "QL5064 Companion Design for SRAM FPGAs[10]". There are no deviations from the specifications of the external interfaces. The programming of the SMT417 FPGA, however, is handled by the SMT417 CPLD, rather than the capability offered by the QL5064[11].

5.1.1. ENABLE PCI ACCESS

The basic steps necessary to ***begin*** working with the SMT417 (from the PCI) are as follows:

1. Map the two primary memory regions, BAR0 and BAR1
2. Setup the BAR1-BAR4 bus region chip selects and timings for each of the bus region address spaces. The registers are in the BAR0 bus regions and indexed by constants given in `ql5064_pci.h` under "`QLCD_BAR0_BUS_REGION_*`".
    a. The "`_LO_`" register enables the internal transfer acknowledge mode and associated bus cycle delays.
    b. The "`_HI_`" register controls the burst enable, CS line and the strobe delays.
    c. The regions are setup (by default) according to the following table:

BAR	Region	Wait State	RD Delay	WR Delay	Burst	CS_SEL	Description
1	0-6	1	0	0	NO	2	CPLD Registers
1	7	2	0	1	NO	1	FPGA Link Ports
2-4, DMA	0-7	1	0	0	YES	4-16	FPGA Custom Logic

Table 1 - Base Address Region Setup Parameters

    d. ***IMPORTANT***: consider enabling the 'Transfer Acknowledge' function on each of the regions when developing FPGA firmware. An unacknowledged transfer will result in an NMI/Parity Error on the HOST and shutdown the system. Any memory regions which are mapped as 'pre-fetchable' are subject to spontaneous access by the HOST.

[10] See: http://www.quicklogic.com/images/QL5064_CD_UM.pdf

[11] This is different than the SMT407/SMT498 which *did* use this feature of the QL5064.

3. Setup the BAR1-BAR4 bus request addresses. The registers are in the BAR0 bus regions and indexed by constants given in `ql5064_pci.h` under "`QLCD_BAR0_REQAD_BARn`".

Resource	Local Bus Request Address	Resource Size	Prefetchable	Description
BAR0	N/A	8KB	NO	QL5064 Registers
BAR1	0x00000000	1MB	NO	CPLD/FPGA Link Ports
BAR2	0x00000000	256MB	NO	FPGA Custom Logic
BAR3	0x80000000	256MB	NO	FPGA Custom Logic
BAR4	0x00000000	128MB	YES	DSPA SDRAM[12]
BAR5	0x00000000	128MB	YES	DSPB SDRAM

Table 2 – Base Address Region Descriptions

4. Setup the DMA engine bus request addresses The registers are in the BAR0 bus regions and indexed by constants given in `ql5064_pci.h` under "`QLCD_BAR0_REQAD_DMA_*`". The values are not important until the DMA engines are activated for I/O transfers. Disable the DMA controller.
5. Enable access to the local bus by setting bit 7 and bit 2 in the `QLCD_BAR0_LB_CTRL` register.
6. Verify Read/Write access to QL5064 by performing the following actions:
    a. Write the channel 0 MWAR register at `bar0[QL5064_BAR0_CH0_MWAR]`.
    b. Read it back to ensure that it was written.
    c. Read the revision ID at `bar0[QLCD_BAR0_REV_ID]`.
7. The revision ID in #6.c, above determines if 'Bit Swizzling' needs to occur for CPLD accesses. If the revision id is `0xB0102`, then this bit swizzling needs to occur prior-to and after any data access to BAR1 targeting the CPLD registers. A macro for this purpose is provided in `smt417.h` under the names: `smt417CpldSwizzle()` and `smt417CpldDeswizzle()`.
8. Enable PCI operations by unlocking the CPLD as follows:
    a. Write `SMT417_CPLD_MAGIC_IDX` into `bar1[SMT417_CPLD_REGIDX_ADR]`.
    b. Write `SMT417_CPLD_MAGIC_VALUE` into `bar1[SMT417_CPLD_REGS_ADR]`.

5.1.2. DISABLE PCI ACCESS

The basic steps necessary to stop working with the SMT417 (from the PCI) are as follows:

1. Disable PCI operations by locking the CPLD as follows:
    a. Write `SMT417_CPLD_MAGIC_IDX` into `bar1[SMT417_CPLD_REGIDX_ADR]`.

[12] BAR4,5 SDRAM mapping to PCI requires support in the FPGA design. This is planned, but not currently implemented. Contact Sundance DSP for details.

b. Write 0 into `bar1[SMT417_CPLD_REGS_ADR]`.

2. Disable the DMA controller by writing 0 to `bar0[QLCD_BAR0_DMA_CTRL]`.
3. Unmap any memory regions which were mapped above.

5.1.3. RESET

The basic steps necessary to reset the SMT417 (from the PCI) are as follows:

1. (optional) Save the state of the `CPLD_SMCTL` and `CPLD_DSPJTAG` registers.
    a. Write `SMT417_CPLD_SMCTL_IDX` into `bar1[SMT417_CPLD_REGIDX_ADR]`.
    b. Read `bar1[SMT417_CPLD_REGS_ADR]`.
    c. Write `SMT417_CPLD_DSPJTAG_IDX` into `bar1[SMT417_CPLD_REGIDX_ADR]`.
    d. Read `bar1[SMT417_CPLD_REGS_ADR]`.
2. Set the `QLCD_BAR0_LB_CTRL_INIT_LRST` bit in `QLCD_BAR0_LB_CTRL` register.
3. Hold for 25ms
4. Clear the `QLCD_BAR0_LB_CTRL_INIT_LRST` bit in `QLCD_BAR0_LB_CTRL` register.
5. Delay for 2.5 sec (to allow the system PLLs to resync, etc.)
6. Set the `SMPROGB, SMINITB` and `FRESET` bits in `CPLD_SMCTL`.
7. Hold for 100ms
8. Clear the `FRESET` bit in `CPLD_SMCTL`.
    a. You may consider the original state of the `CPLD_SMCTL` bits saved in #1 above when writing the final value to the `CPLD_SMCTL` register.
    b. Write `SMT417_CPLD_SMCTL_IDX` into `bar1[SMT417_CPLD_REGIDX_ADR]`.
    c. Write `bar1[SMT417_CPLD_REGS_ADR]`.
9. Hold for 100ms
10. Clear the `DSPRESET` bit in the `CPLD_DSPJTAG` register.
    a. You may consider the original state of the `CPLD_DSPJTAG` bits saved in #1 above when writing the final value to the `CPLD_DSPJTAG` register.
    b. Write `SMT417_CPLD_DSPJTAG_IDX` into `bar1[SMT417_CPLD_REGIDX_ADR]`.
    c. Write `bar1[SMT417_CPLD_REGS_ADR]`.

5.2. CPLD OPERATION

The CPLD is responsible for managing board reset state, linking the DSP JTAG, and programming the FPGA via SelectMAP. The CPLD provides 4 decode pages on the PCI, and two 8-bit registers on each page. The table below describes the location and meaning of the page registers.

Resource	Local Bus Request Address	Register Size	Description
BAR1	0x000E0000	8-bit	CPLD Register Data Port
BAR1	0x000E0008	8-bit	CPLD Register Index Port
BAR1	0x000E1000	8-bit	SelectMAP Data Port
BAR1	0x000E2000	8-bit	DSP JTAG Data Port
BAR1	0x000E3000	8-bit	Unassigned

Table 3 - CPLD Register Pages

Within the first decode page (0xE0000), there are several CPLD registers which are accessible via the CPLD Register Data Port once the CPLD Register Index Port is written with the appropriate value.

See Section 7.2. below for details on the CPLD Registers bit assignments.

5.2.1. CPLD MAGIC Register

The CPLD MAGIC (indexed at `0x40B`) register is a read/write register enables PCI access to the board resources. This register must be written with the value `SMT417_CPLD_MAGIC_VALUE` before normal PCI operations will be allowed to the higher order BARs and the FPGA. This value is defined in the header `smt417.h` included with the SMT417 Board Support Package.

5.3. FPGA CONFIGURATION

The XC2VP50 FPGA present on the SMT417 may be configured by a variety of methods. The typical method is to have the DSPA bootloader (re-)load the FPGA configuration upon any reset of the board.

During application development, a user may wish to load/change the FPGA design often, and so the following methods are available.

5.3.1. JTAG

The SMT417 provides an external JTAG port dedicated for the FPGA JTAG chain. This port is compatible with the Xilinx Parallel Cable IV and other JTAG emulators from Xilinx.

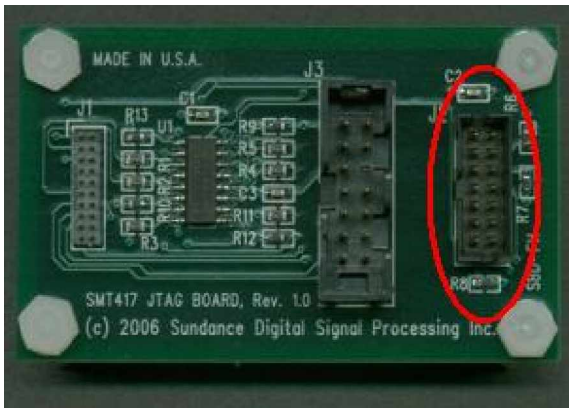


Figure 13 - Xilinx FPGA JTAG Port on JTAG Adapter

The JTAG adapter connects via a 20-pin ribbon cable between J2 on the SMT417 and J1 on the JTAG adapter. A standard 14-pin Xilinx JTAG is attached to J2 on the JTAG adapter, as pictured above. Once connected and powered, the CPLD, FPGA and QL5064 devices are present on the FPGA JTAG chain:

Figure 14 - Devices on the FPGA JTAG Chain

The programming files for the CPLD (XC2C256) and the QL5064 devices are provided in the SMT417 Board Support Package under `firmware\smt417\`. The pre-built programming files for the FPGA (XC2VP50) are also provided, but typically the user wishing to change the FPGA design will have their own `.bit` files that they wish to program.

Updating the FPGA design is simply a matter of selecting the device, and using the Xilinx iMPACT tool to program the bitstream. Please make note of the following caveats:

1. You should build your `.bit` with the `DriveDone = YES` flag set in the `bitgen` options.

2. You should build your firmware to respect the nRESET control provided to the FPGA.

If you use 3L Diamond/FPGA to build your firmware, then please note the following (additional) caveat:

3. Diamond/FPGA will generate firmware that uses the DSPA EMIF clock as the default clock. Thus, when loading your FPGA design, you must ensure that the DSPs are taken out of reset. The DSP EMIF clock does not run when the DSP is held in reset.

5.3.2. DSP via CPLD under Application Control

The FPGA can be programmed by DSPA through the CPLD. This can occur either at reset by the bootloader (typically), or by the users application at any other time. To do this, the SMCTL register is accessed by the DSP and the bitstream is loaded under the control of the DSP.

On the DSP, the SelectMAP control register is accessed at the address SMT417_DSP_CPLD_SMCTL, which is provided in the smt417.h header file. See 7.2.2. below for the bit definitions. The manual procedure is as follows:

1. Set INIT and FRESET and clear RDWR and PROG.
2. Delay 100ms.
3. Set the PROG bit.
4. Delay 100ms.
5. Check the INIT and DONE bits. INIT must be '1' and DONE must be '0', otherwise the FPGA is not ready to receive a new bitstream.
6. Write all the words in the desired bitstream DWORD-wise to the SelectMAP Data Port mapped in the DSPAs address space at SMT417_DSP_CPLD_SMD. The words can be sent in a burst, as the EMIFB timings have been designed to meet the specifications of the SelectMAP port on the FPGA.
7. Delay 100ms.
8. Check the INIT and DONE bits. Both INIT and DONE must be '1' if the FPGA has been successfully programmed.

An example and API for accomplishing this is provided in src\smt417\flash\hal_smt417.c in the SMT417 Board Support Package.

5.3.3. DSP via CPLD under Bootload

The default bootloader provided with the SMT417 performs an FPGA bitstream load function, if an FPGA bitstream is loaded to the appropriate sectors of the on-board NAND FLASH memory device. This is perhaps the easiest way to configure the FPGA once it is developed. To use this feature, the .bit file must be programmed into the FLASH at the appropriate sector.

The smt417FlashTool application is provided for this purpose. The smt417FlashTool is designed to operate under CCS JTAG, so DSP JTAG connectivity must first be established. The source code for the smt417FlashTool is provided at src\smt417\flashtool\ in the SMT417 Board Support Package. Details on using the tool can be found in the SMT417 Installation Guide.

5.3.4. PCI via CPLD

The SMT417 FPGA can be configured from the PCI. These functions are available to any application which uses the `ql5064_hal.h` API. Additionally several programs are distributed with the SMT417 Board Support Package to provide this facility from the command line.

The basic steps necessary to program the FPGA on the SMT417 (from the PCI) are as follows:

1. (optional) Hold the DSP in reset during this operation by setting the `DSPRESET` bit in the `CPLD_DSPJTAG` register.
2. Assert `PROG` by clearing `PROG` and `RDWR` in the `CPLD_SMCTL` register.
3. Delay for 100ms.
4. Set `PROG`, `INIT` and `FRESET` in the `CPLD_SMCTL` register.
5. Delay for 100ms.
6. Check the `INIT` and `DONE` bits. `INIT` must be '1' and `DONE` must be '0', otherwise the FPGA cannot accept a new bitstream.
7. Write all the words of the bitstream BYTE-wise to the SelectMAP Data Port[13].
    a. Write into `bar1[SMT417_CPLD_SMDATA_ADR]`.
    b. For every 1024 bytes, check the `INIT` bit in the `CPLD_SMCTL` register.
        a. If the bit is '0', this indicates a configuration error of some sort, so stop.
8. Delay for 100ms
9. Check the `INIT` and `DONE` bits. Both must be '1', otherwise the FPGA did not configure.
10. Set the `PROG`, `INIT` and `FRESET` bits in the `CPLD_SMCTL` register.
11. Hold for 100ms
12. (optional) If the DSP was held in reset in #1 above, release it.
13. Clear the `FRESET` bit in the `CPLD_SMCTL` register.
14. Delay for 100ms.
15. (optional) Configure the I/O link ports in the FPGA which provide connectivity to the FPGA from the PCI. To do this, index the link port's `CSR` register and set the `TRIGSIZE()` value for each link port. Toggle the `RESET` bit on the port as well. These operations are done in the `ql5064_hal.c` and the `ql5064_hal.h` API.

[13] You may want to parse the `.bit` header and only send the RAW data to the device, but the FPGA accepts the header portion of the `.bit` file.

5.4. FPGA I/O INTERFACES

This section describes the operation of the various I/O interfaces which are present on the SMT417 board. Since all of the important interfaces are connected to the FPGA, any of these descriptions can be modified by users of the SMT417 for their custom application needs. This section describes the ***default*** firmware design which is provided in the SMT417 Board Support Package.

5.4.1. Comports

Comports are implemented in order to allow communication between the DSPs. The presentation of the comport to the DSP is described in the Sundance literature[14,15].

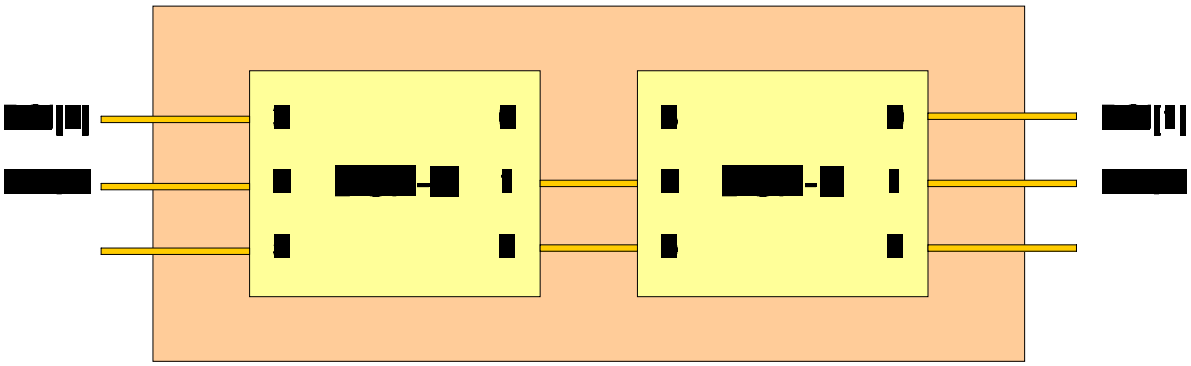


Figure 15 - Comport Links to DSPs

The diagram above describes the mapping of comport links between external resources and the DSPs. These links are implemented in the FPGA; each DSP accesses its comports via memory-mapped I/O in its respective EMIF(A) address space.

The comport interface includes a status register indicating the current port direction and number of FIFO entries (for each direction). The interface has a minimum transfer unit of 1 (32-bit) DWORD. Interrupts generated by comports are routed through standard Sundance interfaces described above.

5.4.2. PCI

A comport-like interface is established between each DSP and the PCI bridge. These are mapped as standard comports with respect to the DSP, and as the link ports described below with respect to the PCI. The main differences between this interface and a standard comport are as follows:

1) Separate ports for inbound/outbound data and control. I.e. link ports are uni-directional
2) 64-bit wide I/O capability.
3) 1024 (64-bit) QWORD FIFO depth in the FPGA.

[14] http://www.sundance.com/docs/SMT6400.chm

[15] http://www.sundance.com/docs/Firmware.pdf

The SMT417 Board Support Package provides source code, drivers and applications which describe the use of the link ports for I/O between the DSPs. Please refer to Section 7.3. below for register details.

5.4.3. SHB

The Sundance High Speed Bus[16] is implemented to allow high-bandwidth digital data transport to occur between modules. The SHBs can be configured for data widths of 16, or 32-bits, typically[17]. The presentation of the SDB interface is also described in the Sundance literature.

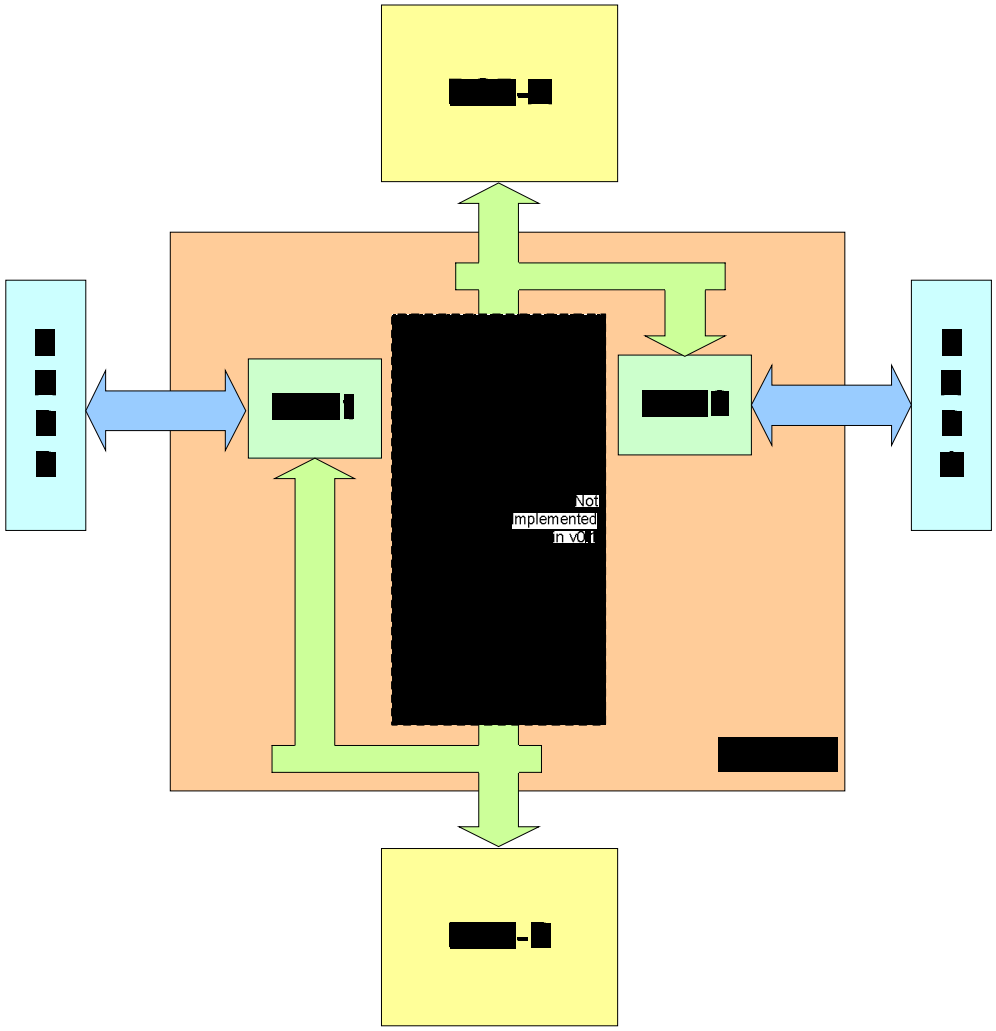


Figure 16 - SHB Links to DSPs

The firmware loaded onto the FPGA determines the organization of the SDB and which ports are connected to which DSPs. On multi-DSP modules, it is common to provide an SDB link through the FPGA. See the release notes for your version of the SMT417 Board Support Package for specific details.

---

[16] The Sundance Digital Bus (SDB) is used interchangeably. The physical layer protocol is identical with only the number of bits available on the connector being different. The SMT417 implements a full-specification SHB connector (60 signals).

[17] Multiple 8-bit and other interfaces can also be accommodated. Contact Sundance DSP for details on special firmware support.

5.4.4. MGTs

The XC2VP50 provides 16 Multi-Gigabit Transceiver pairs. These are routed to several connectors on the SMT417. All RX links are AC-coupled on the FPGA.

1. A Sundance RSL connector implements 7 bidirectional links. *Note, that the RSL specification defines only 6 bidirectional pairs, but the connector allows for 14 signal pairs, so the 7th link is connected.*

2. The XMC connector implements 8 bidirectional links according to ANSI/VITA 42.2 (Serial RapidIO for XMC).

3. A set of 4 coaxial connectors in a high-density mounting (5mm x 32.20mm) from Samtec. The GRF1-J PCB connector mates with a GRF1-C cable end to provide a means to expose a single 1x bidirectional link.

Please see Section 9.4. 9.6. 9.7. for details on the pin locations at the connectors. The table below describes the different resources and their location on the FPGA.

Location	IOB	Resource	Lane	Termination Power	CLOCK	Connector
A30-A33	X0_Y1	RSL	3	VRIOA	TOP.BREFCLK	JA6
A26-A29	X1_Y1	XMC	0	VRIOA	TOP.BREFCLK	J5
A22-A25	X2_Y1	XMC	4	VRIOA	TOP.BREFCLK	J5
A18-A21	X3_Y1	XMC	1	VRIOA	TOP.BREFCLK	J5
A14-A17	X4_Y1	XMC	2	VRIOA	TOP.BREFCLK	J5
A10-A13	X5_Y1	XMC	5	VRIOA	TOP.BREFCLK	J5
A6-A9	X6_Y1	XMC	3	VRIOA	TOP.BREFCLK	J5
A2-A5	X7_Y1	RSL	4	VRIOA	TOP.BREFCLK	JA6
AP2-AP5	X7_Y0	RSL	5	VRIOB	BOT.BREFCLK2	JA6
AP6-AP9	X6_Y0	GRF	0	VRIOB	BOT.BREFCLK2	JA5
AP10-AP13	X5_Y0	XMC	6	VRIOB	BOT.BREFCLK2	J5
AP14-AP17	X4_Y0	RSL	0	VRIOB	BOT.BREFCLK2	JA6
AP18-AP21	X3_Y0	RSL	1	VRIOB	BOT.BREFCLK2	JA6
AP22-AP25	X2_Y0	XMC	7	VRIOB	BOT.BREFCLK2	J5
AP26-AP29	X1_Y0	RSL	2	VRIOB	BOT.BREFCLK2	JA6
AP30-AP33	X0_Y0	RSL	6	VRIOB	BOT.BREFCLK2	JA6

Table 4 - MGT Cross-Reference for SMT417 PCB V2

5.4.4.1. FPGA Options

The FPGA device is an XC2VP50 of package type FF1152. In order to support the 637 total I/Os required by this design, the minimum device size will be a VP30. A VP50 is the minimum size that supports all 16 RSL links possible on this board. The table below shows the number and allocation of MGTs for different FPGA devices.

Device	XMC Lanes	RSL Lanes	GRF-1
XC2VP30	4	3	1
XC2VP40	4	7	1
XC2VP50	8	7	1

Table 5 - MGT Allocation vs. FPGA Size

5.4.4.2. Presentation to the DSP

Use of the MGTs via the DSP will be provided under 3L Diamond/FPGA under the RSL protocol. Contact Sundance DSP for details on accessing the MGTs apart from Diamond/FPGA or the RSL protocol.

5.4.4.3. Clock Source

When using the MGTs, it is important to consider the geographical location of the MGT pairs with respect to the available clock source. The possible clocks for the MGTs are as follows:

CLOCK	Signal	Freq	Reference Designator	Device	Notes
TOP.BREFCLK	PXPCLK	100MHz 125MHz	U22	ICS874005	XMC Clock via Jitter Cleaner/Retimer
TOP.BREFCLK2.P	DSPB.nAPDT	N/A	N/A	N/A	Not Used
TOP.BREFCLK.N	DSPB.nASOE3	N/A	N/A	N/A	Not Used
BOT.BREFCLK.P	SHBBCLK3	USER	JA4	N/A	User Option
BOT.BREFCLK.N	SHBBCLK0	USER	JA4	N/A	User Option
BOT.BREFCLK2	RSLCLK	125MHz	Y4	EG-2121CA	RSL Clock

Table 6 - MGT Clock Sources on SMT417

The TOP.BREFCLK is used for the MGT pairs connected to VRIOA, while BOT.BREFCLK2 is used for the MGT pairs connected to VRIOB.

For the XMC pairs, the incoming PXPCLK is routed through a Jitter Cleaner/Retimer as the XMC reference clock is typically 100MHz, but the XC2VP50 MGTs require a 125MHz clock to generate the 2.5GHz TX clock required.

For the RSL/GRF pairs, the SMT417 provides an on-board low-jitter clock source based on the EG-2121CA Series from Epson. The default value for this clock is 125MHz, which provides a 2.5GHz TX clock for these MGTs. Contact Sundance for options if a different value clock is required.

5.4.5. Interrupts

The SMT417 provides 4 interrupt lines to each DSP.

The Sundance firmware interface describes how interrupts are used by the DSPs. All of the I/O sources can be configured to interrupt according to their connection and data ready state. Registers grouped under this heading serve to provide two basic functions: interrupt routing and I/O interfaces. The interrupt control registers (ICR) allow interrupts from any comport, SHB or PCI I/O interfaces to be mapped to any of the four external interrupts connected to each DSP.

The signals are given in the following table:

FPGA Location	Signal	Target
F31	INTA4	DSPA
F30	INTA5	DSPA
J28	INTA6	DSPA
J27	INTA7	DSPA
AL34	INTB4	DSPB
AL33	INTB5	DSPB
AG28	INTB6	DSPB
AH27	INTB7	DSPB

Table 7 - FPGA Interrupt Lines

Custom interfaces are encouraged to conform to either the comport or SHB interface to the EMIF. This provides the most ready-to-use interface under both simple (polling) or advanced (EDMA) methods on the DSP.

5.4.6. User-defined I/O

The FPGA provides four GPIO signals to JA2, the GPIO header on Side 2 of the SMT417 board. Each DSP implements two GPIO signals to the same header, for a total of 8 signals. Please see Section 9.9. below for the pinout and routing of the header. *NOTE, these GPIO pins are **not** +5V tolerant!! It is important to use the +3.3V reference voltage on the JA2 connector, or ensure that the signals are clamped to +4.5V. Damage to the XC2VP50 FPGA may occur if the voltage on these GPIO pins exceeds +5V.*

Additionally, the DSPs implement 3 McBSP ports each to the DSP. There is no standard Sundance firmware design for these ports, but users may implement the necessary logic in the FPGA to enable them to route these signals as they wish.

Finally, the PMC P14 connector provides a total user-defined I/O space of 64 signals. Two of these signals are routed to global clock nets on the FPGA. All of the signals on the P14 connector are +5V tolerant by virtue of a pair of QS34X245Q3 "zero-delay" FET switches at U20 and U21. *NOTE, these are the **only** +5V tolerant pins that interface directly to the FPGA. All other external interfaces must be clamped to +4.5V*

Please refer to Section 9.1.4. below for the pinout and routing of the user-defined I/O connections on the P14 connector of the SMT417.

5.5. DSP

This section describes the various operations that can be performed by the DSP.

5.5.1. Boot Mode

The DSPs are each configured for one type of boot mode only. DSPA is configured to boot from FLASH at address base `0x64000000`, while DSPB is configured to boot from HPI. The HPI on DSPB is mapped to an address region on DSPA's EMIFB. This means that DSPA will 'bootload' both DSPs.

DSPA can be prevented from booting following a DSP reset event by holding the `DSPBOOT` bit low in the CPLD. There are two versions of the CPLD distributed: `smt417_cpld_noboot_v0p1.jed` and `smt417_cpld_v1p0.jed`. The former has `DSPBOOT` bit default low, while the latter is default high. The SMT417 are shipped pre-configured with the 'noboot' version which requires the board to be reset under PCI control.

When DSPA is reset and booting, the reset mechanism will load 1KB from FLASH at address `0x64000000`, copy that to internal memory at address `0x0` and begin execution.

5.5.2. Bootloader

The DSPA boot loader performs the following initializations:

1) Copy the rest of itself from FLASH page 0 to DSP internal memory.
2) Configure the EMIF on DSPA.
3) Determine if an FPGA bit stream is present in FLASH and configure the FPGA.
4) Determine if a DSP application for DSPB is present in FLASH
    a. If it is, load it to DSPB [*internal memory*] via HPI.
    b. DSPB is reset and the loaded application is started once loaded.
5) Determine if a DSP application for DSPA is present in FLASH
    a. If it is, load it to DSPA [*internal memory*] by copying its contents.
    b. The boot loader jumps to the entry point for the application once loaded.

The SMT417 are shipped with a boot loader that performs the above actions. The boot loader source is distributed in '`src\smt417\bootloader\`' of the SMT417 Board Support package.

It is not generally necessary to change the boot loader unless you have been given instructions by Sundance support engineers to do so. User applications can be installed in DSPA and DSPB to execute from FLASH directly by updating the two application areas instead.

NOTE: The boot loader must be kept to within the first page of FLASH (0x0 - 0x7FF). This allows subsequent applications to be loaded without concern for size or location.

NOTE: The DSP bootstrap mechanism (DMA) only copies the first ½ page of FLASH (0x0 - 0x3FF). The boot loader must copy the rest of the page to internal memory if it requires the additional code.

NOTE: The DSP bootstrap mechanism (DMA) will only work properly if the FLASH device is reset to read page 0. This means that care must be taken to ensure that the FLASH device is returned to page 0

when no longer in use. The distributed applications do this. Failure to do so may cause a boot load failure until the next power-cycle or use of the FLASH memory tool via DSP JTAG.

5.5.3. CPLD Control Registers

From the DSPs point of view, the CPLD is responsible for facilitating FLASH device access and enabling the (re-)program the FPGA on demand. The table below describes the location and meaning of the registers in the CPLD available to DSPA. The CPLD control registers are mapped onto CE0 of DSPA's EMIFB.

Resource	Local Bus Request Address	Register Size	Description
EMIFB	0x60000001	8-bit	CPLD SelectMAP Control Register
EMIFB	0x60000004	8-bit	CPLD FLASH Control Register
EMIFB	0x60008000	32-bit	SelectMAP Data Port

Table 8 - CPLD Register Addresses in DSPA Memory

Please refer to Section 7.2. below. For details on specific bits of the above registers.

5.5.4. EMIF Control Registers

Upon initialization the DSPs EMIF registers must be initialized in order for the (external) memory regions to function properly. The boot loader performs this action at system load for DSPA only. If you load a program on DSPB, configuring DSPB's EMIF is required.

Address Base	Size	Resource	Register Name	Register Value	Description
		EMIFA	GCTL	0x000820A0	
0x80000000	128MB	EMIFA	CE0	0x000000D0	SDRAM64
0x90000000	256MB	EMIFA	CE1-CE2	0x00000030	FPGA (SDRAM32)
0xB0000000	128MB	EMIFA	CE3	0x00000030	FPGA (SDRAM32)
		EMIFA	SDRAMREF	0x03000BB8	
		EMIFA	SDRAMCTL	0x63227000	COL9, ROW13 SDRAM
		EMIFB	GCTL	0x00082020	
0x60000000	128KB	EMIFB	CE0	0x10F10303	CPLD Timings (8-bit)
0x64000000		EMIFB	CE1-CE2	0x00B10301	FLASH Timings (8-bit)
0x6C000000	2MB	EMIFB	CE3	0x01310511	DSPB-HPI Timings (16-bit)

Table 9 - DSP EMIF Register Setup Values

The above values are also available in the `smt417.gel` file which is distributed with the SMT417 Board Support Package. This allows CCS users to operate the DSPs w/o concern for boot state.

5.5.5. SDRAM

Memory space CE0 on EMIFA is used to access 128MB of 64-bit wide SDRAM. The speed of the SDRAM is matched to the EMIF rate (133MHz for the TMS320C6416T).

5.5.6. FLASH

Memory spaces CE1 and CE2 on EMIFB of DSPA are used to access 512MB of 8-bit wide NAND FLASH. The NAND device acts more like a solid-state disk drive rather than a memory; it must be directed to 'seek' to a page before that page can be read-out. Once arrived, the page must be read out sequentially. Similarly, a NAND device can only be programmed in blocks (or groups of pages).

For the MT29F4G08BABWP device used on the SMT417, a page is 2KB and a block is 128KB.

FLASH commands are given by writing the command latch and/or address latch values.

Resource	Local Bus Request Address	Register Size	Description
DATA	0x64000000	32-bit	FLASH Bank 0 Data Port
ALE	0x64008000	8-bit	FLASH Bank 0 Address Latch
CLE	0x64010000	8-bit	FLASH Bank 0 Command Latch

Table 10 - DSP NAND FLASH Register Assignments

The specific details of controlling the NAND FLASH device are not described here. The SMT417 Board Support Package provides an API for accessing the memory device in "`src\smt417\flash\`" as well as examples of usage in "`src\smt417\flashtool\`" and "`test\ccs\smt417\smt417HalTest\`" within the distribution hierarchy.

Please refer to the device datasheet for additional details on utilizing the NAND FLASH in your own applications at your desired performance level.

5.5.6.1. FLASH Memory Organization

The boot loader distributed with the SMT417 defines the following organization on the FLASH memory in order to accomplish its stated operation:

Sector	Description
0	Bootloader
1-8	DSPA Application (internal memory only)
9-16	DSPB Application (internal memory only)
17-39	FPGA Bitstream
40-4095	Available for USER

Table 11 - SMT417 Default FLASH Organization

For simplicity of use, the API defines a 'sector' to represent a unit of I/O which can be read or written to. For the SMT417, the sector will therefore consist of 128KB. All FLASH management operations will operate with this granularity. The parameters above are provided in `smt417.h`.

NOTE: The source for the boot loader is provided in "`src\smt417\bootloader\`" of the SMT417 Board Support Package. This enables a user to tailor their bootstrap sequence according to their needs.

5.5.7. FPGA

From the DSPs perspective, the FPGA appears in the EMIFA address space at CE3, with the same SDRAM timing as the remainder of the spaces. All I/O resources are accessible as memory-mapped registers according to the standard Sundance firmware model.

The addresses of the SDB and comport interfaces are described in the SMT6400 help file.

5.5.8. Timer

The TINP[0:1] and TOUT[0:1] pins on each DSP are connected to the FPGA. This provides the opportunity to create/route a clock source in the FPGA and associate a DSP timer to it.

31-6	5	4	3-0
	TCLK1	TCLK0	
	RW,0	RW,0	

Table 12 - Timer Control Register

TCLKx 0=TCLKx is an input, 1=Enable TCLKx as an output

If the TCLKx pin is selected as an output, the DSP TOUTx signal will be used to drive it. TCLKx pin will always drive the DSP TINPx input. See the diagram below:

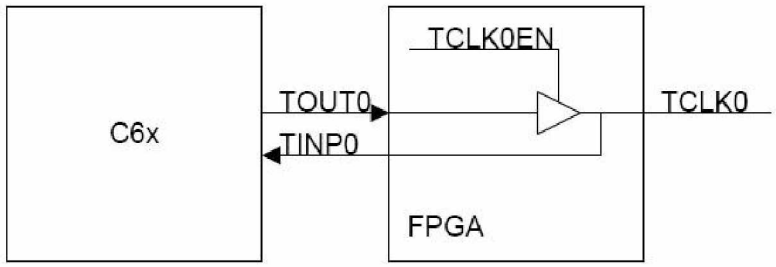


Figure 17 - DSP TCLKx Routing

TCLK0 is a signal that can be assigned to a User I/O pin to complete the standard timing control firmware.

NOTE: The smt417_vp50_v0p1.bit firmware does not implement a connection to TCLK0. Contact Sundance DSP for details regarding this feature.

5.5.9. LED and TTL I/O

The SMT417 has 2 LEDs and 2 TTL I/O pins available to each of the DSPs directly (via GPIO).

31-4	3	2	1	0
	TTL7	TTL6	LED D4	LED D3
	RW,0	RW,0	W,0	W,0

Table 13 - LED and GPIO Register for DSPA (0x01B00008)

31-4	3	2	1	0
	TTL5	TTL4	LED D6	LED D5
	RW,0	RW,0	W,0	W,0

Table 14 - LED and GPIO Register for DSPB (0x01B00008)

Using these values involves configuring the GPIO port on the DSP to drive or sample the pins and perform read/write access to the memory-mapped GPIO registers on each DSP. Several examples of manipulating these registers are provided in the SMT417 Board Support Package.

5.5.10. JTAG

The SMT417 provides an external JTAG port dedicated for the DSP JTAG chain. This port is compatible with the XDS510 specification and a variety of emulators from numerous vendors can be used to provide emulation capability.

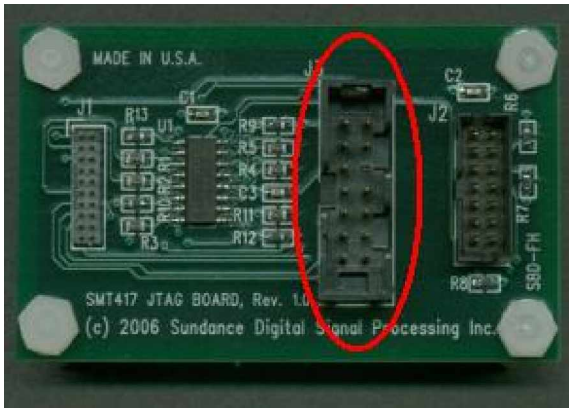


Figure 18 - XDS510 JTAG Port on JTAG Adapter

The TI DSP JTAG chain connects the two DSPs to separate pins on the same high-density debug header (J2), which is then brought out to the outboard JTAG Adapter pictured above.

Additionally, this chain terminates into I/O pins of the CPLD. The CPLD *can* function as a Master (driver) of the chain, or as a Linker (transparent) according the debug mode desired. When functioning as a master, the CPLD is under the control of the host driver. This chain is used to control and debug DSP

software, as well as to run the `smt417FlashTool.out` programming utility to managing the contents of the FLASH.

Contact Sundance DSP for details on suitable host driver software to enable CCS to provide JTAG emulation without an external JTAG.

5.6. CLOCK SOURCES

There are several independent clock sources on the SMT417:

1. PCI Clock: From the external PCI host, this clock is connected only to the QL5064. This clock may be idle if no external host is present.

2. QLCLK: The clock for the FPGA side of the QL5064, a dedicated crystal oscillator provides a fixed 64MHz clock. This clock is distributed to the QL5064, the FPGA and the CPLD.

3. DSPCLKA/B: Both DSPs have a fixed 50MHz clock input, and may be configured to run at an internal clock rate which is any supported multiple of this frequency. For a C6416T device this includes 1GHz (x20), 600MHz (x12), and 300MHz (x6). The crystal oscillator may be populated with a different value to support other DSP clock speeds.

4. EMIFCLK: Both DSPs are supplied with a single clock to use with the two EMIF ports. If the DSP is operating at no more than 800MHz, the user has the option of generating the EMIF clock by dividing-down the DSP clock by 6, or by using the external clock. Whichever clock is chosen by software will be passed to the external devices through the ECLKOUT pins. EMIFA and EMIFB may be configured separately. If the DSP clock is faster than 800MHz, then the external EMIF clock must be selected for both EMIFA and EMIFB. The frequency of the EMIF crystal must be selected at build time based on the speed of the SDRAM devices installed, (133MHz default). The EMIFB clock input runs at ½ the rate of the EMIFA clock input.

5. PCIXCLK: The XMC connector provides a differential reference clock for the purpose of generating the TX clock for the MGT transceivers. This clock is specified at 100MHz. In order to generate the 2.5GHz signalling rate, the XC2VP50 device requires a reference clock of 125MHz. Therefore, this signal first enters U22, an ICS874005 PCIe Jitter Cleaner and Retimer. This device synthesizes the 125MHz clock required by the XC2VP50 MGT logic from the 100MHz reference.

6. RSLCLK: The fixed-frequency differential 125MHz clock is fitted at Y4 for use by RSL and GRF connectors. The device is an Epson EG-2121CA125.000M-PGAN. This supports 2.5GHz TX signalling. Other values can be fitted according to customer requirements. Refer to the Sundnace RSL document and the Xilinx datasheets for additional details.

5.7. POWER SUPPLIES

The SMT417 conforms to the PMC standard for single-size modules. The PMC connectors supply the module with +5.0V and +3.3V power supply. The +3.3V will be used to supply all LVTTL digital I/O voltages directly, including the FPGA I/O rail V_{CCO}. The FPGA Core Voltage (V_{CCINT} = +1.5V, up to 10A) and DSP Core Voltage (V_{DSP} = +1.2V, up to 5A) are generated from the +5.0V by high-efficiency DC/DC converters. To avoid problems with the FPGA, the ramp rate of V_{CCINT} is limited by soft-start circuitry to between 200us and 50ms.

The FPGA Auxiliary voltage (V_{CCAUX} = +2.5V) is derived from +3.3V using a linear LDO regulator to minimise losses.

+2.5V Power for the Rocket-IO sections of the FPGA is supplied by two independent linear regulators.

Note: On 11/17/04, the Virtex-IIPro datasheet was amended, removing the requirement for special power-supply sequencing. From the v4.5 datasheet: "V_{CCAUX} and V_{CCO} can power on at any ramp rate. Power supplies can be turned on in any sequence."

5.8. RESET HIERARCHY

The SMT417 obeys the reset signal provided by the PMC connector; however this signal will only reset the QL5064. If desired, the DSPs and FPGA may be reset via PCI control through the CPLD interface. Additionally, the DSPs may also reset the FPGA. In any case the FPGA reset should not be released until the FPGA configuration has completed. Proper operation of the board in a stand-alone configuration (no PCI host present, no PCI clock) is ensured by use of a dedicated reset generator.

There are two fundamental scenarios at power-on:

1. PCI-controlled: The PCI bus resets the QL5064. Following PCI enumeration the driver software asserts reset to the DSPs and FPGA, configures the FPGA, loads code into DSPA and/or DSPB via JTAG, and releases the resets. Note that in this case, if there is valid code in the flash memory, the DSPs may start to execute code before the host PC has gotten around to asserting reset. This is a necessary consequence of supporting the following non-PCI case, where the state of the QL5064 is undefined. If this could be a problem, a "NOP" program should be loaded into the flash memory.

2. Embedded: The PCI bus may or may not be connected. Following the expiration of the on-board reset timer, DSPA begins to execute code from the flash memory. This code likely contains a configuration for the FPGA which will be loaded by DSPA, as well as code to be loaded into DSPB through that processor's host port. DSPB will not begin execution until commanded to do so by host-port control. Once the FPGA and DSPB have been configured, the two DSPs may communicate with each other through the FPGA, and other peripherals through various comports.

6. APPLICATION DEVELOPMENT

Depending on the complexity of the application, software and firmware can be developed in several ways.

6.1. SMT6400

For simple applications, the Sundance SMT6400 software support package and its associated header files (`SmtTim.h` and `ModSup.h`) can provide simplistic, polling calls to the I/O resources. The SMT6400 product can be installed free of charge, and provides additional examples.

The SMT417 Board Support Package provides the headers at "`include\smt6400\`". The calls are modified to place the calls as static inline functions which are optimized within the context of your code and make for easier build system integration.

6.2. 3L DIAMOND

Diamond is a sophisticated, optimized multi-processor and multi-FPGA operating system. Diamond allows your application to be partitioned into a number of independent *tasks* that communicate over *channels*. The channels are virtualized and routed by the Diamond RTOS enabling large networks of DSPs interconnected by data links to be managed automatically and efficiently.

The true power of Diamond comes into focus when some of the independent tasks are actually IP tasks placed within FPGA(s) to create hybrid DSP/FPGA topologies.

http://www.3l.com/Diamond/Diamond.htm

NOTE: The SMT417 is partially supported by 3L Diamond as of the date of this document; all of the FPGA bitstreams are developed with Diamond/FPGA. An application loader and FPGA re-programmer are in development.

6.3. SMT6045

SMT6045 is Sundance's "Universal Target Services for Sundance Hardware" package. It provides application development support, high-performance I/O services, and HOST platform support.

http://www.sundancedsp.com/edge/files/productpage.asp?STRFilter=SMT6045

The SMT417 Board Support Package is a subset of the complete SMT6045 Package.

6.4. PARS

Parallel Application from Rapid Simulation (PARS) is a tool that assists in converting a Simulink (a MathWorks product) model to software/firmware targeting multiple-DSPs and multiple-FPGA. PARS works in conjunction with Diamond/DSP and Diamond/FPGA to implement hardware-in-the-loop operation on Sundance hardware.

http://www.sundancedsp.com/edge/files/productpage.asp?STRFilter=PARS

NOTE: Support for PARS on the SMT417 is dependent on 3L Diamond at this time.

7. CONTROL REGISTER DESCRIPTIONS

This section describes the control registers present in various devices on the SMT417.

7.1. QL5064 REGISTERS

The SMT417 implements the "Companion Design for SRAM FPGA" in the QL5064. This is a design that provides an efficient non-transparent bridge operation between the PCI bus and the SMT417 Local Bus connecting the QL5064, the FPGA and the CPLD. 4 independent DMA engines are available to move data through the chip.

Resource	Offset	Register Size	Description
BAR0	0x1000	32-bit	Companion Design Revision ID
BAR0	0x1008	8-bit	GPIO
BAR0	0x1010	32-bit	Local Bus Control Register
BAR0	0x1C00-0x1CCC	32-bit	Local Bus Region Lo BARn
BAR0	0x1D00-0x1DFC	32-bit	Local Bus Region Lo DMA
BAR0	0x1E00-0x1EFC	32-bit	Local Bus Region Hi BARn
BAR0	0x1F00-0x1FFC	32-bit	Local Bus Region Hi DMA
BAR0	0x1200..0x1230	64-bit	DMA CH0..3 Address
BAR0	0x1208..0x1238	64-bit	DMA CH0..3 Count
BAR0	0x1240	32-bit	DMA Control
BAR0	0x1800-0x181C	32-bit	Local Bus Request Address BARn
BAR0	0x1820-0x183C	32-bit	Local Bus Request DMA Address

Table 15 - QL5064 Register Offsets in BAR0

7.1.1. Vendor ID and Device ID

The Vendor ID is 0x10B5. The Device ID is 0x8417.

7.1.2. Revision ID Register

The QL/CD Revision ID is 0x0b0102 for PCB V2.

7.1.3. GPIO Register

The QL5064 GPIO Register provides a method for the PCI to drive control signals to the devices on the SMT417 without performing a local bus bridge transaction. The following bits are defined:

31-24	23-16	15-8	7-0
ISTAT	OTYPE		OSTAT
R,00000000	RW,00000000	R,00000000	RW,00000000

Table 16 - QL5064 GPIO Register Bits

The definitions for this register are provided in the file `smt417_pci.h` of the Board Support Package.

OSTAT Drives bit 0..7 of the QL5064 GPIO.

OTYPE Controls the direction of the corresponding GPIO bit. 0=input, 1=output

ITYPE Reports the status of the corresponding GPIO bit.

The GPIO pins output from the QL5064 Device are routed to the following devices:

GPIO	Device	Pin
0	FPGA	D23
1	FPGA	D24
2	FPGA	C24
3	FPGA	K20
4	CPLD	A8; 4.7K pull-down
5	CPLD	N13
6	CPLD	P14
7	LEDS	LED D7

Table 17 - QL5064 GPIO Device Routing

7.1.4. Local Bus Control Register

The local bus control register affects features of the companion design that affect the operation of the bridge.

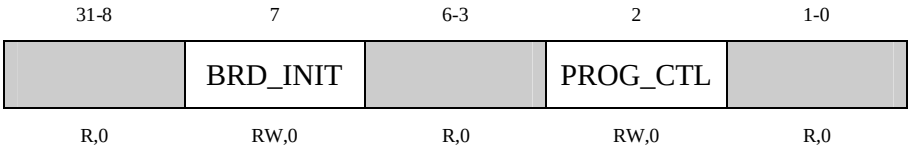


Table 18 - QL5064 Local Bus Control Register Bits

The definitions for this register are provided in the file `smt417_pci.h` of the Board Support Package, etc. Unspecified bits may be defined in the QL5064 Companion Design but are not used on the SMT417.

PROG_CTL	Unused but may be accessed.
BRD_INIT	Notify QL5064 that all bus regions are setup. Write 1 after all are initializations are setup to enable PCI bridge operations to begin.

7.1.5. QL5064 Companion Design Registers

The remainder of the companion design registers are described in the QuickLogic document.

http://www.quicklogic.com/images/QL5064_CD_UM.pdf

Refer to that document for register definitions and methods of setting up the DMA engines as well as details of setting up the local bus regions. The actual values to setup the registers were described in Section 5.1.1. above. Also, please refer to the code in `ql5064_init()` which is found in the "`src\win32\ql5064\hal\ql5064_hal.cpp`", the implementation of the QL5064 Abstraction Layer.

7.2. CPLD REGISTERS

The CPLD is responsible for managing board reset state, linking the DSP JTAG, exposing the FLASH control bits and programming the FPGA via SelectMAP. The CPLD provides 4 decode pages on the PCI, and two 8-bit registers on each page. The table below describes the location and meaning of the page registers.

Resource	Local Bus Request Address	Register Size	Description
BAR1	0x000E0000	8-bit	CPLD Register Data Port
BAR1	0x000E0008	8-bit	CPLD Register Index Port
BAR1	0x000E1000	8-bit	SelectMAP Data Port
BAR1	0x000E2000	8-bit	DSP JTAG Data Port
BAR1	0x000E3000	8-bit	Unassigned

Table 19 - CPLD Register Pages

Within the first decode page (`0xE0000`), there are several CPLD registers which are accessible via the CPLD Register Data Port once the CPLD Register Index Port is written with the appropriate value.

7.2.1. CPLD VERSION Register

The CPLD Version register is a read-only register that returns the current version of the CPLD. This register is accessible only from the PCI, at index `0x000`.

7.2.2. CPLD SMCTL Register

The CPLD SelectMAP Control register is a read/write register that manipulates the FPGA SelectMAP port. This register is available from the PCI at index `0x001`, and to DSPA (EMIFB) at address `0x60000001`. The following bits are defined:

7	6-5	4	3	2	1	0
RDWR		BUSY	FRESET	DONE	INIT	PROG
RW,1	R,00	R,0	RW,1	R,0	RW,0	RW,1

Table 20 - CPLD SelectMAP Control Register Bits

The definitions for this register are provided in the file `smt417.h` of the Board Support Package, etc.

PROG	Drives the PROG (active-low) pin on the FPGA.
INIT	Reports the INIT pin on the FPGA.
DONE	Reports the DONE pin on the FPGA.
FRESET	Drives the RESET pin on the FPGA.

BUSY Reports the state of BUSY for the SelectMAP interface. Typically used by the DSP only when programming the FPGA.

RDWR Controls the SelectMAP direction (0=Read, 1=Write)

The definitions for this register are provided in the file `smt417.h` of the Board Support Package, etc.

7.2.3. CPLD DSPJTAG Register

The CPLD DSP JTAG Control register is a read/write register that manipulates the DSP functions, and the JTAG interface. This register is available only to the PCI at index 0x02. The following bits are defined:

7	6	5	4-3	2	1	0
	DSPBOOT	DJPRESENT	DEMU	DEMUPUP	DSPRESET	DJTAGENB
R,0	RW,0	R,0	RW,00	RW,0	RW,0	RW,0

Table 21 - CPLD DSP JTAG Control Register Bits

The definitions for this register are provided in the file `smt417.h` of the Board Support Package, etc.

DJTAGENB Enables CPLD control over the JTAG port. If this bit is '0', then the CPLD simply passes-thru the JTAG and the use of an external emulator can be used. A HOST XDS510 driver may set this bit in order to provide JTAG emulation capability from the PCI bus.

DSPRESET Drives the reset control for both DSPs (1=Reset, 0=Not Reset)

DEMUPUP Controls whether the EMU[0:1] pins are pulled-up or not.

DEMU Controls the (driven) state of EMU[0:1] pins.

DJPRESENT Reports whether an external emulator is connected to the DSP JTAG chain.

DSPBOOT Controls whether DSPA boots when coming out of reset. (0=no boot, 1=boot)

7.2.4. CPLD LEDS Register

The CPLD LED register is a read/write register that manipulates the ouput state of the two LEDs attached to the CPLD. This register is only available to the PCI at index `0x03`. (DSPA has access to these LED bits via the FLCTL register, described below). The following bits are defined:

7-2	1	0
	D2	D1
R,0	RW,0	RW,0

Table 22 - CPLD LED Register Bits

The bits control the lit state of the LEDs D1 and D2 respectively. A value of '1' lights the LED.

7.2.5. CPLD MAGIC Register (0x40B)

The CPLD MAGIC register is a read/write register enables PCI access to the board resources. This register must be written with the value `SMT417_CPLD_MAGIC_VALUE` before normal PCI operations will be allowed to the higher order BARs and the FPGA.

7.2.6. CPLD FLCTL Register

The CPLD FLASH Control register is a read/write register that provides DSPA with certain functions of the CPLD, including primarily functions to control the FLASH. This register is available only to DSPA (EMIFB) at address `0x60000004`. The following bits are defined:

7	6	5-4	3	2	1	0
READY	WP	CPLED	PCIOK		DSPBHINT	DSPBHRDY
R,0	RW,1	RW,00	R,0	R,0	RW,0	R,0

Table 23 - CPLD DSP JTAG Control Register Bits

The definitions for this register are provided in the file `smt417.h` of the Board Support Package, etc.

DSPBHRDY	Reports the state of DSPB Host Ready Signal. This is used when DSPA controls communication to DSPB over the HPI.
DSPBHINT	Drives the Host Interrupt control for DSPB (1=Assert, 0=Not Asserted)
PCIOK	Reports whether the PCI interface has been configured or not.
CPLED	Controls the (driven) state of the CPLD LED (D1 and D2 on Side 2). *NOTE: this setting can be overridden by the PCI side access to the CPLD LED Register described above.*
WP	Controls the Write Protect signal to the FLASH memory. (1=write, 0=no write)
READY	Reports the Ready signal from the FLASH memory. (0=not ready, 1=ready)

7.3. FPGA I/O INTERFACE REGISTERS

The FPGA is responsible for interfacing the bridged local bus to the DSPs and any external I/O interfaces that are defined by the firmware. From the PCI side, the following registers are exposed by the default firmware that is shipped with the SMT417:

Resource	Local Bus Request Address	Register Size	Description
BAR1	0x00000008	64-bit	LED/Debug Port
BAR1	0x00000010	64-bit	Global Status Register
BAR1	0x00000050	32-bit	Port Configuration Register
BAR1	0x00000058	32-bit	Global Control Register
BAR1	0x00000060	32-bit	Control/Status Register (Link 0)
BAR1	0x00000068	64-bit	Data Register (Link 0)
BAR1	0x00000070	32-bit	Control/Status Register (Link 1)
BAR1	0x00000078	64-bit	Data Register (Link 1)
…	…	…	…
BAR1	0x000000D0	32-bit	Control/Status Register (Link 7)
BAR1	0x000000D8	64-bit	Control/Status Register (Link 7)

Table 24 - FPGA Register Offsets in BAR1

The local bus interface in the FPGA implements a target-only mode. High speed transfers are performed by activating the QL5064 DMA engine on the link and letting the hardware mechanisms move the data across the PCI bus automatically. The QL5064 DMA engine acts as a Bus Master on both the SMT417 local bus as well as the PCI bus.

The basic philosophy of the link interface is to provide 'N' link pairs. The EVEN-numbered link within a pair receives data from the PCI bus and sends it to the board, while the ODD-numbered links receive data from the board and send it to the PCI bus. The terms 'transmit' and 'receive' will be used referring to the board's perspective. The host software will consume data from transmit links and send data to receive links.

7.3.1. Global Status Register

This 64-bit read-only register represents a bit map of the current 'readiness state' of all the configured link ports. Bit N indicates the readiness of link N. This means that the link as at least "`TRIGSIZE`" DWORDs of data available (for transmit links) or at least '`TRIGSIZE`' DWORDs of space available (for receive links). There is room in the address map for extending this register up to 512 bits, or 256 link port-pairs.

7.3.2. Port Configuration Register

This 32-bit read-only register indicates the number of link port pairs implemented on the firmware currently loaded on the board, as well as the size of the FIFOs. The following bits are defined:

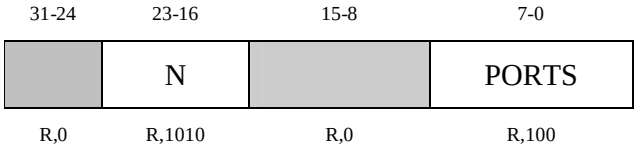


Table 25 – FPGA Port Configuration Register Bits

The definitions for this register are provided in the file `smt417_pci.h` of the Board Support Package, etc.

PORTS	The number of link ports implemented by the firmware.
N	Number of bits in the FIFO depth.

The total number of DWORDs implemented in the FIFO is therefore $2^{(N-1)}$.

7.3.3. Global Control Register

This 32-bit read-write register determines the assignment of which link port is assigned to which DMA engine. The following bits are defined:

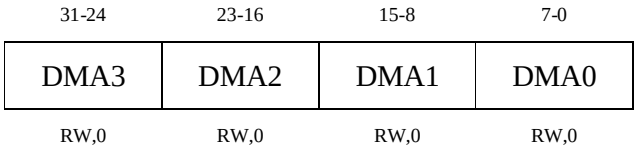


Table 26 – FPGA Global Control Register Bits

The definitions for this register are provided in the file `smt417_pci.h` of the Board Support Package, etc.

DMA0	This is a PCI->FPGA DMA Engine. Assign an EVEN link port.
DMA1	This is a FPGA->PCI DMA Engine. Assign an ODD link port.
DMA2	This is a PCI->FPGA DMA Engine. Assign an EVEN link port.
DMA3	This is a FPGA->PCI DMA Engine. Assign an ODD link port.

By configuring the port in this way, it enables the DMA engine to decode the opportunity for data transfer on the local bus for the configured port. The QL5064 DMA will fetch/write data on the local bus in order to fill/drain the transfer FIFOs.

7.3.4. Control/Status Register

Each link port maintains an independent 32-bit Control/Status register. The register provides all the information needed to determine if the port has/can accept data as well as how much. This register also holds the I/O trigger level at which requests will be made of the DMA interface. The following bits are defined:

31-20	19	18	17	16
LEVEL	ERROR	DONE	TRIG	READY
R,0	R,0	R,0	R,0	R,0

15	14	13	12	11-0
		IEN	RESET	TRIGSIZE
R,0	R,0	RW,0	RW,0	RW,0

Table 27 – FPGA Link Port Control/Status Register Bits

The definitions for this register are provided in the file `smt417_pci.h` of the Board Support Package, etc.

TRIGSIZE	The number of 32-bit DWORDs/spaces to assert TRIG
RESET	Clear all data and reset any error
IEN	Enable interrupt on TRIG
READY	At least one DWORD of data/space is present
TRIG	At least TRIGSIZE DWORDs of data/space are present
DONE	Receive FIFO is empty, or Transmit FIFO is full; in other words, the far side of the FIFO is stalled.
ERROR	An over/underflow condition has occurred. Assert RESET to clear
LEVEL	Report the number of 32-bit DWORDs/spaces are currently available

7.3.5. Data Register

Each link port maintains a 64-bit Data register for which access to the FIFO is made. The register is sensitive to a read/write according to the direction of the link. “Reverse” operation is not supported. 32-bit operation is supported on the low 32-bit of the port.

There are two versions of the Link Port interface firmware. One is a 64-bit (QWORD) based firmware which requires a minimum granularity of 64-bit access lengths to complete transactions. Another handles 32-bit (DWORD) as the minimum granularity. The latter uses more resources in the FPGA but is compatible with the 3L Diamond link layer protocol whose minimum granularity on all I/O is 32-bit.

8. FOOTPRINT

8.1. TOP

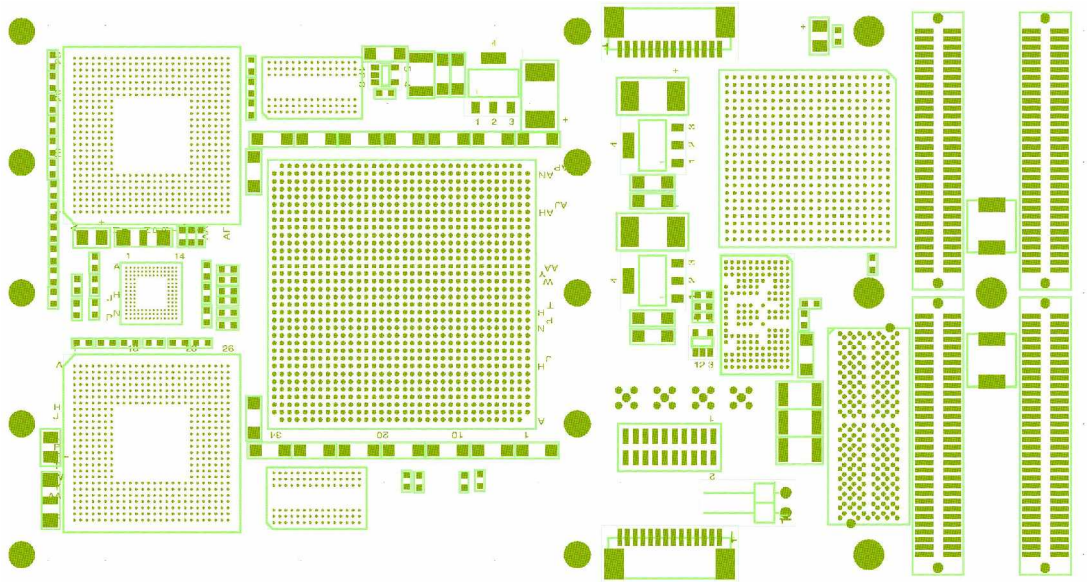


Figure 19 - SMT417 v2 PCB Top Layout (*Side 1*)

8.2. BOTTOM

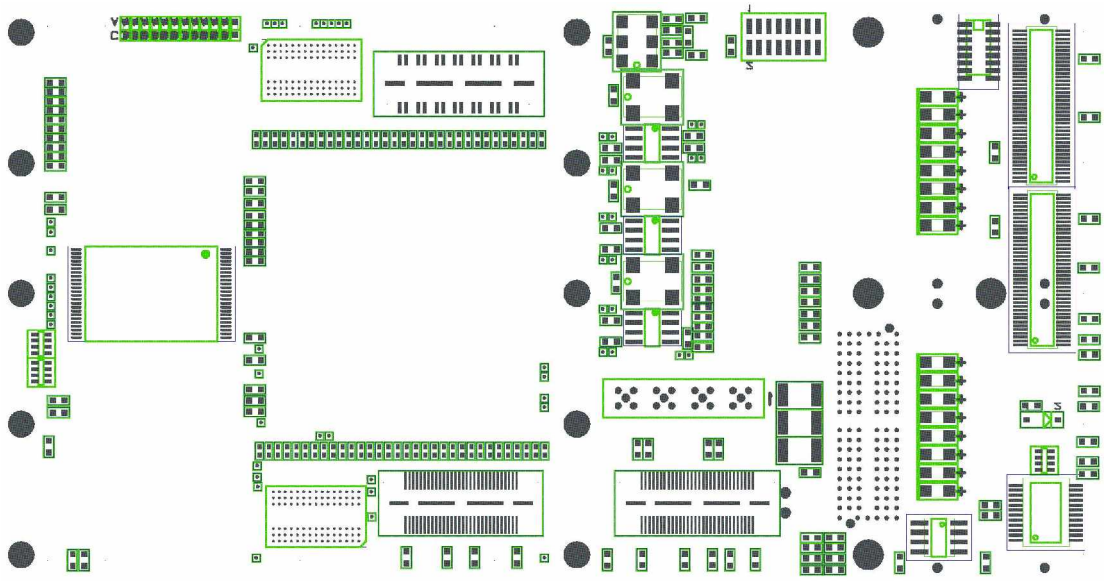
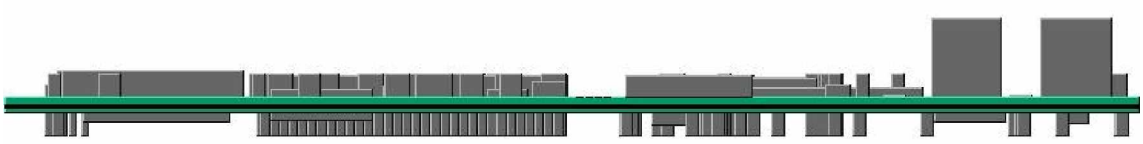


Figure 20 - SMT417 v2 PCB Bottom Layout (*Side 2 X-RAY VIEW*)

8.3. EDGE VIEW



8.4. MECHANICAL LAYOUT DIAGRAMS

The following diagrams describe the location and placement of mounting holes, connectors and components. The origin is as described in ANSI/VITA 20-2001 (R2005) Figure 3-1, pg.16.

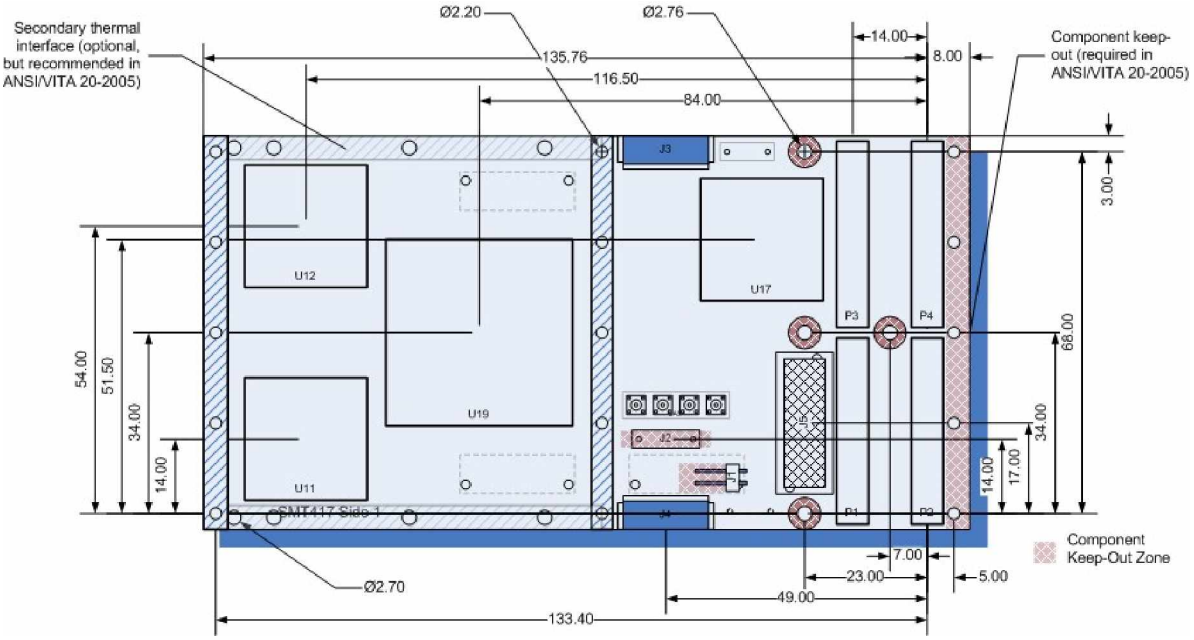


Figure 21 - Side 1 Mechanical Diagram

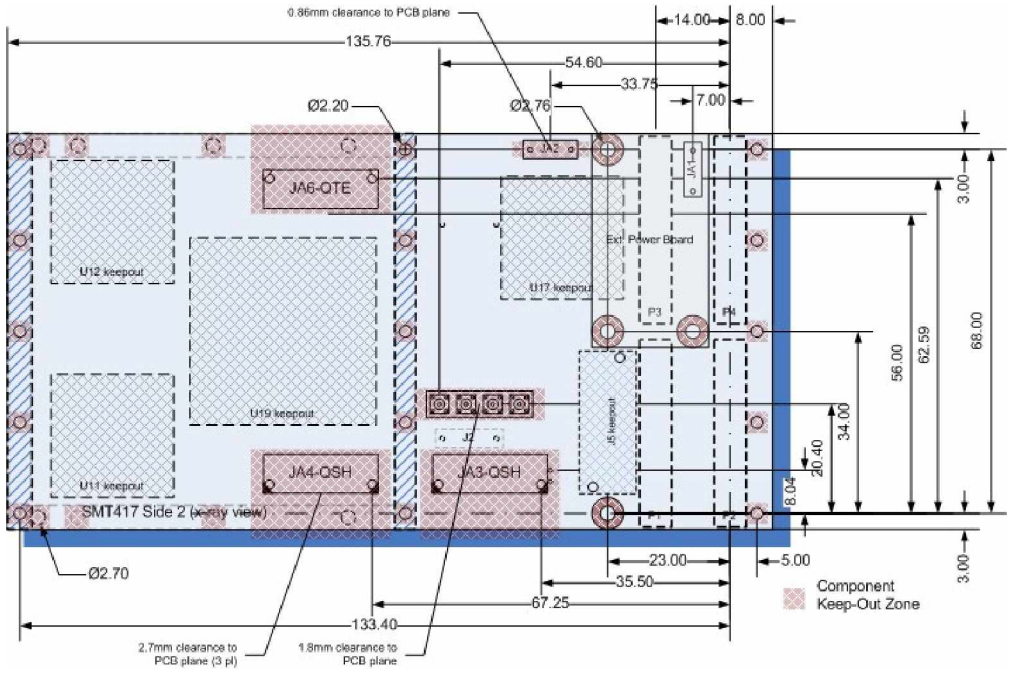


Figure 22 - Side 2 Mechanical Diagram

9. PINOUT

9.1. PCI

The PCI interface is implemented by four connectors, designated P11 thru P14. The connectors are Molex 71436-2364. Please refer to the manufacturer for mating connector information.

9.1.1. PMC P11 Connector

Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
1	TCK	-12V	2	33	FRAMEN	GND	34
3	GND	INTAN	4	35	GND	IRDYN	36
5	INTBN	INTCN	6	37	DEVSELN	+5V	38
7	BUSMODE1N	+5V	8	39	GND	LOCKN	40
9	INTDN	PCI-RSVD*	10	41	PCI-RSVD*	PCI-RSVD*	42
11	GND	3.3Vaux	12	43	PAR	GND	44
13	CLK	GND	14	45	VIO	AD15	46
15	GND	GNTN	16	47	AD12	AD11	48
17	REQN	+5V	18	49	AD9	+5V	50
19	VIO	AD31	20	51	GND	C/BE0N	52
21	AD28	AD27	22	53	AD6	AD5	54
23	AD25	GND	24	55	AD4	GND	56
25	GND	C/BE3N	26	57	VIO	AD3	58
27	AD22	AD21	28	59	AD2	AD1	60
29	AD19	+5V	30	61	AD0	+5V	62
31	VIO	AD17	32	63	GND	REQ64N	64

Table 28 - P11 Pin Assignments

9.1.2. PMC P12 Connector

Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
1	+12V	TRSTN	2	33	GND	PMC-RSVD	34
3	TMS	TDO	4	35	TRDYN	+3.3V	36
5	TDI	GND	6	37	GND	STOPN	38
7	GND	PCI-RSVD*	8	39	PERRN	GND	40
9	PCI-RSVD*	PCI-RSVD*	10	41	+3.3V	SERRN	42
11	BUSMODE2N	+3.3V	12	43	C/BE1N	GND	44
13	RSTN	BUSMODE3N	14	45	AD14	AD13	46
15	+3.3V	BUSMODE4N	16	47	M66EN	AD10	48
17	PMEN	GND	18	49	AD8	+3.3V	50
19	AD30	AD29	20	51	AD7	PMC-RSVD	52
21	GND	AD26	22	53	+3.3V	PMC-RSVD	54
23	AD24	+3.3V	24	55	PMC-RSVD	GND	56
25	IDSEL	AD23	26	57	PMC-RSVD	PMC-RSVD	58
27	+3.3V	AD20	28	59	GND	PMC-RSVD	60
29	AD18	GND	30	61	ACK64N	+3.3V	62
31	AD16	C/BE2N	32	63	GND	PMC-RSVD	64

Table 29 - P12 Pin Assignments

9.1.3. PMC P13 Connector

Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
1	PCI-RSVD	GND	2	33	GND	AD48	34
3	GND	C/BE7N	4	35	AD47	AD46	36
5	C/BE6N	C/BE5N	6	37	AD45	GND	38
7	C/BE4N	GND	8	39	VIO	AD44	40
9	VIO	PAR64	10	41	AD43	AD42	42
11	AD63	AD62	12	43	AD41	GND	44
13	AD61	GND	14	45	GND	AD40	46
15	GND	AD60	16	47	AD39	AD38	48
17	AD59	AD58	18	49	AD37	GND	50
19	AD57	GND	20	51	GND	AD36	52
21	VIO	AD56	22	53	AD35	AD34	54
23	AD55	AD54	24	55	AD33	GND	56
25	AD53	GND	26	57	VIO	AD32	58
27	GND	AD52	28	59	PCI-RSVD	PCI-RSVD	60
29	AD51	AD50	30	61	PCI-RSVD	GND	62
31	AD49	GND	32	63	GND	PCI-RSVD	64

Table 30 - P13 Pin Assignments

9.1.4. PMC P14 Connector

Pin	FPGA	FPGA	Pin		Pin	FPGA	FPGA	Pin
1	AJ18	AF11	2		33	AJ13	AG18	34
3	AE19	AJ21	4		35	AK13	AM13	36
5	AK21	AM22	6		37	AL11	AF16	38
7	AM21	AF19	8		39	AM11	AG16	40
9	AG10	AG19	10		41	AE15	AH15	42
11	AH10	AH20	12		43	AF15	AJ15	44
13	AK8	AJ20	14		45	AG14	AL14	46
15	AL8	AL21	16		47	AH14	AL15	48
17	AE13	AL20	18		49	AL13	AD17	50
19	AF13	AD18	20		51	AL12	AE17	52
21	AG13	AE18	22		53	AD16	AH16	54
23	AH13	AH19	24		55	AE16	AJ16	56
25	AJ21	AJ19	26		57	AJ14	AK16	58
27	AK11	AK19	28		59	AK14	AL16	60
29	AE14	AL19	30		61	AM14	AF17	62
31	AF14	AF18	32		63	AG17	AJ17	64

Table 31 - P14 Pin Assignments

PMC pins 1 and 64 are connected to GCLK pins on the FPGA.

9.2. SHB

The SHB is implemented by two connectors, designated JA3 and JA4. The connectors are Samtec QSH-030-01-L-D-A-K. Please refer to the manufacturer for mating connector information. The table immediately following shows the general layout of the pins, while the 2nd and 3rd tables in this section describe the connection of pins from the connector to the FPGA.

W	Hw		QSH Pin number	QSH Pin number	W	Hw	
CLK	Hw0	CLK	1	2	D0	Hw0	D0
D1		D1	3	4	D2		D2
D3		D3	5	6	D4		D4
D5		D5	7	8	D6		D6
D7		D7	9	10	D8		D8
D9		D9	11	12	D10		D10
D11		D11	13	14	D12		D12
D13		D13	15	16	D14		D14
D15		D15	17	18			USERDEF0
		USERDEF1	19	20			USERDEF2
		USERDEF3	21	22	WEN		WEN
REQ		REQ	23	24	ACK		ACK
			25	26			
			27	28			
			29	30			
			31	32			
			33	34			
			35	36			
	Hw1	CLK	37	38	D16	Hw1	D0
D17		D1	39	40	D18		D2
D19		D3	41	42	D20		D4
D21		D5	43	44	D22		D6
D23		D7	45	46	D24		D8
D25		D9	47	48	D26		D10
D27		D11	49	50	D28		D12
D29		D13	51	52	D30		D14
D31		D15	53	54			USERDEF0
		USERDEF1	55	56			USERDEF2
		USERDEF3	57	58			WEN
		REQ	59	60			ACK

Table 32 - General SHB Pin Allocation

The above table describes how an SHB is partitioned logically. The tables below describe the connections that the SMT417 makes from JA3 and JA4 to the FPGA.

9.2.1. SHB JA3 Connector

Pin	FPGA	FPGA	Pin	Pin	FPGA	FPGA	Pin
1	E17	E6	2	31	H16	H13	32
3	C11	E7	4	33	G16	G13	34
5	K15	H9	6	35	F16	D9	36
7	J15	G9	8	37	D17	C9	38
9	F14	H10	10	39	E16	K14	40
11	E14	G10	12	41	D16	J14	42
13	C14	J10	14	43	L17	F13	44
15	C13	K11	16	45	K17	E13	46
17	L16	J11	18	47	G17	E10	48
19	K16	F9	20	49	F17	D10	50
21	G15	E9	22	51	D19	H14	52
23	F15	D5	24	53	L18	G14	54
25	D14	D6	26	55	K18	D13	56
27	D15	K12	28	57	G18	D12	58
29	J16	J12	30	59	F18	D11	60

Table 33 - JA3 Pin Assignments

Pins 1 and 37 on JA3 (SHBA) are connected to GCLK pins on the FPGA.

9.2.2. SHB JA4 Connector

Pin	FPGA	FPGA	Pin		Pin	FPGA	FPGA	Pin
1	AK17	N6	2		31	V6	K4	32
3	D2	N5	4		33	V5	J2	34
5	D1	M1	6		35	V8	K2	36
7	F8	N1	8		37	AL17	L8	38
9	F7	P8	10		39	H2	L7	40
11	E4	P7	12		41	H1	L6	42
13	E3	N4	14		43	V7	L5	44
15	E2	N3	16		45	N8	K1	46
17	E1	N2	18		47	N7	L1	48
19	J8	P2	20		49	L4	N10	50
21	J7	R10	22		51	L3	N9	52
23	F5	R9	24		53	M4	M7	54
25	F4	M10	26		55	M3	M6	56
27	Y2	M9	28		57	P10	L2	58
29	W2	K5	30		59	P9	M2	60

Table 34 - JA4 Pin Assignments

Pins 1 and 37 on JA4 (SHBB) are connected to GCLK pins on the FPGA.

Typically, right-angle SHB cables are used, such as SMT512-120-DA or SMT512-120-AD.

9.3. JTAG

The SMT417 implements a high-density debug header to allow the Xilinx (FPGA) and TI (DSP) JTAG headers to be available. The header is a Samtec FTS-110-02-F-DV for an IDC ribbon cable. A small companion PCB and short cable interfaces to this high-density connector and provides standard Xilinx Parallel Cable IV or Platform Cable USB and TI XDS510 (IN and OUT) emulation headers.

9.3.1. J2 Header

Signal	Pin No.	Type	Function
DEMU0	17	I/O	DSP JTAG EMU0 Signal
DEMU1	19	I/O	DSP JTAG EMU1 Signal
DNTRST	5	In	DSP JTAG /TRST Signal
nDJPRESENT	18	Out	DSP JTAG /PD Signal
DTCK	11	In	DSP JTAG TCK Signal
DTCK_RET	15	Out	DSP JTAG TCK Return Signal
DTDI	1	In	DSP JTAG TDI Signal
DTDOB	13	Out	DSP JTAG TDO Signal
DTMS	3	I/O	DSP JTAG TMS Signal
FTCK	8	In	FPGA JTAG TCK Signal
CTDI	14	In	FPGA JTAG TDI Signal
QTDO	12	Out	FPGA JTAG TDO Signal
FTMS	6	I/O	FPGA JTAG TMS Signal
GND	7,9,10,16,20		Ground
V33	2,4		+3.3V

Table 35 - J2 Header Pinout

9.4. XMC

The XMC connector conforms to the type, position, and pinout specified in VITA 42.2 for XMC serial RapidIO. The header is a Samtec ASP-105885-01 header. The pinout is shown below.

9.4.1. J5 (P15) Header

	A	B	C	D	E	F
1	S0_TD0+	S0_TD0-	3.3V	S0_TD1+	S0_TD1-	VPWR
2	GND	GND	TRST#	GND	GND	MRSTI#
3	S0_TD2+	S0_TD2-	3.3V	S0_TD3+	S0_TD3-	VPWR
4	GND	GND	TCK	GND	GND	MRSTO#
5	S1_TD0+	S1_TD0-	3.3V	S1_TD1+	S1_TD1-	VPWR
6	GND	GND	TMS	GND	GND	+12V
7	S1_TD2+	S1_TD2-	3.3V	S1_TD3+	S1_TD3-	VPWR
8	GND	GND	TDI	GND	GND	-12V
9	RFU	RFU	UD	RFU	RFU	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	S0_RD0+	S0_RD0-	MBIST#	S0_RD1+	S0_RD1-	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	S0_RD2+	S0_RD2-	3.3V AUX	S0_RD3+	S0_RD3-	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	S1_RD0+	S1_RD0-	UD	S1_RD1+	S1_RD1-	VPWR
16	GND	GND	MVMRO	GND	GND	MSCL
17	S1_RD2+	S1_RD2-	RFU	S1_RD3+	S1_RD3-	RFU
18	GND	GND	UD	GND	GND	UD
19	RFU	RFU	UD	RFU	RFU	UD

Table 36 - J5 (P15) Pin Allocation

9.4.2. PCIe Support

In order to support PCIe operation over the XMC connector, the following signals are implemented according to ANSI/VITA 42.3:

	A	B	C	D	E	F
19	REFCLK+0	REFCLK-0		WAKE#	ROOT0#	

Table 37 - P15 Signals for PCIe Support

9.5. FMS

Two “FMS” connectors are provided on side 1 at J3 and J4. The connectors are JST 14FMS-1.0SP-TF and mate with the 14-pin FLAT cables which are commonly provided by Sundance. The connectors are single-row 14-pin type with 0.6mm pitch.

Signal	Pin No.	Type	Function
DET1	1	I/O	Direction Indicator
CxD(0-7)	2-9	I/O	Comport Data Bus
CREQx	10	I/O	Comport Token Request
CACKx	11	I/O	Comport Token Acknowledge
CSTRBx	12	I/O	Comport Data Strobe
CRDYx	13	I/O	Comport Data Ready
DET2	14	I/O	Direction Indicator

Table 38 – General FMS Pin Allocation

To determine ownership of the port on initialization, one of the two “detect” pins may be pulled-up to 3.3V while the other is grounded. It is important to connect FMS cables in such a way that the direction indicator pins are “crossed-over”. This can be accomplishing by twisting the cable such that the cable is inserted in the opposite manner for the far end connector.

9.5.1. J3 Pin Allocation

Pin	FPGA	FPGA	Pin
1	AF12	AF21	2
3	AJ22	AK22	4
5	AL24	AM24	6
7	AE20	AF20	8
9	AG21	AH21	10
11	AL22	AL23	12
13	AD19	AJ9	14

Table 39 - J3 Pin Allocation

A 4.7k pull-up is fitted from pin 1 and 14 to +3.3V.

9.5.2. J4 Pin Allocation

Pin	FPGA	FPGA	Pin
1	AK9	AF24	2
3	AG25	AH25	4
5	AK27	AL27	6
7	AE22	AF22	8
9	AG22	AH22	10
11	AJ24	AK24	12
13	AE21	AL9	14

Table 40 – J4 Pin Allocation

A 4.7k pull-up is fitted from pin 1 and 14 to +3.3V.

For mating with other SMT417's and other Sundance carriers, please use SMT500-FMS20.

9.6. RSL

A single RSL "Bottom" type connector is fitted on the SMT417, designated JA6. The connectors are Samtec QTE-014-01-F-D-DP-A. Please refer to the manufacturer for mating connector information. Table 4 above, described the logical partitioning of the RSL among the MGT ports of the FPGA.

9.6.1. JA6 Pin Allocation

Pin	FPGA	FPGA	Pin		Pin	FPGA	FPGA	Pin
1	AP15	AP16	2		17	A3	A4	18
3	AP14	AP17	4		19	A2	A5	20
5	AP19	AP20	6		21	AP3	AP4	22
7	AP18	AP21	8		23	AP2	AP5	24
9	AP27	AP28	10		25	AP31	AP32	26
11	AP26	AP29	12		27	AP30	AP33	28
13	A31	A32	14		29	GND	GND	30
15	A30	A33	16		31	GND	GND	32

Table 41 - JA6 Pin Allocation

For mating to other Sundance TIM modules, please use SMT522-RSL10. For mating to other SMT417, please use SMT522-320-HE (Samtec EQCD-020-12.60-SBL-STR-2 or HDR-130332-01-EQCD).

9.7. GRF

A single MGT transceiver pair is exposed onto a set of four high-density coaxial conectors, designated JA5. The connectors are Samtec GRF1-J-P-XXX. Please see the manufacturer for mating options.

9.7.1. JA5 Pin Allocation

Pin	Signal	FPGA	FPGA	Signal	Pin
1	RXGN0	AP6	AP7	RXGP0	2
3	TXGP0	AP8	AP9	TXGN0	4

Table 42 - JA5 Pin Allocation (SMT417 PCB V2)

9.8. LED

The SMT417 provides twelve LED to assist in system diagnostics. The LEDs are all lit by active low signalling. To light an LED drive a '0' logic level onto the respective pin.

LED	Device	Pin/Connection		LED	Device	Pin/Connection
D1	CPLD	P12		D7	QL5064	GPIO7
D2	CPLD	N6		D8	FPGA	E19
D3	DSPA	GPIO0		D9	FPGA	F19
D4	DSPA	GPIO1		D10	FPGA	G19
D5	DSPB	GPIO0		D11	FPGA	H19
D6	DSPB	GPIO1		D12	FPGA	ON=not prog, OFF=prog

Table 43 - LED Signal Allocation

The SMT417 LEDs are arranged along the edge of the board along Side 2.

9.9. GPIO

The SMT417 GPIO header is JA2. The connector is a Samtec FTS-108-02-F-DV header. Please contact the manufacturer site for mating connector information.

9.9.1. JA2 Pin Allocation

Header Pin	Function	Pin
2,4	V33	+3.3V
6,8,10,12,14,16	GND	
1	FPGA	G22
3	FPGA	D26
5	FPGA	C26
7	FPGA	K21
9	DSPB	GPIO2
11	DSPB	GPIO3
13	DSPA	GPIO2
15	DSPA	GPIO3

Table 44 - JA2 Pin Allocation

9.10. EXTERNAL POWER

The SMT417 provides the option for external power input via JA1. Typically a separate PCB is fitted with a power supply to enable operation from a single-supply. The connector is a Samtec MLE-108-01-G-DV-A female header. Please contact the manufacturer site for mating connector information.

9.10.1. JA1 Pin Allocation

Header Pin	Function	Pin
1,3,5	VCC	+5V
2,4,6,8,10,12,14,16	GND	
7,9,11	V33	+3.3V
13	V12P	+12V
15	V12N	-12V

Table 45 – JA1 Pin Allocation

+12V is only used on the SMT417 to supply the FAN power connector J1. It is typically provided by the PMC and XMC headers. -12V is not used on the SMT417, but is provided because of its presence on the PMC and XMC headers.

10. OPERATING CONDITIONS

10.1. POWER ESTIMATE

A power consumption estimate is performed for the following conditions:

- DSP CPU utilization of 60%, EMIF @133MHz, 50%, 70°C junction
- FPGA with standard firmware, PCI and SHB at 100% utilization
- Both DSPs active, no RSLs in use

SMT417 Active Power

PMC Card, 2DSP + 1FPGA, 256MB total

Item	P/N	Power Max.	Util. %	Qty.	Total Pwr (W)	Notes
Xilinx Vertex-2 FPGA	XC2VP50			1		Handling PCI access for DSP, and Comports among DSPs and to carrier. NO DATA PROCESSING included.
Iccintq		0.411	100%	1	0.411	70C Junction
Iccauxq		0.417	100%	1	0.417	
EMIF Data I/O		0.417	100%	1	0.417	133MHz
EMIF CLB I/O		0.684	100%	1	0.684	
EMIF FIFOs		0.186	100%	1	0.186	includes BRAM (FIFOs)
PCI Data I/O		0.100	100%	1	0.100	64MHz
PCI CLB I/O		0.165	100%	1	0.165	Includes BRAM and DCM
PCI FIFOs		0.328	100%	1	0.328	
SHB/External I/O		0.314	100%	1	0.314	100MHz
SHB/External CLBs		0.257	100%	1	0.257	
SHB/External FIFOs		0.080	100%	1	0.080	coupled with FMS, etc.
Clock Gen		0.011	100%	1	0.011	
FPGA Subtotal (W)	3.370					
SDR SDRAM	MT48LC16M32S2B5-6			4		NOTE: 4 x32 chips
single-bank active		0.825	50%	4	1.650	167MHz, assume EMIF is going at 133, SDR, at 50%
background		0.264	50%	4	0.528	
MEM Subtotal (W)	2.178					
TI DSP	TMS320C6416T			2		1.2V, 1GHz, 70C Junction
CPU		0.438	100%	2	0.876	
EMIF		0.214	100%	2	0.428	A=133MHz, B=66MHz
Misc		0.121	100%	2	0.242	timers, McBSP, misc. GPIO, etc.
Baseline		0.937	100%	2	1.874	Constant Power, 70C (includes values for CPU=0% and EMIF=0%)
DSP Subtotal (W)	3.420					
DC-DC	ip1201	1.800	100%	1	1.800	IOR power loss (from ip1201 data, fig. 2-5)
Misc.		0.500	100%	1	0.500	Unrepresented IO, etc.
PMC					11.268	

Table 46 - Full Power Dissipation Estimate

DSP power estimates are obtained from "spraa45.xls". FPGA power estimation is obtained from web-based Xilinx Power Central. Other estimates are obtained from respective manufacturer datasheets.

The expected "full-power' dissipation is 11.27W at 70C junction temperatures, not counting RSL consumption.

10.2. POWER REQUIREMENTS

Using the standard Comport/SDB/PCI interface FPGA firmware, and with arbitrary DSP programs running on both processors, the SMT417 is required to conform to PMC specification of no more than 7.5W power dissipation.

Voltage	Current (nominal)	Current (maximum)	Current (estimated)	Derived	Supplies
+3.3V				3.3V PCI	LVTTL Digital I/O, FPGA Vcco, DSP Vio
+2.5V				3.3V PCI	FPGA Vccaux
+2.5V				3.3V PCI	FPGA MGT Transceivers
+1.5V		10A		5V PCI	FPGA Vccint
+1.2V		5A		5V PCI	DSP Vcore

Table 47 - Power Budget based on Supply

Note that in the table above, the maximum current represents the capacity of the power supply unit, not the actual consumption of the derived rail.

10.3. THERMAL

The following diagrams describe a thermal simulation performed with the SMT417 PCB V1 which is based on the power estimate in 10.1. above. Note that the estimated dissipation of the power supply is factored into the thermal simulation.

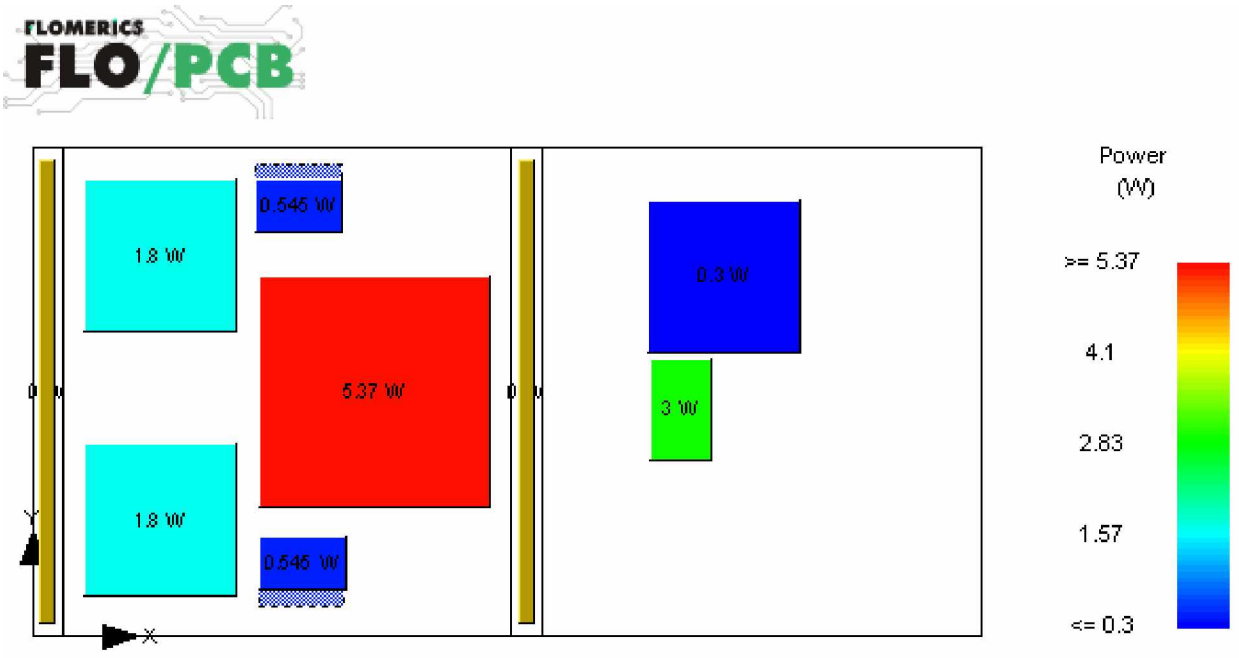


Figure 23 - Power Dissipation of Components

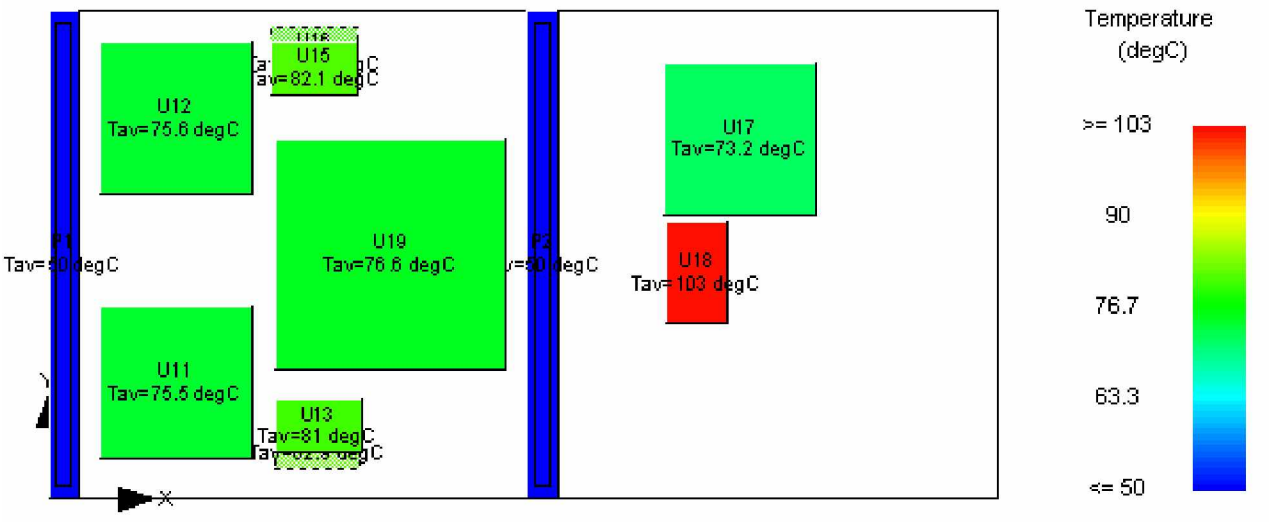


Figure 24 - Thermal Solution for SMT417

Based on the dissipation of the components in Figure 23, above, a thermal solution is presented for the SMT417 board. This solution assumes conduction cooling only, and a temperature at the thermal interface which is held at 50C.

This solution should be considered as 'maximum' operating conditions.

10.4. SAFETY

The module presents no hazard to the user.

10.5. EMC

The module is designed to operate within an enclosed host system that provides adequate EMC shielding. Operation within the EU EMC guidelines is only guaranteed when the module is installed within an appropriate host system.

The module is protected from damage by fast voltage transients introduced along output cables from outside the host system.

Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.

11.DATASHEETS

12. ORDERING INFORMATION

SMT417-<fpga>-<speed>-<xmc>-<option>

where:

<**fpga**>= VP50, VP40, VP30

<**speed**>= 5, 6, or 7

<**xmc**>= XMC connector and power options: "A"=No XMC, "B"=XMC +5V VPWR, "C"=XMC +3.3V (special, contact Sundance DSP), "D"=XMC +12V VPWR

<**option**>= none(std), "E"=(RSL+SHB+GRF+GPIO, "EX"=IO + external power option

FPGA may be ordered as XC2VP30 through XC2VP50, and speed grades from 5 through 7. Please note that Xilinx describes limitations on MGT signalling speed based on speed grade.

Selecting "A" for the bus option will de-populate the XMC connector. Selecting "B" through "D" will provide both XMC and PMC connectors. Note the value of VPWR, and select the appropriate case. Contact Sundance DSP for clarification before ordering "C" and "D" varieties.

Selecting no option for I/O will result in no additional connectors on Side 2, to be compliant with IEEE 1384-2001 for PMC modules. Selecting "E" will add the additional connectors for RSL, SHB, GRF and GPIO, etc. Selecting "EX" will include a power add-on board to enable the SMT417 to operate as a stand-alone board (without bus interface). Contact Sundance DSP for clarification before ordering "EX" variants.

12.1. EXAMPLES

SMT417-VP50-5-A-E	This is an SMT417 with no XMC, VP50-5 and all I/O connectors fitted.
SMT417-VP50-6-B	This is an SMT417 with XMC, +5V VPWR and no side 2 I/O, which is compliant to IEEE 1384-2001.