



June 2007

- Director's note: [Virtex-4](#)
- [SMT148-FX60](#)
- [Client's success: EREMS](#)
- [Exhibitions: Asia-Pacific](#)
- [Distributors](#)
- [Previous eNews](#)



SMT368 FPGA board for XtremeDSP™ processing



SMT362 Dual DSP for Serial RapidIO™ performance

Sundance hearts still belongs to Xilinx Virtex-4...

Our "love-affair" with [Virtex-4 FX60](#) started from the early stages of the Virtex-4 family roll-out. The FX60 was our chosen flagship as it contains everything anybody could ever require (this week!). This was late in 2004 and we were hoping and expecting to supply our growing customer base with pre-production products in September 2005. How wrong could we be?

The increased complexity, larger devices and high clock frequencies has surely made the task of design and testing a lot more tricky. But nobody could predict the delay to be years before we could ship working products. Well done to the Xilinx Team for actually making it happen as other companies might simply have forgotten about it and moved on.

So why do Sundance have such crush on Virtex-4 FX60, and why can it be found on five new Modules that were released to production early this year?

- Perfect number of FPGA slices for even the most demanding FFT, image compression or such demanding application.
- Ideal physical size to fit on any Sundance Module, sufficient I/O pins and very cost-effective in comparison to other options.
- Integration of dual PowerPC™ GPU for "MIPS-processing" tasks not suited to DSPs or FPGAs.
- Hard-core IP-cores for Serial interfaces (MGT) that will allow PCI Express, Serial Rapid I/O and Sundance's own Rocket Serial Link interface.

What more can any Human ask for a little piece of silicon? OK, it does not make the tea... yet.

Fleming CHRISTENSEN, Managing Director

Sundance's Virtex™-4 enabled modules:

In partnership with Texas Instruments and Xilinx, the Sundance Business Intelligence leads design engineers towards the new generation of Best-in-Class technologies for signal processing applications:

- Dual C6455 processors: [SMT362-FX60](#),
- Video and Multimedia DM642 DSP: [SMT339-FX60](#),
- Coprocessor FPGAs: [SMT348-LX160](#), [SMT368-SX35](#) and [SMT348-SX55](#),
- Quad-site PCI express development carrier: [SMT150-Quadro](#),
- Industrial VME64/VXS carrier board: [SMT329-VSX](#),
- Embedded and standalone platform system: [SMT148-FX60](#).

[More Details](#)

Zoom in on the Real-Time Beacon Simulator

EREMS specialises in the design of electronic instruments for high technology applications. EREMS has its own engineering, manufacturing and tests facilities located in the heart of the European Space region: Toulouse, France. For over 25 years, EREMS has been developing its expertise in the design for embedded systems integrated with customised software applications.

EREMS has designed and developed simulators for several generations of ARGOS and SARSAT satellite beacons.

The last model used in acceptance integration and validation phase of the GALILEO Payloads programme. ARGOS and SARSAT satellite beacons enhance performance for data collection, search and rescue.

Each simulator features:

- A compact PC including one [SMT395VP30_DSP](#) module and an [ADC board](#). This system computes and generates the modulation waves of the ARGOS/SARSAT beacons in real time (up to 32 at a time over 4 channels).
- Digitalised signals generated are controlled and transmitted in real time by the PC to the payloads.

The user software interface and the DSP software were designed by EREMS using [3L Diamond](#). The DSP software code was developed and optimised in Texas Instruments assembly language in order to support the beacon data throughput.

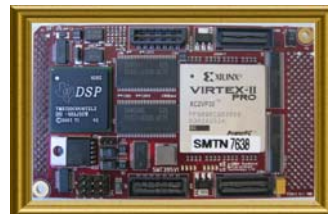
The instrument can generate the following type of modulations: BPSF, QPSK and GMSK. The simulation of transmission channel includes phase error, gain error, Doppler and quadrature error.

[More Details](#)

Article written in cooperation with G. Dejonghe & B. Chatelan, EREMS, France



ARGOS/SARSAT simulator



The SMT395VP30 hybrid DSP+FPGA architecture

