SUNDANCE The DSP & FPGA Development Force

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The Many Habits of Highly Effective Multiprocessor Design'

At the beginning of January a news item flashed across my desk from Sandia Labs...'more chip cores can mean slower supercomputing'. As a veteran advocate of the multiprocessing model you can imagine this caught my attention. What had the guys at Sandia discovered? What was this new revelation?

The answer was a rather well worn, well versed and long standing issue (though I applaud the Sandia team for highlighting it again). So I contacted Peter Robinson at 3L, a multiprocessing design authority and we 'shared our memories' on the subject. This meeting of minds, memories (coupled with a certain sense of déjà vu) resulted in the following '**7 Habits of Highly Effective Multiprocessor Design**'; some golden rules that will help you deliver faster computing and supercomputing performance.

The Multicore Dilemma: (Photo by Randy Montoya)

At the heart of the Sandia analysis was that **shared memory doesn't really work**. As they put it, "the problem is the lack of memory bandwidth as well as contention between processors over the memory bus available to each processor."

"The difficulty is contention among modules," said *James Peery*, director of Sandia's Computations, Computers, Information and Mathematics Center. "The cores are all asking for memory through the same pipe. It's like having one, two, four, or eight people all talking to you at the same time, saying, 'I want this information.' Then they have to wait until the answer to their request comes back. This causes delays."

And James is absolutely right, the shared memory concept for multi-core is flawed. This approach to general purpose multi-core processing is like building Hadrian's Wall with 100 builders spread between Newcastle and Carlisle with one guy with a wheelbarrow delivering the bricks... and the problems become worse as the number of processor cores on one chip increases.

So how can you overcome this problem? What are the 7 Habits you need to employ? I've listed them below, but if you want more information or want to discuss this further, please email me at flemming.c@sundance.com or contact Peter Robinson at psr@3L.com, you'll find us a receptive audience.

The Many Habits of Highly Effective Multiprocessor Design

1. Get rid of shared resources
2. Use simple processors (with independent memories) that can be programmed efficiently using higher level languages
3. Make them go as fast as possible, using the simplicity to drive the speed increases (and leave room for more on-chip memory)
4. Don't waste silicon with a vast array of specialized peripherals
5. Limit peripherals to a uniform set of very fast serial links: fast = simple to use and with none of the undesirable "features" that destroy things like RapidIO
6. Combine these with independent memories.
7. At the periphery, where the system interacts with the rest of the universe, add specialized convertors from links to whatever device standards you need.

..and just in case. If someone tells you that software can solve the problem, please remember the wise words of Tensilica's CEO, *Chris Rowen*, "The challenge of writing software for programming general purpose computing applications is generally recognized in the scientific computing community as the biggest single unsolved, and perhaps unsolvable, computing problem."

'There's a new kid on the block... and his friends name is Butch.'

You knew it was only a matter of time before we brought to you, our most obvious cliché, but with the arrival of our new kid on-the-block, we thought the time was right.

The kid in question is the 'Sundance Kid' and better known as the SMT712, a tough talkin, hard workin Dual DAC PXI Express Hybrid Peripheral Module. And just like the Sundance Kid who was immortalized by Robert Redford, the SMT712 takes no prisoners.

The SMT712 is a dividend of the PXI product development roadmap we announced in October 2008 and demonstrates our commitment to customers who have taken the PXI specification to the heart of their product and service development.

It integrates two fast 12-bit DACs, 2 banks of 64 bit wide 300MHz DDR2 memory and 8 lanes of 2.5Gbits/s PXI Express. At the heart of the SMT712 is a Xilinx Virtex 5 LX110T device, optimized for high performance logic and advanced serial connectivity. The device features 640 User I/O, 64 DSP48E slices and can access both 1GB DDR2 memory banks to store data on the fly.

The SMT712s Dual DACs are optimized for wideband communications and radar applications and feature an update rate up to 2.3Gsps. They have four 12-bit multiplexed low-voltage differential signaling (LVDS) input ports that operate up to 575MHz and have outstanding spurious and noise performance.

As standard, the SMT712 is a 3U PXI Express peripheral module. It's supplied with two PXI Express connectors, XP4 and XP3, and it dedicates 8 lanes to the PXI Express bus giving an effective bandwidth per direction of 16Gb/s. The SMT712 can also plug in any PXI Express Peripheral Slot or any PXI Express Hybrid Slot, or it can be a 3U Hybrid Peripheral Slot Compatible PXI-1 Module through the supply of an XP4 connector a P1 connector.

In summary, it's the PXI Express solution you can have your way! For more information please contact your local Sundance Office or email enquiries@sundance.com

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'Sundance @ the Mobile World Congress'

If you didn't get to the Mobile World Congress (MWC09) in Barcelona, you might not be aware that Sundance, our partners and customers were right at the heart of the show, mixing it with the likes of Microsoft's Steve Ballmer, Vodafone's Vittoria Colao...and Kevin Spacey, yes Kevin Spacey!

Promoting their position as the pioneer's of LTE (Long Term Evolution) on software defined radio platforms, were our customer and friend mimoOn. They were demonstrating, amongst other things, LTE software integration onto high-end TI DSP, and end-to-end LTE video streaming calls between a complete LTE eNodeB protocol stack and a complete LTE terminal protocol stack implementation.

mimoOn use our MIMO development systems that feature the SMT901 Dual MIMO RF transceiver module. It comprises two complete, fully configurable transceiver chains between two 2 x 10-bit digital I/Q interfaces and two dual-band 50 Ohm antenna ports.

Created to help companies such as mimoOn push the boundaries of communications design, our MIMO solutions provide the fastest, lowest risk route to prototyping and testing next generation MIMO applications and algorithms. They are scalable to add more channels and more DSP and FPGA processing power and are fully supported by 3L's Diamond multiprocessor tool-suite.

To learn more about mimoOn please visit www.mimoon.de and to find out how Sundance solutions are catalyzing next generation communications please visit www.sundance.com.
