

APPLICATION NOTE 1

Application Note - Multiple SMT702 System.

SMT702v2

SUNDANCE MULTIPROCESSOR TECHNOLOGY LTD.

Date	Comments / Changes	Author	Revision
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Document Title		Application Note - Multiple SMT702 System .doc			
Date	13/05/2010	Revision	1	Page	1 of 11

Introduction

The SMT702v2 is PXI Express module that integrates two fast 8-bit ADC (3GSPS), a clock circuitry, 2 banks of DDR2 memory (1Gbytes each), a 4-lane PXI Express core and two SHB connectors (32-bit bus, Double-Data Rate).

More than one board can be integrated within a system. We will look at the case of five modules in this example.

In multiple acquisition board systems, it is important that all modules receive the same sampling clock. In our case, there will be a single clock source that is distributed to the modules via a power splitter. In the case of the SMT702v2s, ADCs take a DDR sampling clock, which means that a 1.5-GHz signal will allow the converters to work at their maximum speed (3GSPS).

It is often the case that acquisitions from more than one ADC channels are only meaningful when they are gathered and linked to an identical time reference. This is the case in the system we are looking at, ADC samples are gathered from one board to another thanks to the fast DDR SHB buses available on each board.

Resources available in FPGAs can be used to implement some processing to combine channels or reduce the amount as an example.

System Block Diagram

The diagram below shows the connections between the boards (SMT702v2s) and how samples are routed. Each board is individually configured via its own PXI Express interface.

The architecture of the system showed below is symmetrical. There are two SMT702v2s used to sample signal on each side of a fifth one that gathers, stores and transfer to the host samples from all 8 channels.

Thanks to the power splitter, all 8 ADCs receive an identical clock in frequency and phase. ADC chips implement a clock divider (divide by 8) to clock samples out of the chip. These dividers are reset by the chip reset. One of the requirements of this system is to have all ADCs sampling and outputting data at the same time, this is the reason why an external trigger is needed to synchronise the converters and be part of the logic to reset the converters.

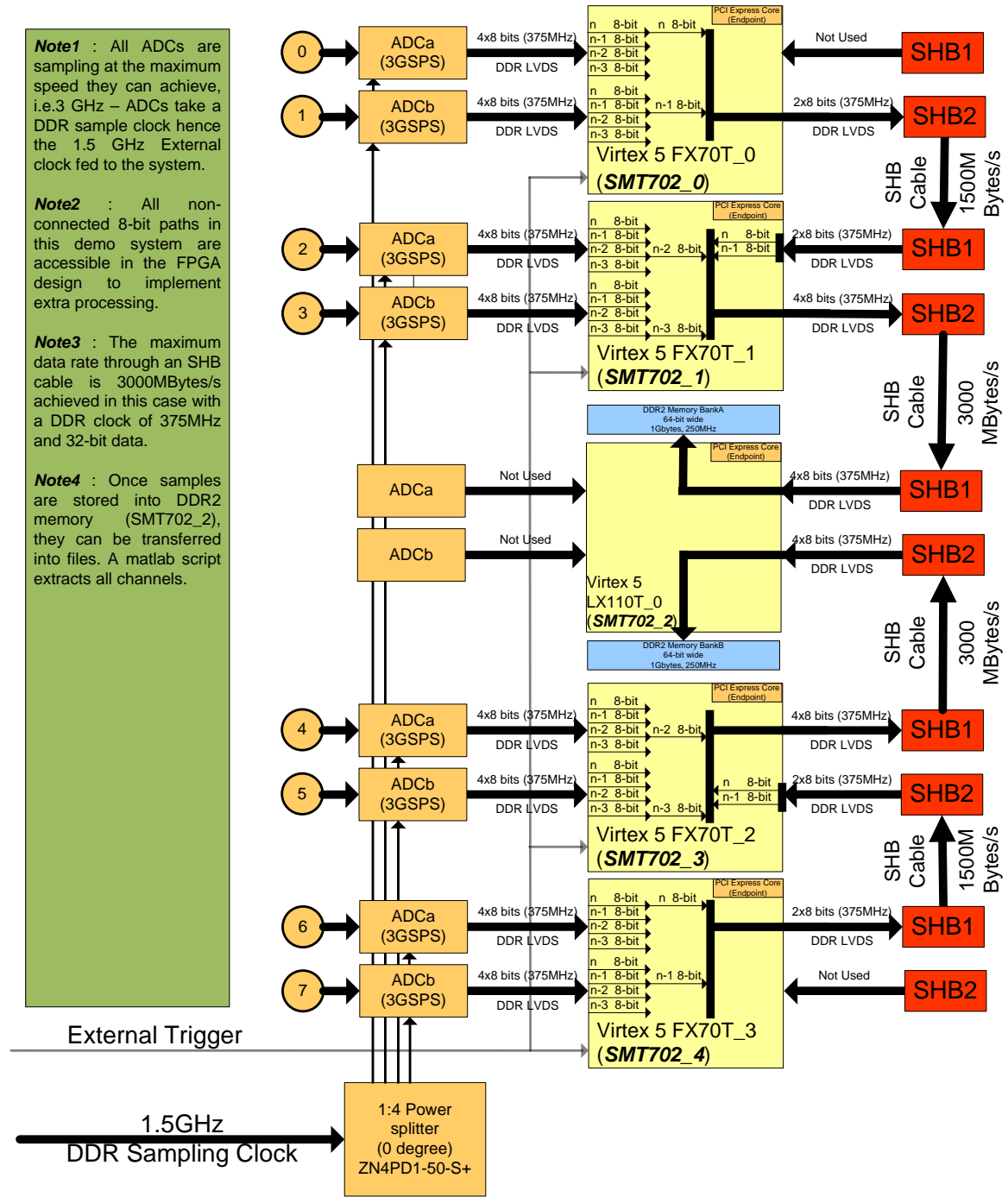
Document Title	Application Note - Multiple SMT702 System .doc				
Date	13/05/2010	Revision	1	Page	2 of 11

Note1 : All ADCs are sampling at the maximum speed they can achieve, i.e.3 GHz – ADCs take a DDR sample clock hence the 1.5 GHz External clock fed to the system.

Note2 : All non-connected 8-bit paths in this demo system are accessible in the FPGA design to implement extra processing.

Note3 : The maximum data rate through an SHB cable is 3000MBytes/s achieved in this case with a DDR clock of 375MHz and 32-bit data.

Note4 : Once samples are stored into DDR2 memory (SMT702_2), they can be transferred into files. A matlab script extracts all channels.



Document Title	Application Note - Multiple SMT702 System .doc				
Date	13/05/2010	Revision	1	Page	3 of 11

Hardware Setup

The system to be used is a PXI Express type chassis. Photos below have been taken based on the NI PXIe-1075Q, which is an 18-slot 3U PXI Express chassis. The FPGA's in the five SMT702's used are from Xilinx's Virtex 5 range, and are from left to right: XC5VFX70T, XC5VFX70T, XC5VLX110T, XC5VFX70T, XC5VFX70T. The SHB connections between the SMT702 boards will be described based on the location of the card from left to right, where the first card will be called 702_0, the next to the right will be 702_1, and so on. The firmware as provided depends upon an external trigger to be provided to each of the cards which are sampling data, and if the data is to be captured in synch there must be an external clock provided, although for demonstration purposes the onboard oscillators may be used.



Document Title	Application Note - Multiple SMT702 System .doc				
Date	13/05/2010	Revision	1	Page	4 of 11

SHB connections between boards

702_0 ⇔ 702_1	702_1 ⇔ 702_2	702_2 ⇔ 702_3	702_3 ⇔ 702_4
SHB2 ⇔ SHB1	SHB2 ⇔ SHB1	SHB2 ⇔ SHB2	SHB1 ⇔ SHB2

Here is clearly visible outside the rack how the SHB cables are connected.



The cables are routed up and over the railings between each slot.



Document Title	Application Note - Multiple SMT702 System .doc				
Date	13/05/2010	Revision	1	Page	5 of 11

Firmware Flow of Data

On each board there are two ADC's, each driven by the same external clock or onboard oscillator which can be selected by the Host software. Each 8 bit ADC provides a 1/8 speed data clock to the FPGA to clock 4 samples in time on every rising and falling edge, achieving a maximum performance of 3GB/s. The data clock is first locked into a DCM before it is used to latch in the ADC data. Due to this and the speed being handled, a phase shift of the clock is necessary to ensure the data is correctly latched between the rising and falling edge of the clock. This is easily performed by calibrating the DCM through the Host applications GUI.

As the board receives 4, 8 bit samples for every edge, but the SHB bus width is only 32 bits, the samples must be decimated in order to get samples from each of the 8 ADC's to the center, Host interface SMT702. This is achieved by taking one 8 bit sample in time for every four provided, and forwarding both of these channels onto the SHB bus with the clock that it was latched with so the delay relationship between the data and data clock remains the same. This enables samples to be provided from all of the 8 ADC's in the 4 outer SMT702's, sampling at 3GB/s, but the effective sampling frequency is reduced to 1/4 this speed to 750MHz. The block diagram illustrates this behaviour more clearly. To keep the ADC's on each board synchronized to each other, a trigger is expected during the ADC reset.

The forwarded clock over SHB must also be recovered in the same way that the data clock is recovered from the ADC's, by using a DCM with a phase adjustment, also adjustable by the Host software. Due to the fact that the data is captured with a clock that must be phase adjusted, any change in the sampling clock provided will result in a subsequent change being necessary in the DCM phase increment/decrement. The higher the frequency used to capture the data, the more sensitive the ADC's will be to this setting due to the shorter period.

Once configured by the Host, the 702_0, 702_1, 702_3 and 702_4 all continuously forward samples to the 702_2, which has all of its capture enable and store to memory functions controlled over PCIe from the Host software.

Document Title	Application Note - Multiple SMT702 System .doc				
Date	13/05/2010	Revision	1	Page	6 of 11

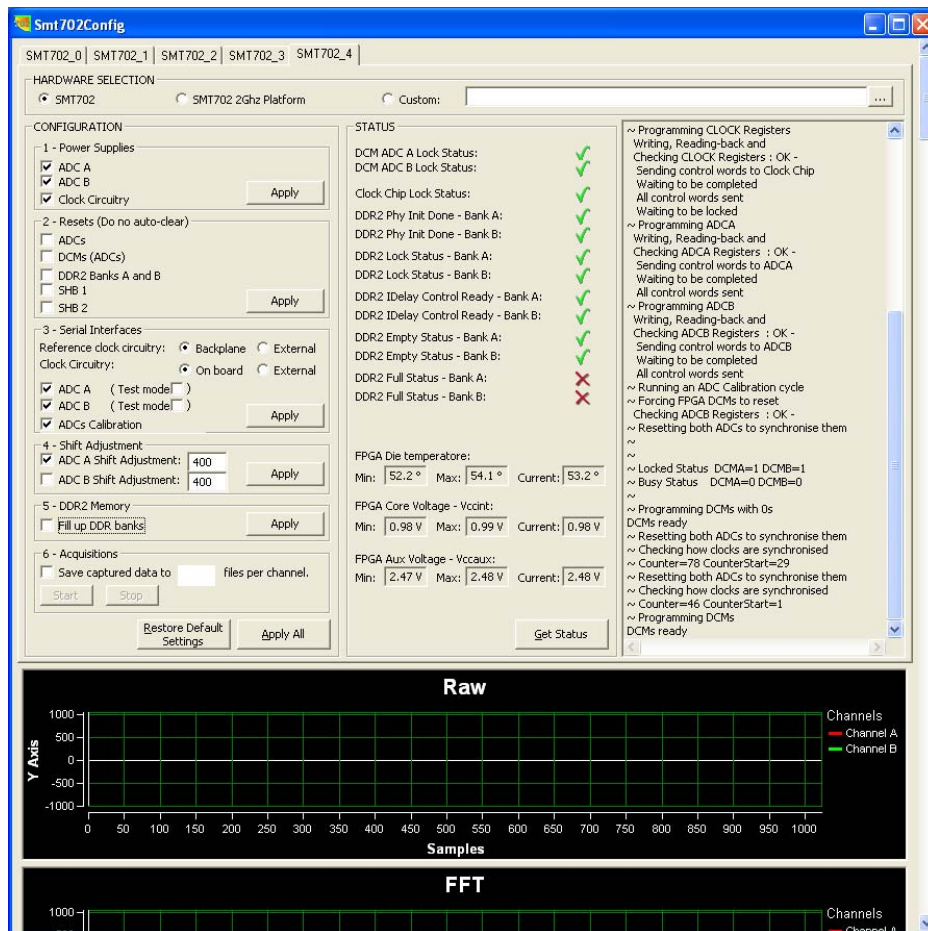
Software Setup

The Host application GUI was developed in Visual Studio C++ 6.0, and can be found under 'C:\Program Files\Sundance\SMT7026\Multi702\.'

Along with the Xilinx ISE 11.4 firmware project and the standard firmware for the single board default operation. The standard Host GUI project is under:

'C:\Program Files\Sundance\SMT7026\.'

Each of the boards are displayed and configured separately by tabs at the top of the GUI indicating the board which is currently being controlled. The intent of the GUI designed was to keep the control as functionally similar to the default SMT702 Host software as possible. Bearing this in mind, it is important to understand the firmware contents of each board to know which features are present and which are not, e.g., the center SMT702 (702_2) does not sample data and so does not have this capability in the firmware, so sending a reset to the ADC's or initiating a calibration cycle will likely cause the GUI to lock up. The following picture describes the setup for both the outer SMT702's (702_0 and 702_4) as they are both identical in firmware contents.



STATUS

When the tabs are first selected, all the 'STATUS' signals monitored in the FPGA are 'X', this is normal as all components are held in reset at power up. As the configuration is carried out the signals change to a green check mark to illustrate setup is complete. The 'Get Status' button can always be clicked as well to get an updated setting and view current measurements from the system monitor in the FPGA (temperature, voltage, etc.)

Document Title	Application Note - Multiple SMT702 System .doc				
Date	13/05/2010	Revision	1	Page	7 of 11

Power Supplies

Ensure each of these options are checked to allow proper power up of the board components. Press 'Apply' when complete.

Resets

Unless needed to change for a custom firmware or testing, each of these options should be unchecked before the 'Apply' button is pressed. The reset registers written to remain in reset until the check is removed and the 'Apply' button is pressed again.

Serial Interfaces

'Back plane' and 'External' are where the reference clock can be chosen from. The next 'On board' and 'External' radio buttons are the selection for where the sampling clock is to be provided from. If an external clock is being used, the 'External' button should be selected. Ensure 'ADC A', 'ADC B' and 'ADCs Calibration' are all selected before pressing the 'Apply' button. This will run the components through a set of resets and calibration sequences, then ensure the DCM's lock onto the data clock provided from the ADC's. At this point it is also important to verify the external trigger is connected before pressing 'Apply', otherwise the GUI is likely to hang on the first run due a reset being applied at this stage. This is dependent on the trigger to keep the ADC's reset at the same moment, ensuring close synchronisation.

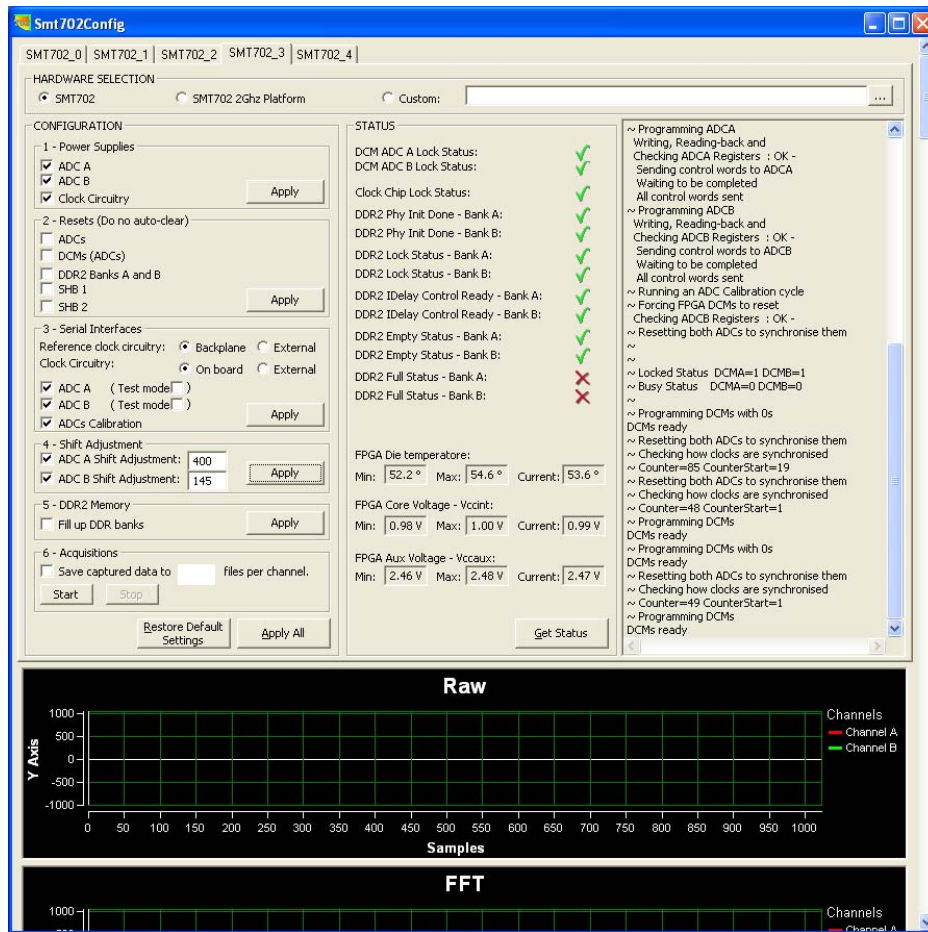
Shift Adjustment

'ADC A Shift Adjustment' corresponds to the data clock being locked onto from the onboard ADC's. 'ADC B Shift Adjustment' plays no role in this firmware and should remain unchecked. At the onboard sampling clock frequency of 1.5GHz, the shift adjustment needed is 400, but some adjustment will be necessary for different sampling frequencies. The shift values run from 0 to 511, and correspond to 1/256 of the sampling frequencies period, either positive or negative. The DCM data sheet provided by Xilinx can offer further insight into this feature if desired.

The remaining options should remain unchecked as these features are not used in the firmware, it only meant to configure and forward ADC samples onto the next board over SHB. General status and feedback to which operations are being performed are displayed to the far right window.

Document Title	Application Note - Multiple SMT702 System .doc				
Date	13/05/2010	Revision	1	Page	8 of 11

The following picture describes the setup for both the inner ADC sampling SMT702's (702_1 and 702_3) as they are both identical in firmware contents also.



All settings are the same for these two SMT702 and should be setup according to the 702_0 and 702_4 setup above, with the exception being the *Shift Adjustment* window.

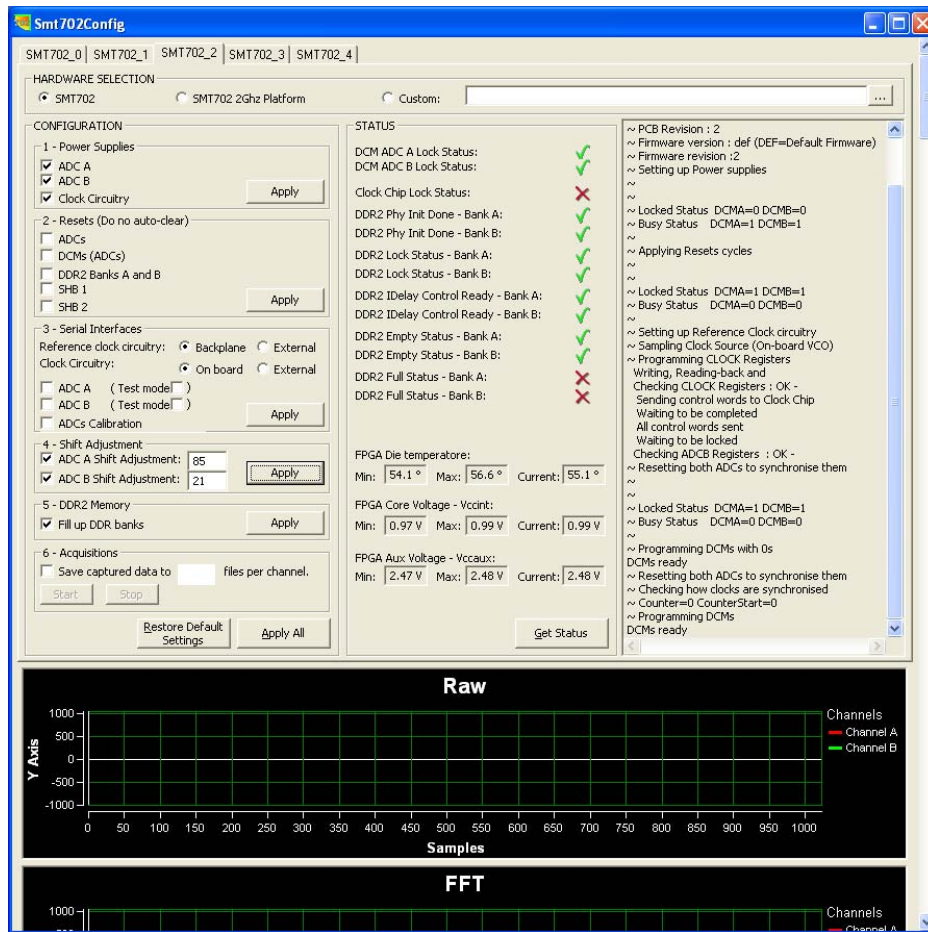
Shift Adjustment

As in the first boards setup, 'ADC A Shift Adjustment' corresponds to the data clock being locked onto by a DCM from the onboard ADC's. 'ADC B Shift Adjustment' in this case is controlling the DCM which locks onto the data clock being sent over SHB from either 702_0 or 702_4, depending on which is being setup at the moment. At the onboard sampling clock frequency of 1.5GHz, the shift adjustment needed for DCM A (ADC A) is 400, and the shift adjustment needed for DCM B (SHB data clock) is 145, but some adjustment will be necessary for different sampling frequencies or clock performance.

The remaining options should remain unchecked as these features are not used in the firmware, it is only meant to configure and forward ADC samples onto the next board over SHB, as well as received samples from the previous board over SHB. A delay is going to occur in the data samples as they are buffered through this board which can be perceived through closer analysis of captured data streams, and can be later removed by software if necessary. General status and feedback to which operations are being performed are as before, displayed to the far right window.

Document Title	Application Note - Multiple SMT702 System .doc				
Date	13/05/2010	Revision	1	Page	9 of 11

The following picture describes the setup for the center SMT702 that is providing the memory interface to the Host application GUI, and receiving all samples from the other four boards.



This configuration will be different from the other two because the ADC's are not being utilized; only the DDR memory and the DCM phase alignment are implemented.

First ensure the *Power Supplies* and *Resets* are applied as in the previous configurations.

Serial Interfaces

None of the ADC's are implemented with this firmware, so sending any of these commands will cause the GUI to freeze. Be sure to un-check each of the ADC options before clicking 'Apply'.

Shift Adjustment

'ADC A Shift Adjustment' corresponds to the data clock being locked onto from the SHB of the 702_1 board (left of the system), and 'ADC B Shift Adjustment' controls the DCM locking onto the SHB data clock from the 702_3 board (right of the system). The different phase adjustments are due to the different locations in the FPGA of the DCM's. At the onboard sampling clock frequency of 1.5GHz, the shift adjustment for A is 85, and the shift adjustment for B is 21. Some adjustment will be necessary for different sampling frequencies.

Document Title	Application Note - Multiple SMT702 System .doc				
Date	13/05/2010	Revision	1	Page	10 of 11

DDR2 Memory

This should be checked already; click 'Apply' to store samples to DDR memory from the 8 ADC's.

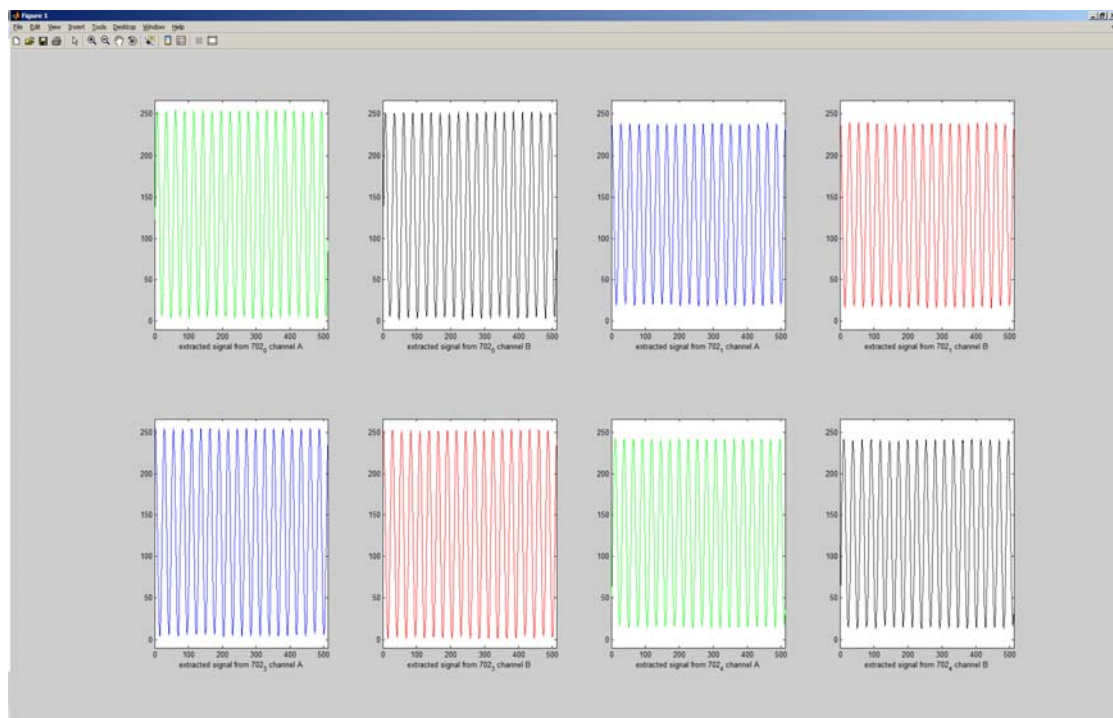
Acquisitions

This window allows the sampled data in memory to be stored into files on the Host PC, in the same directory as the executable for the GUI. Press 'Start' to verify samples are being retrieved from the 8 ADC's. The 'Raw' window will begin scrolling the samples as they are received over the SHB channel, so they will not be completely recognizable as the data which is being captured. To really view this data, check the 'Save captured data to' and place a 1 in the box to store one file with the samples. Press 'Start' to actually send the samples to the Host. Now the samples are ready to be viewed in MATLAB.

MATLAB

Any graphing software can be used to separate the captured data samples in order to display which ADC was capturing them, but in this case we will use the script, 'Display.m' to do it in MATLAB.

Open up a MATLAB session and place the captured files, 'smt7002_total_cha.txt' and 'smt7002_total_chb.txt' in the same working directory as the 'Display.m' script. In the Command Window simply type 'Display'. The following window should appear:



These are the sampled data from each of the ADC's as described in the window captions. If the data is not clearly visible, try adjusting the *Shift Adjustment* values accordingly to see if the DCM data clock can be locked a little more clearly.

Document Title		Application Note - Multiple SMT702 System .doc			
Date	13/05/2010	Revision	1	Page	11 of 11