APPLICATION NOTE 1

Application Note - SMT372T + SMT943

SMT943

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Introduction

In this application note is described how to set-up both the software and hardware required to run the demonstration provided with the SMT111 + SMT372T + SMT943 system.

The SMT372T is a multi-core DSP and FPGA processor board based on two of TI's C6472 DSPs (TMS320C6472)) and one Xilinx Virtex5 FX30T FPGA (xc5vfx30t-1-ff665). Channels of communication between the FPGA and DSPs include SRIO, UTOPIA2 to DSP A, I2C, HPI, and EMAC. Two 16-bit wide, 2Gb DDR chips are used providing 256MB of memory per DSP at 266MHz. The FPGA has additional links to Sundance RSL connectors, Ethernet PHY and an SLB to link to the SMT943 or any other one of Sundance's long list of mezzanine modules.

The SMT943 is a single width expansion TIM that plugs onto the SMT372T and incorporates 1 Texas Instrument dual-channel Analog-to-Digital Converter (ADS62P49) and 1 Texas Instrument dual-channel Digital-to-Analog Converter (DAC5688). The SMT943 implements a comprehensive clock circuitry based on a chip (CDCE72010) from Texas instrument that allows synchronisation among the converters and the use of an external reference clock or sampling clock. It provides a complete conversion solution and stands as a platform that can be part of a transmit/receive base station. The SMT943 has an on-board VCXO of frequency 491.52MHz. The SMT943 module is well-suited for multi-carrier, wide bandwidth communication applications.

For further information regarding the SMT372T see:

http://www.sundance.com/web/files/productpage.asp?STRFilter=SMT372T-FX30

For further information regarding the SMT943 see:

http://www.sundance.com/web/files/productpage.asp?STRFilter=SMT943

Hardware Set-up

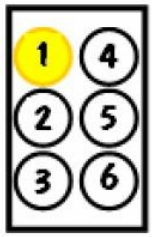
The system demonstration runs on the hardware using CCSv4 as a debugging tool to load and run the application into DSP A. The application in DSP A in turn controls the firmware registers in the FX30T that program and enable the DAC, ADC, and clock circuitry of the SMT943. The SMT372T's FPGA configures itself from flash at power up with the necessary firmware when the hardware is received. If desired, it is possible for the user to load a custom bit-stream into the flash of the TIM. To gain access to the flash, the user must use JTAG to configure the FPGA with a new firmware that creates a link from the Comport to the flash to utilize the capabilities of the SMT6002. Please also ensure that SW1 settings are "1=OFF, 2=OFF, 3=ON, 4=OFF.

- Open iMPACT and program the FPGA with: C:\Program Files\Sundance\SMT6002\Firmware\Smt372T\flash.bit
- Launch the SMT6002 Flash Programming Utility.
- Once the board is detected, the window presented will display the loaded bit-stream in flash. If you want a different one, select the current bit-stream, click 'Delete', then select 'Add'.
- The new window will allow you to select the new bit-stream to load. Choose 'Basic', and select position '1'. Click 'Okay', and then 'Commit'.

When the tool has completed loading the new custom bit-stream, re-power the board and the FPGA should be configured with the newly loaded firmware. Because the FPGA configures itself from flash and is not managed by a CPLD as in other Sundance TIM's, there can only be one firmware loaded at a time, in position 1. For further information on the SMT6002, see the SMT6002 Help.

The following is the pin-out for connecting to the FPGA JTAG chain

Signal	Pin	Pin	Signal
VCC	1	4	TMS
GND	2	5	TDI
TCK	3	6	TDO



The SMT943 SLB should be placed on top of the SMT372T with two extenders placed between them to allow room for the large voltage regulators on the base board. Channel A and channel B of the mezzanine are the ADC's, and should be provided with a signal generator source not to exceed 2.4vpp. The gain settings may be adjusted in the software later if desired to provide a different source level. The demo design will route the incoming ADC samples to the output DAC channels C and D. These two outputs should be connected

to an oscilloscope to verify correct operation. Keep in mind the sampling frequency in the demonstration is 250MHz when choosing a frequency to provide to the system.

The two DSP's and FPGA can get very warm when power is applied. The mezzanine has a fan already dedicated for cooling, but care should be taken to ensure there is adequate cooling between the two boards to maintain the base boards larger processors at an acceptable operating temperature, especially if additional functionality is to be added in the future.

The DSP JTAG emulator for debug should be attached to the JTAG1 connector of the SMT111 prior to attempting the software set-up.

For help in locating connectors or features of the board, refer to the EVP6472 website:

http://www.evp6472.com/

Firmware

An ISE11.4 project is provided with the system demonstration for investigation or modification by the user. It will be loaded into flash to configure itself at power-up when received.

All functionality of the mezzanines clock circuitry, ADC's and DAC's are controlled by the DSP application to the registers of the FPGA. For a detailed understanding of the registers in firmware for controlling the SMT943, please visit our website for the Product Manual:

http://www.sundance.com/docs/SMT943%20User%20Manual.pdf

Software Setup

The base board's DSP A directly controls all the register level settings for the mezzanine through the HPI link to the FPGA. The HPI interface by default is a slave peripheral to the DSP from the FPGA, yet the DSP needs to control the FPGA through this port. We achieve this by setting aside a block of memory in the DSP which the firmware in the FPGA will monitor for instructions and respond to the DSP through. A communication structure similar to how Diamond communicates with its Host Server is utilized, only the FPGA is viewed as the Host would be after a program has been loaded.

Before this protocol can be utilized, the FPGA needs to be powered up and a reset through SW2 of the SMT111 be applied. When the reset is released, the FPGA will run through a sequence which configures the DSP's external memory with the addresses which will be monitored for this communication, as well as configure the DSP's internal PLL's to communicate at a faster speed. The process can be observed by watching the LED's D7 and D9. The 25MHz clock on the base board will stay steady and cause D7 to blink, but D9 will blink faster after reset as the PLL's will be configured from 4.6MHz to 50MHz.

The communication structure of the HPI link works by setting aside eight consecutive address locations in external memory:

Write Addresses	**Write Structure**
0xE0000000	number of bytes to write
0xE0000004	address of where to start writing to the FPGA from
0xE0000008	address for the FPGA to indicate when a transaction is complete
0xE000000C	default write complete address pointed to by FPGA at initialization

Read Addresses	**Read Structure**
0xE0000010	number of bytes to read
0xE0000014	address of where to write to the DSP from the FPGA when reading
0xE0000018	address for the FPGA to indicate when a transaction is complete
0xE000001C	default read complete address pointed to by FPGA at initialization

The FPGA is preconfigured to write **0xE0000020** to the start address write structure (0xE0000004). It is also preconfigured to write **0xE0001024** to the start address read structure (0xE0000014). These are the locations the DSP will write and read all transaction to and from the FPGA. To indicate to the FPGA that a transfer is ready, the DSP needs to write an interrupt to the HINT bit of the HPIC register within the HPI peripheral. The DSP in turn will wait for the done complete bit to go high in either the write or read address pointed to by the communication structure before clearing this bit and moving on to the next instruction.

Once the board is powered up and the DSP is initialized, launch CCSv4 and open up a Workspace. Once in the workspace, create an empty project with the default settings, and import the provided archive file, "SMT372T_SMT943.zip". Within this project is the header files which describe the addresses and behaviour of the mezzanine, along with a target configuration file for connecting to the system using a SEED USB XDS560PLUS emulator. If a different emulator is to be used, create a new target configuration file according to the manufacturer's instructions. Make sure the correct configuration file is selected as the Active, Default file for connecting.

Once all the set-up is complete, run a clean build to ensure the project copied over correctly. Then select 'Target' -> ''Debug Active Project"

The Debugger will establish a link with each of the internal processor cores of both DSP's, but the application will only be loaded into Core 0 of DSP A.

Once the emulator is connected and the debugger started, press the “play” button to run the program.

The application will step through the initialization and set-up of the configuration registers and program the clocks to run at the right speed. The Console will indicate each step of the set-up progress and whether or not it was successful. By default, the program simply routes the ADC input to the DAC output, so once the configuration is complete and the DSP application has quit, the input signal generator source should be visible on the connected oscilloscope from the DAC output. Take note – The input to ADC A is output DAC D, and the input to ADC B is routed to DAC C.