APPLICATION NOTE

Application note about SMT702_SMT712 System: 2-Ghz Platform

SMT702 and SMT712

SUNDANCE MULTIPROCESSOR TECHNOLOGY LTD.

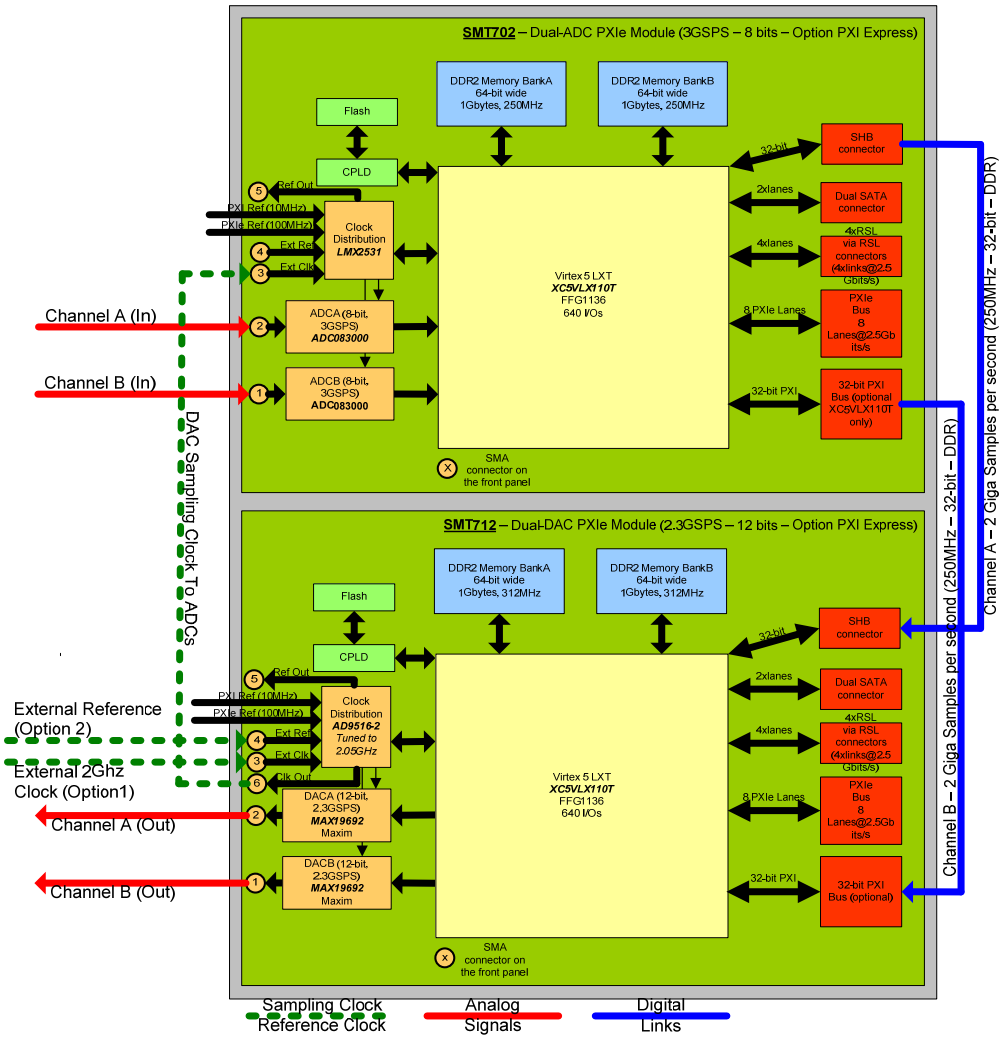
Date	Comments / Changes	Author	Revision
12/03/10	Original Document completed	PhSR	1
08/06/10	Replaced photos, added details	PhSR	2

The 2-GHz platform is a system that is composed of one SMT702 (PXI Express – FX70T or LX110T FPGA), which integrates two fast 8-bit ADCs (3GSPS) and an SMT712 (PXI Express – FX70T or LX110T FPGA), which integrates two fast 12-bit DACs. Both modules integrates also a clock circuitry, 2 banks of DDR2 memory (1Gbyte each), a 4-lane PXI Express core and 2 SHB connectors (32-bit bus, Double Data Rate).

Resources left available in the FPGAs can be used to implement some processing to combine channels and/or reduce the amount of samples, as an example.

System Block Diagram.

The diagram below shows the connections between both boards (SMT702 and SMT712).



2-GHz Dual ADC to DAC Channel Platform. In this system, ADCs and DACs are sampling at the same rate.

Option 1 : Using an external 2-GHz Clock. The clock is fed to the DAC module (SMT712 – Dual DAC option PXI Express – XCV5LX110T FPGA), routed to the DAC chips and also passed to the ADC module (SMT702 – Dual ADC option PXI Express - XCV5LX110T FPGA).
Option 2 : Using an external Reference, fed to the DAC module (SMT712 – Dual DAC option PXI Express – XCV5LX110T FPGA) and used to lock the built-in clock chip VCO to generate a stable 2.05GHz internal clock. The clock is routed to the DACs and passed to the ADC Module (SMT702 – Dual ADC option PXI Express - XCV5LX110T FPGA). Note that for this option the sampling frequency will be 2.05GHz otherwise the clock chip would need to be replaced by AD9516-3 instead of a AD9516-2 as standard.
Notes : For both options, samples are transferred using 2 'internal' SHB links. One of them will be replacing the the 32-bit PXI bus. Each module is to be plugged in a PXIe chassis (for example : http://sine.ni.com/nips/cds/view/p/lang/en/nid/202664). Each module takes the space equivalent to 2 slots. Configuration and setup is made via PXI Express bus from a host module. 8-bit samples coming from the ADC are routed straight to the DAC MSBs. Both DACs need to synchronised because they use a 4:1 mux before any transfer happens – it will be ensure by a scheme implemented in the FPGA.

In this system there are several clocking options as described above. In all cases the DAC module (SMT712), generates the sampling clock for its own converters as well as for the SMT702. An external cable is used to carry the sampling clock (SMA-SMA cable).

ADC samples are moved to the DAC using 2 DDR SHB links (32-bit parallel bus). When the DACs are clocked at 2GHz, samples travel at 1/8th of this frequency on the SHB, i.e. 250MHz DDR. It is to be noted that the SHB links have been tested at 375MHz in DDR mode 32-bit, which is the speed required to output all ADC samples when clocked at the maximum rate (3GHz), meaning that the system can therefore be clocked faster.

ADCs have a resolution of 8 bits whereas the DACs have a resolution of 12 bits. ADC samples are copied onto the DAC MSBs and the LSBs are hardcoded with 0x4 (4 in hexadecimal).

Modules don't require any specific firmware to work as a 2-GHz platform, default versions implement all the necessary options.

The block diagram shows one SMT702 and one SMT712 connected together. FPGAs implement the default firmware and therefore only the remaining logic can be used to add extra processing. An extra board could be added in the system per data path for extra logic and without worrying about converters, PCIe interfaces, etc. This would add extra latency between the ADC inputs and DAC outputs.

Hardware setup.

The system is composed of:

1 - 1xSMT702,

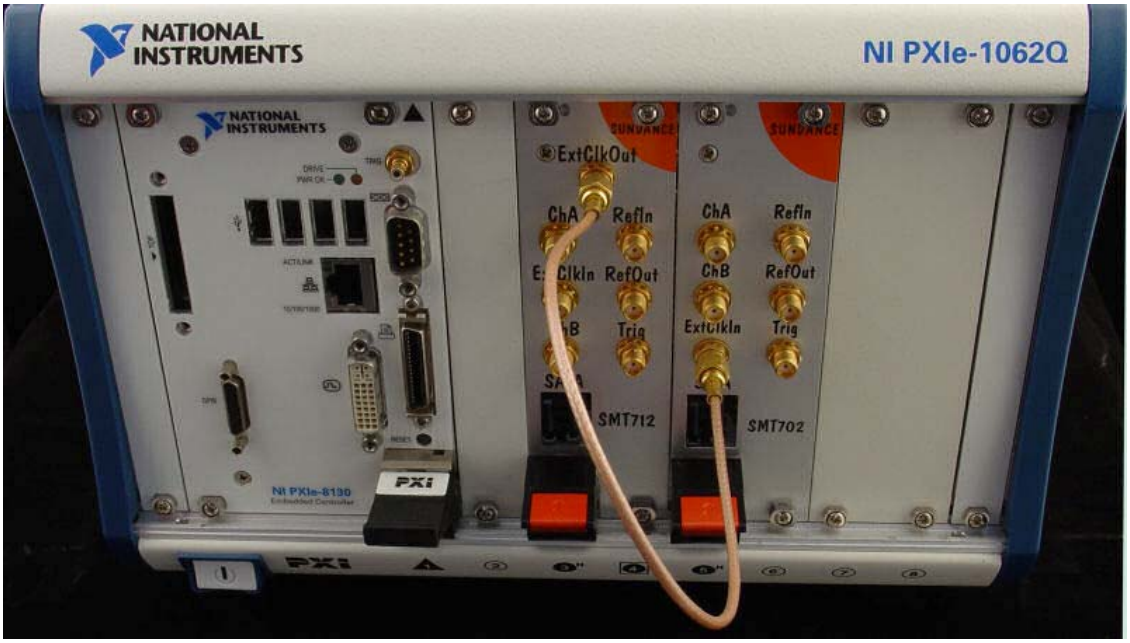
2 - 1xSMT712,

3 - 2xSMT511-320,

4 - 1xSMA-SMA cable.

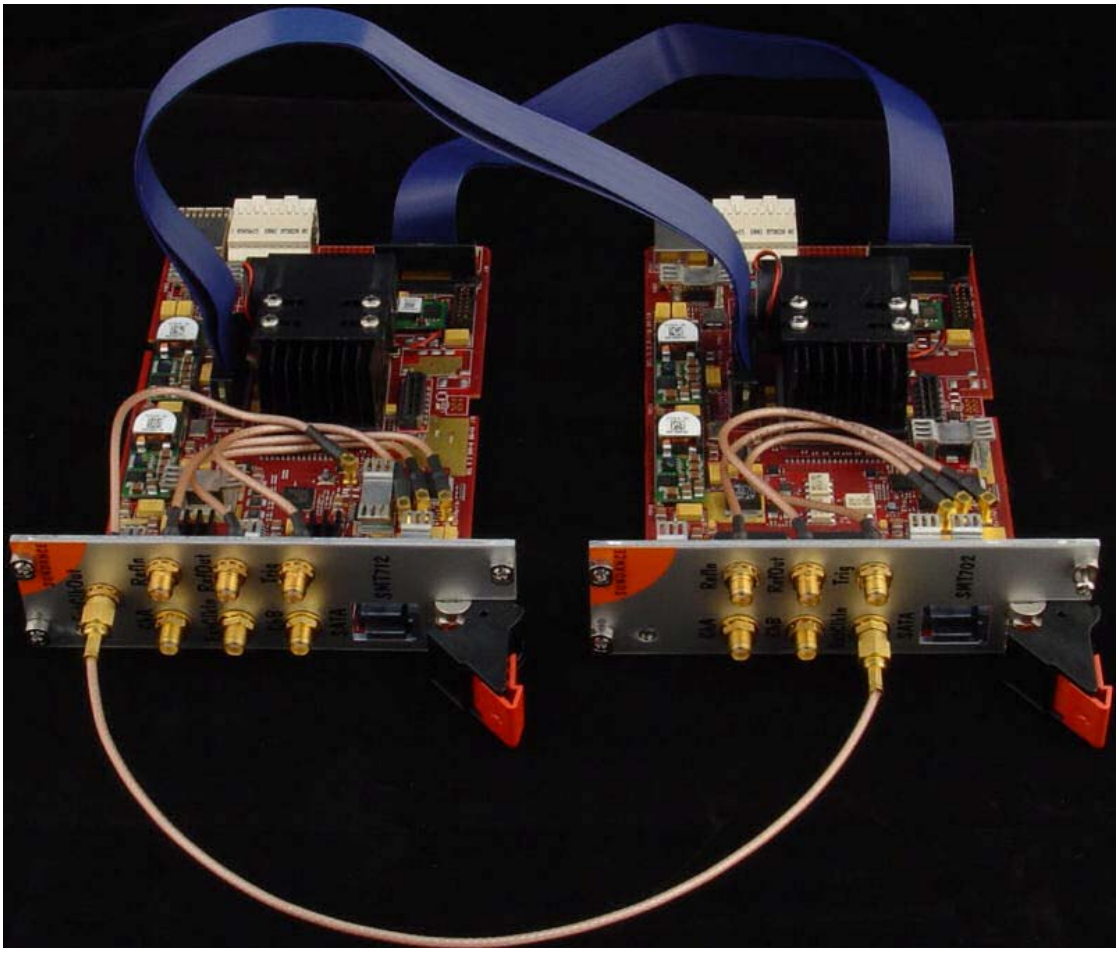
In this section is described how they are connected together.

The system to be used is a PXI Express type chassis. Photos below have been taken based on the NI PXIe-1062Q, which is an 8-slot 3U PXI Express chassis. Boards can be fitted either way in the rack.



The SHB connections (2 SHB cables required – 320mm long – Straight connectors – ***SMT511-320***) between the boards are shown below.

SHB1 (SMT702) is connected to SHB1 (SMT712) using a first cable and SHB2 (SMT702 is connected to SHB2 (SMT712) using a second cable.



In order to ease the routing of the cables, some of the plastic rails to slide the cards in can be removed (Cards are double-width and only one every two rails is used). Make sure that none of the cables gets caught between the module connectors and the backplane when pushing the cards in.

Empty slots can be filled with plastic blockers (blue plastic boxes on the next photo). They will improve the air flow and contribute to a lower system temperature. Fitting spare front panels will also improve the air ducting and therefore system heat extraction.

A short SMA-SMA cable is required to link the external clock output of the SMT712 to the External clock input of the SMT702.

Note: Instead of removing the plastic rails to pass the SHB cables, the cut-out on the SMT712 (near one of the power modules) can be used. Great care must be taken when passing the cable in order not to damage them (sharp PCB edges).

Software setup.

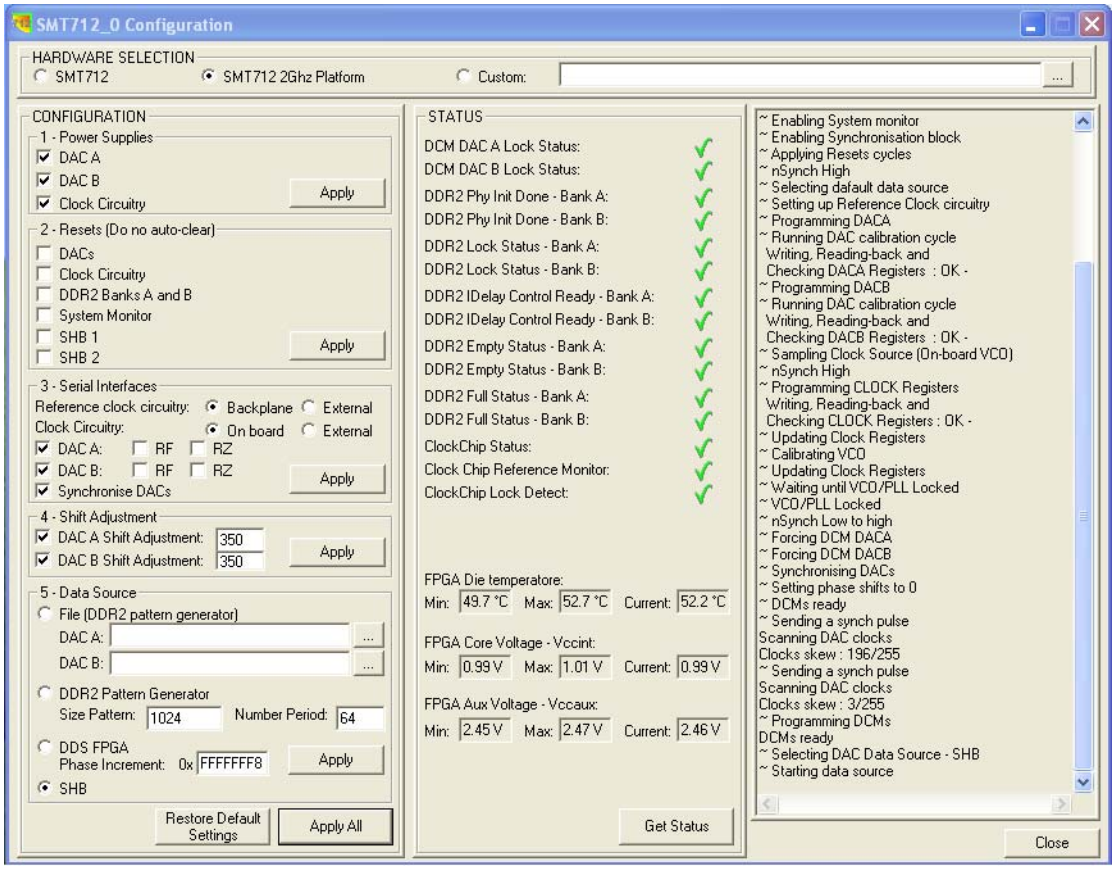
The software setup starts by installing the Sundance Wizard from a CD provided or from our website.

The Wizard will show you what can be installed. SMT6300, SMT6002 and SMT7002 (or SMT7026, basically the same as SMT7002 but includes software source code of the host applications) are required. Other packages can be skipped.

You might be asked to reboot the system once all pieces of software are installed.

Part of the SMT7002 and SMT7026, are 2 host applications. The first one (***SMT702 Configuration***) is to control the SMT702 and the second (***SMT712 Configuration***) is to control the SMT712. The 2-Ghz platform needs to have the SMT712 configured first as it also generates the sampling clock for the SMT702.

SMT712 Configuration. In the start menu, under Sundance – SMT7002 (or SMT7026), you can launch the application to configure the SMT712:

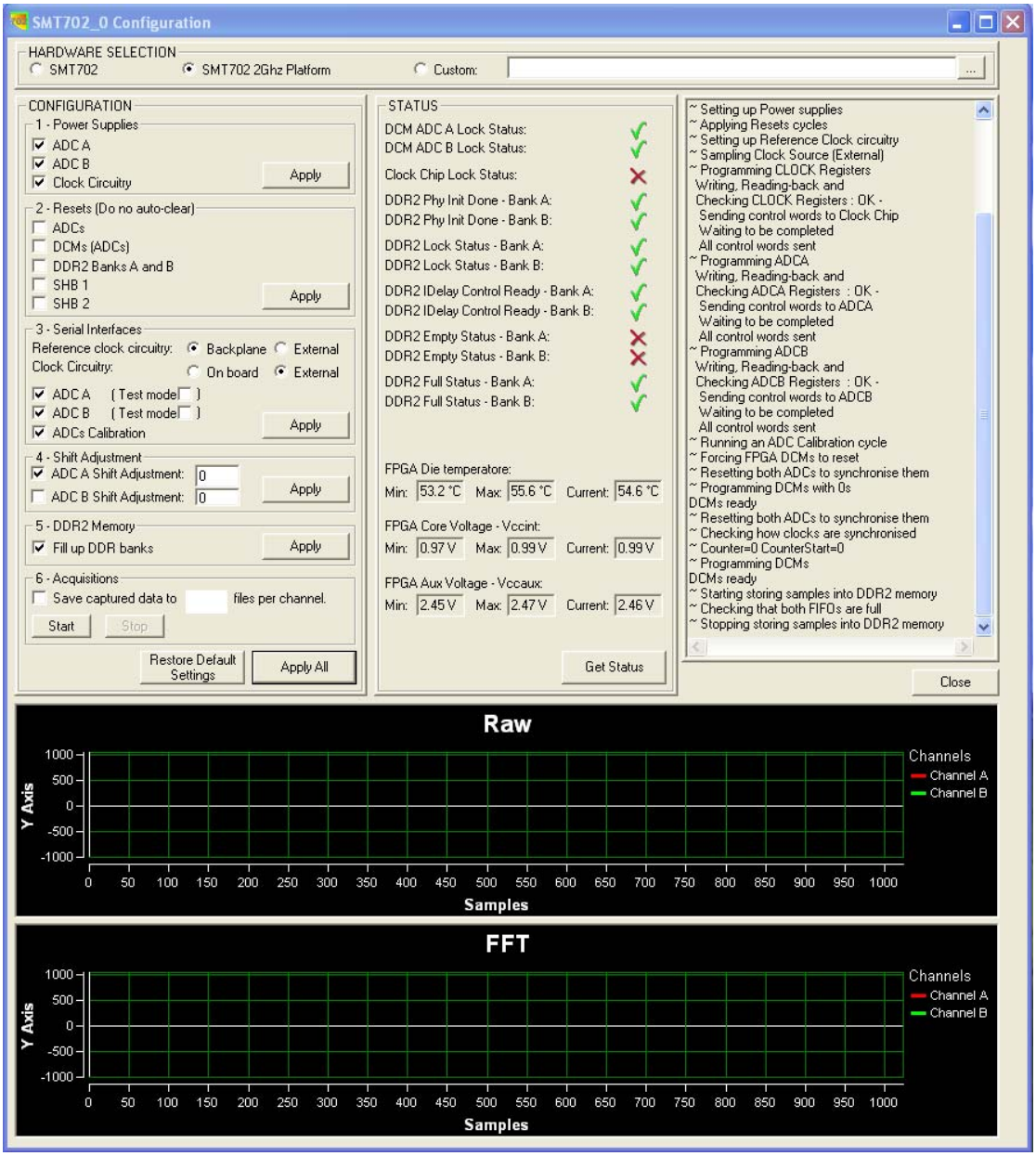


Depending on the hardware selection (SMT712, 2GHz platform or Custom), options will be ticked or not. Parameter can also be read from a file (Custom). Once the hardware selection is made (***SMT712 2GHz Platform*** in our case), you can press '***apply all'*** to execute the commands. The Status column gives a feedback of the clock chip, FPGA DCMs and the DDR2 blocks. The FPGA die temperature is also display, clocking on 'Get Status' updates it, as well as the FPGA core and aux temperatures.

The SMT712 FPGA temperature stays below 70 degrees in a 25-degree environment. The rack has got a switch at the back to have cooling set to maximum or automatic. The second position works fine and has been used to develop this system.

In the log column, more details of the functions executed are given.

SMT702 Configuration. In the start menu, under Sundance – SMT7002 (or SMT7026), you can launch the application to configure the SMT702:



Identical options are available. Once the hardware selection is made (***SMT702 2GHz Platform*** in our case), you can press '***apply all'*** to execute the commands. The Status column gives a feedback of the clock chip, FPGA DCMs and the DDR2 blocks. The FPGA die temperature is also display, clocking on 'Get Status' updates it, as well as the FPGA core and aux temperatures.

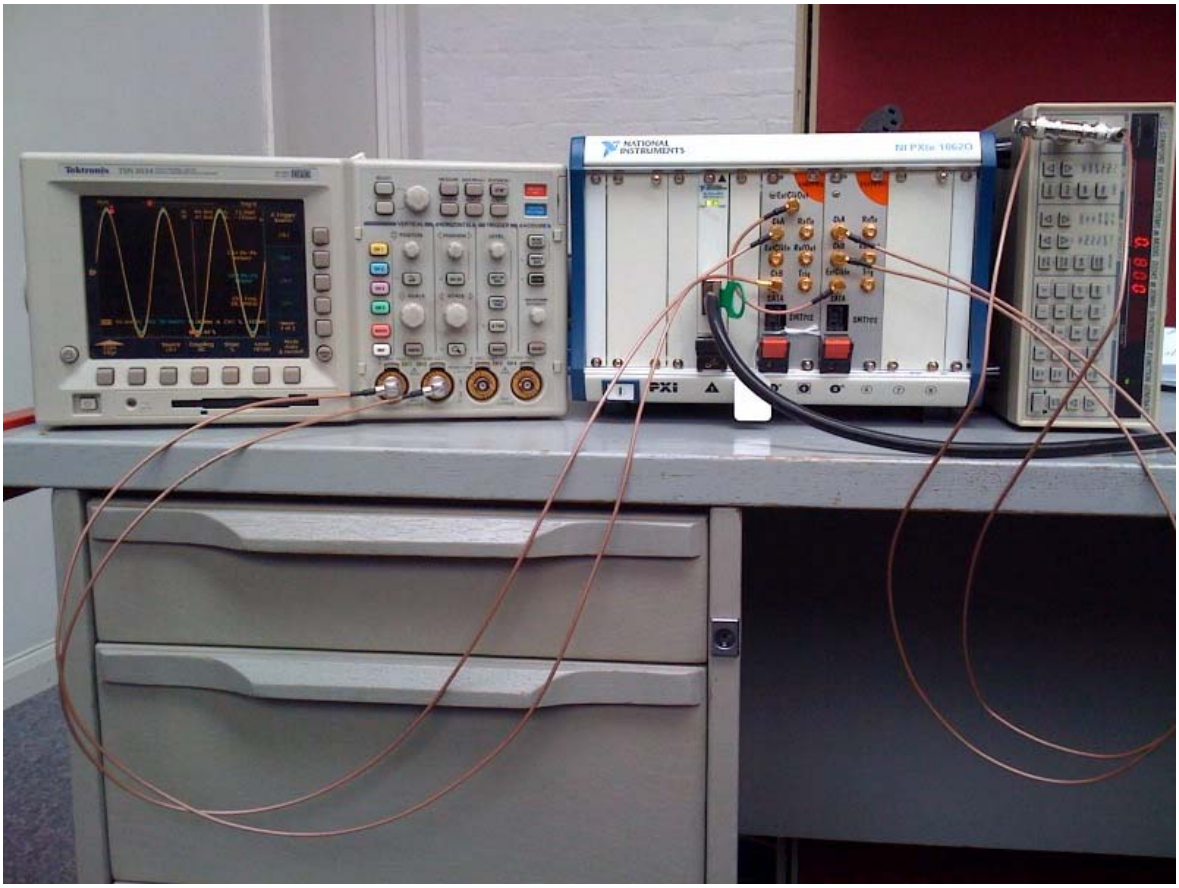
The SMT702 FPGA temperature stays below 65 degrees in a 25-degree environment on the automatic fan position.

In the log column, more details of the functions executed are given.

At this stage the system is configured and working. You can feed a signal in the ADCs and it will come out on the DAC outputs with a latency.

System running.

Once the system configured, the signal generator can be turned on:



System Latency.

The SMT702 firmware (default firmware - revision 3) routes the samples coming out of the FPGA to the SHB connectors going through a few rows of flip-flops.

The SMT712 firmware (default firmware - revision 3) takes the samples coming from the SHB connectors and routes them to the DACs. A few rows of fli-flops are used as well, on top of a FIFO that is only used to re-synch data flows. Only one data at a time is stored in the FIFO, avoiding uncertainty along the data path.

The latency measured using the default firmware is 86ns.

It can be brought down to just over 60ns (as shown on capture below) by removing the FIFO and some of the flip-flops. This would put more effort on the routing of the design. Below is a screenshot of what have been probed (input SMT702 in blue and output of SMT712 in green)

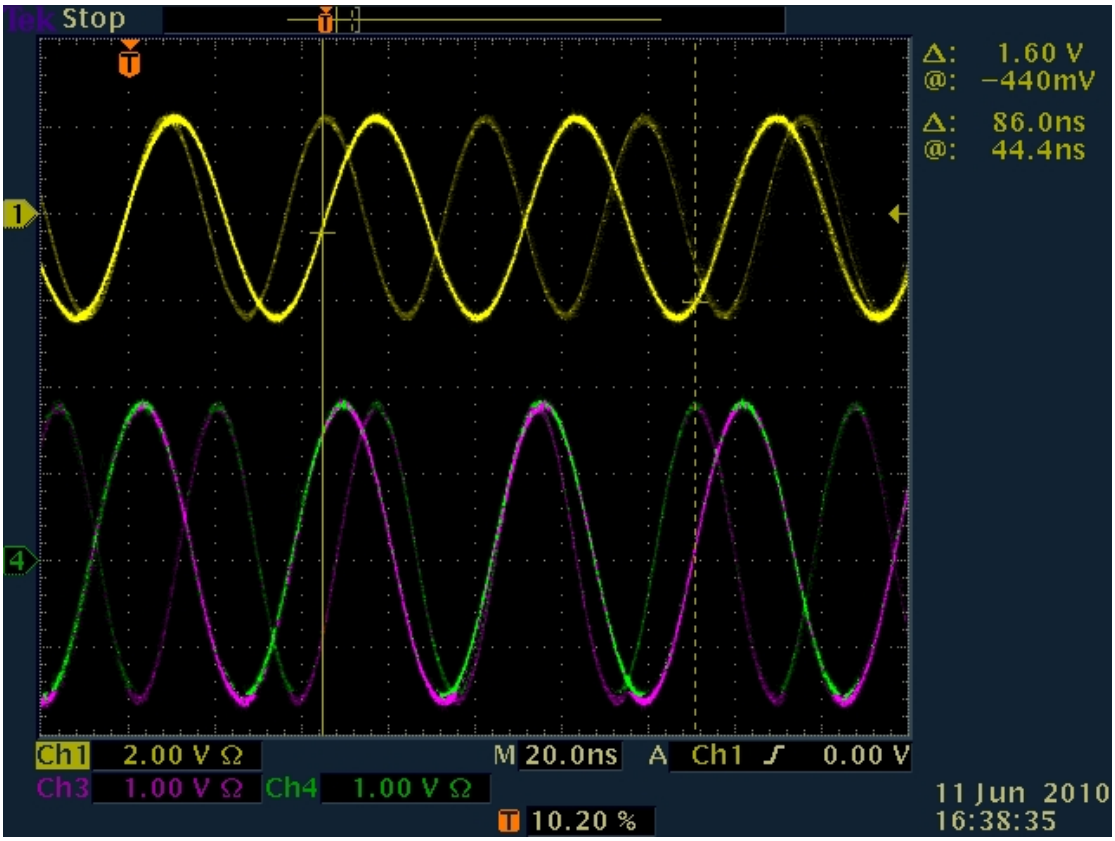


Figure 1 - 86ns latency.

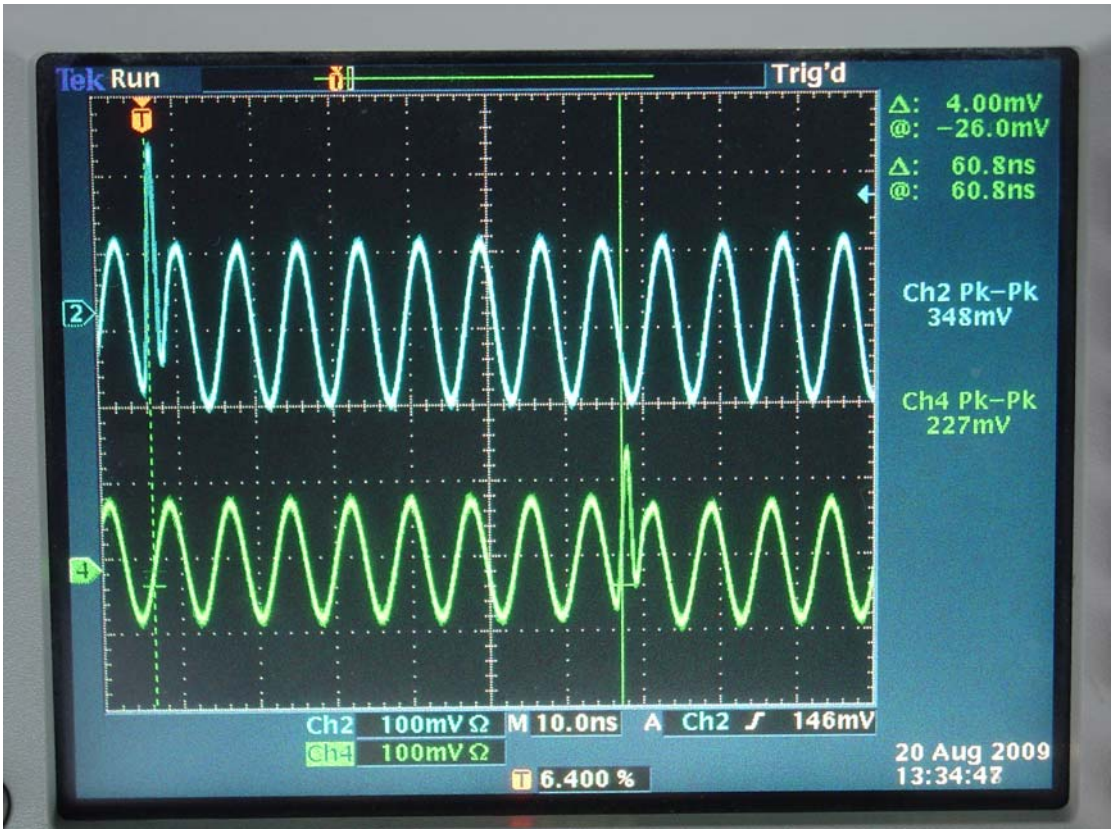


Figure 2 - 60.8ns latency.

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