

# APPLICATION NOTE 2

Application note about bitstream download software

## SMT3x8 FPGA Configuration

SUNDANCE MULTIPROCESSOR TECHNOLOGY LTD.

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## Configuration of the SMT3x8 FPGA

This document describes how to generate a file that can be downloaded to the SMT3x8 FPGA using a DSP TIM as the bitstream loader.

Examples are provided in SMT6500 package available from SUNDANCE at: SMT6500\SMT3x8\Source\Loaded and SMT6500\SMT3x8\Source\Embedded.

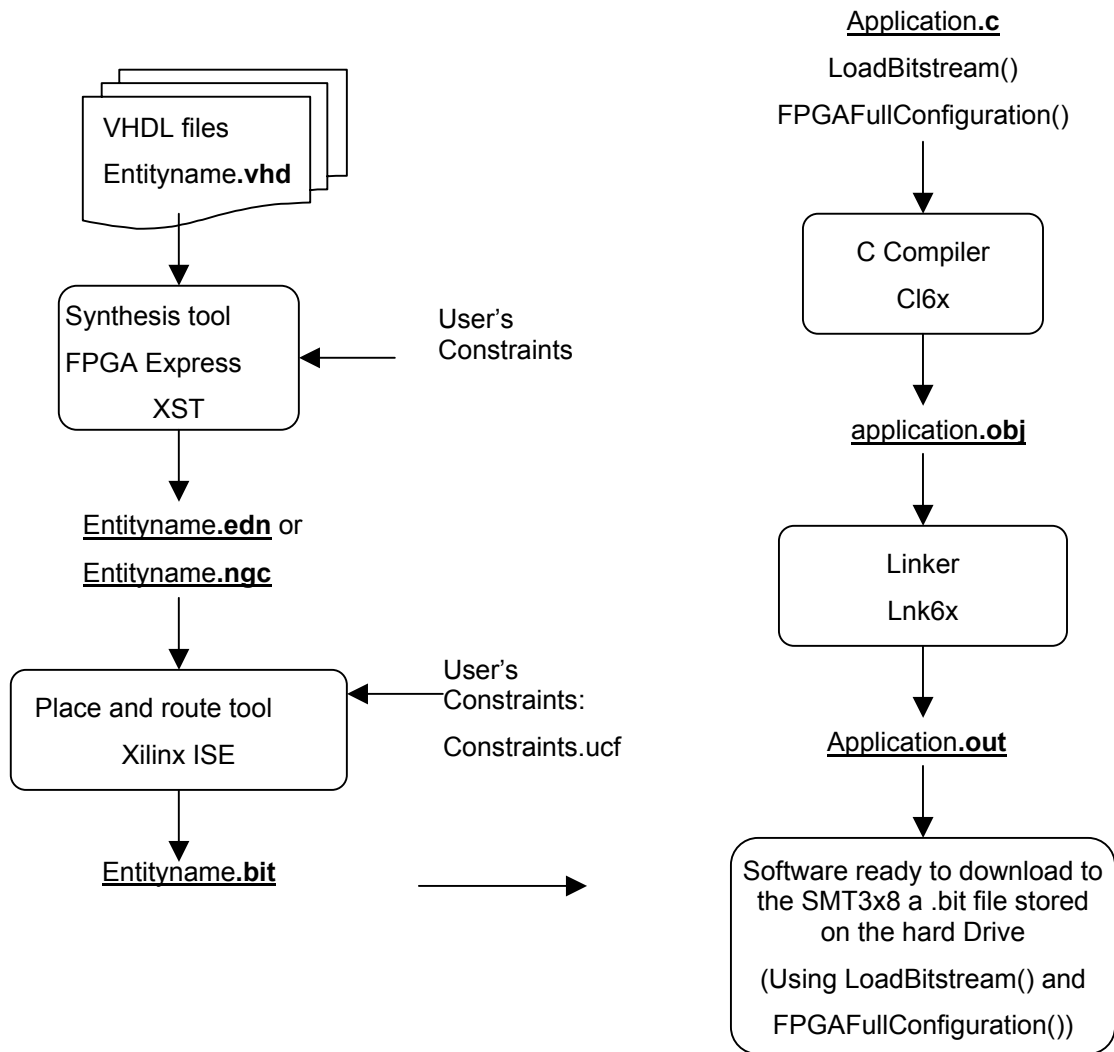
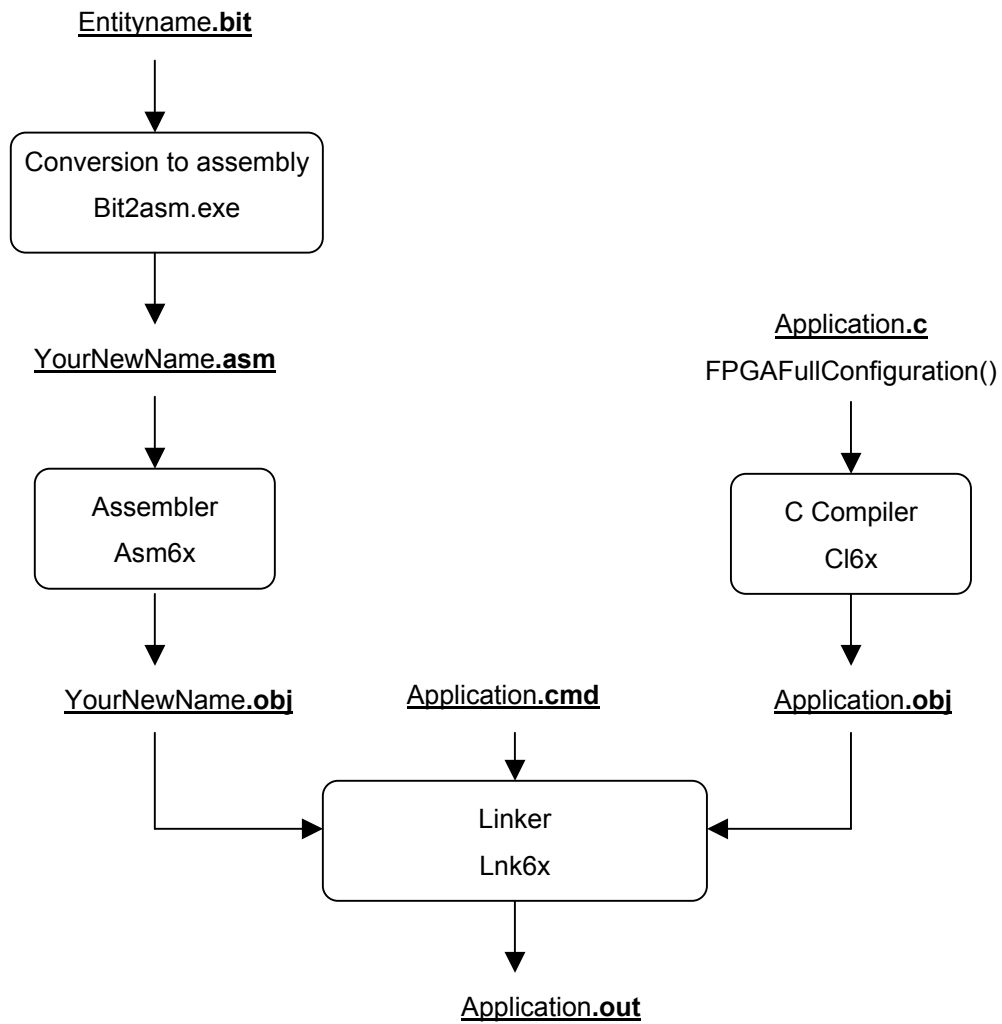


Figure 1: Bistream Loaded using a DSP TIM

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**Figure 2: Bitstream Embedded on a DSP TIM.**

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## The Bitstream formatting

The FPGAFullConfiguration() function: is a necessary step to make.

It formats your bitstream file so that it can be downloaded over Comm-port 3 to the SMT3x8 and configures the FPGA as shown in [Figure 1: Bistream Loaded using a DSP TIM](#).

- The conversion function is needed AFTER a bitstream (.bit file) has been generated by Xilinx Place and Route tools..

Therefore some additional software is required:

- A CAD platform to create a schematic or VHDL design.
- A simulator to simulate the hardware designs.
- Xilinx Place & Route software ISE 5.2i.
- Texas Instrument C compiler and/or 3L parallel C compiler and/or Sundance.

The bitstream that is used to configure the FPGA on the SMT3x8 is built using Xilinx Design implementation tools for FPGAs ISE 5.2i.

Follow these steps to build a bistream that can be downloaded on the SMT3x8.

1. Select your design available in edif format (filename.edf or filename.ngc) with the Xilinx tools.
2. Target the constraint file provided with the SMT3x8 to map your design to the FPGA 's I/O pins (comment out all the I/Os that your design doesn't use)
3. Run Xilinx Design implementation tools.
4. Next, the bitstream is generated (Entityname.bit). The bitstream is a binary image of the VHDL core.
5. The .bit file can be read from your Hard Drive using the function LoadBitstream(). The bit file is now stored on the DSP TIM in internal/external memory.
6. The bit file can now be formatted and written over a ComPort (by the DSP) using the function FPGAFullConfiguration ().
  - It looks for the bitsream start sequence using function StartSequence(unsigned char\* buffer, int lenght)
  - It sends the start key and the end key (if requested) using link\_out\_word(data, nConfig\_port).
  - It formats the bitstream and sends it over ComPort using function FPGAWrite (int nConfig\_port, unsigned char\* buffer, int bytcount, int log)
  - FPGAWrite calls Bitrev(unsigned char ByteValue) to invert the bits in a byte, inverts the bytes in a 32-bit word and writes the 32bit words over ComPort using link\_out\_word(data, nConfig\_port).

At this stage, the SMT3x8 receives the bitsream on ComPort 3 and configures the FPGA..

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Nevertheless, the more gates the FPGA has, the bigger the bitstream is, and therefore the longer the download of the .bit file is going to take because:

1. The read from the hard Drive is not a fast process when operated remotely from a DSP over the PCI.
2. When using CCStudio to run the program on a DSP that reads the bitstream from the hard Drive, the bitstream is downloaded via JTAG, which can take many minutes.

That is why the bitstream file can be embedded in the application downloaded on the DSP TIM module to allow a much faster configuration process.

### **The Bit to Asm Conversion**

**Users need to have CCStudio installed, even if they prefer working with 3L as the bit to asm conversion requires an executable installed under CCStudio. (Asm6x.exe)**

The speed of the FPGA bitstream loading operation onto the DSP TIM can be highly improved by loading it as a data section during the program loading operation. It is therefore converted to an assembly file and directly linked to the application file as shown in **Figure 2: Bitstream Embedded on a DSP TIM..**

The “. Bit” needs to be converted in an “. obj” file so that it can be linked with the DSP application and be part of the “.out” application or of the “.app” application that is run under 3L, for configuring the SMT3x8 FPGA.

Then the download of the bitstream is speeded up because the bitstream is read out of the DSP board on-board memory instead of being read out of the Hard Drive.

The download is instantaneous if the following method is used:

1. Format the YourNewName.bit to an YourNewName.asm file with the standalone application Bit2asm.exe. To do so, you need to modify the Makefile provided.
2. The command line used is made of 3 parameters:
  - a. The name of the “.bit” file. Any name is valid.
  - b. The name of the “.obj” file. Any name is valid.
  - c. A number associated to the bitstream.
    - i. The number must be greater than or equal to 1.
    - ii. 0 will generate an error.
    - iii. To remain compatible with bit2asm version 1, if only 1 bitstream is to be downloaded then **you can** leave the “number” field blank. (the number may be omitted). Therefore the command would only remain with 2 parameters.
3. Place the file(s) YourNewName.bit in the folder containing the executable file Bit2asm.exe.

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4. Edit the file Makefile.
  - a. Replace "**bit2asm bitfilename.bit bitfilename.asm**" by "Bit2asm YourNewName.bit YourNewName.asm". Note that the extensions ". bit" and ". Asm" are necessary. Enter this command line for as many bitstreams as you need.
  - b. Replace "**asm6x bitfilename.asm**" by "asm6x YourNewName.asm". (The asm6x executable is included in CCStudio). Enter this command line for as many bitstreams as you need.
5. Save the Makefile and run it. The executable is called and generates the ". obj" file(s).
6. Once the .obj file is generated, it can be linked with the Dsp application. (xxx.out for CCStudio or xxx.app for 3L) for a future download to the DSP.
7. The bit file can now be formatted and written over a ComPort (by the DSP) using the function FPGAFullConfiguration () as described in step **6**

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