HARDWARE SPECIFICATION

FOR

EMBEDDED PROCESSOR SYSTEMS.

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APPROVAL PAGE

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1. SCOPE

FPGAs with integrated processors make a very attractive solution for developers who want to benefit from both software and hardware worlds.

This document specifies the requirements for a base system set up in a view to develop applications comprising embedded processor cores in a Xilinx FPGA.

1.1. INTRODUCTION

The base system set up must provide the means to configure and debug code running on an embedded processor.

The requirements of a base set up using embedded processors in FPGAs must provide the global information needed by developers who intend to set up their own Sundance platform and choose from the wide range of Sundance products.

The PowerPC PPC405™ in a Virtex-II PRO is the primary target but softcore processors and other Xilinx FPGAs could also be targeted the same way.

1.2. PURPOSE

The purpose is to ensure that the key elements of a base system set up are well defined to ease the task of developers.

1.3. APPLICABILITY

FPGA modules are an ideally simple target for this development.

2. APPLICABLE DOCUMENTS AND REFERENCES

2.1. APPLICABLE DOCUMENTS

2.1.1. External Documents

Xilinx E.D.K. documentation.

2.1.2. Internal documents

Hardware overview documentation from SUNDANCE help file.

2.2. REFERENCES

2.2.1. External documents

N.A

2.2.2. Internal documents

N.A

2.2.3. Project documents

N.A

2.3. PRECEDENCE

In the event of conflict between the text of this document, and the applicable documents cited herein, the text of this document takes precedence. Nothing in this document however, supersedes applicable laws and regulations unless a specific exemption has been obtained and is identified in the text of this document.

3. ACRONYMS, ABBREVIATIONS AND DEFINITIONS

3.1. ACRONYMS AND ABBREVIATIONS

TIM	Texas Instruments Module
PPC	Power PC
JTAG	Joint Test Action Group. This standards defines a 5-pin serial protocol for accessing and controlling the signal-levels on the pins of a digital circuit, and has some extensions for testing the internal circuitry on the chip itself
E.D.K	Xilinx Embedded development Kit

3.2. DEFINITIONS

DSP module	It is a TIM module hosting a C6x DSP coupled to an FPGA.
FPGA-only modules	It is a TIM module with no C6x DSP available, where the FPGA is the centre part of the TIM and provides its functionality.
Comport	A Sundance communication port, or "comport", can connect two TIMs together to provide a bi-directional path for exchanging streams of 32-bit values.

4. REQUIREMENTS

We want to:

- execute code on the embedded processor.
- Start the debugger and look at instructions, memory and registers at any point in time while the design is active.
- We also want to specify the system level requirements at reset and runtime, for debugging and while the application is running.

4.1. PRINCIPLE

To illustrate the principle we suppose that we generated:

- a basic PowerPC hardware design (bitstream)
- Some PowerPC application executable.

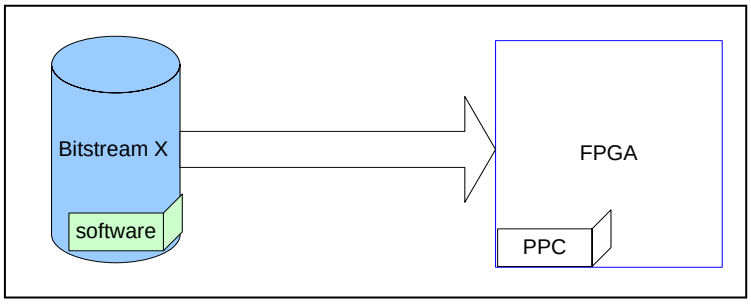

Figure 1: Configuring the PowerPC with an application

At power up, the FPGA is blank and the PowerPC is not connected to the FPGA fabric.

The entire software application fits in the space reserved for it in the Bitstream. The bitstream embedding the software application is designated as bitstream X.

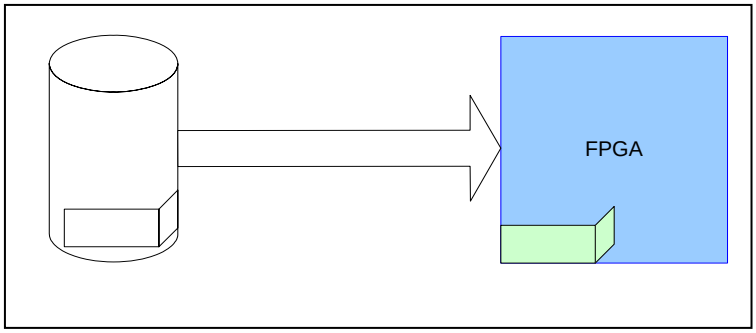

Figure 2: code executing

Once the FPGA has been configured with bitstream X, the processor is brought out of reset and starts executing the software.

4.2. SYSTEM SET UP

A typical system set requires the assembling of a TIM module fitted on a carrier.

The different categories of TIMs are processor TIMs or FPGA TIMs.

The different categories of carriers are stand-alone carriers and carriers that can plug in a host.

Depending on the combination, you need to make sure that:

The TIM module (processor or FPGA module) must provide JTAG access to the FPGA.

The carrier module needs to be able to provide a reset pulse to the TIM module.

4.3. OPERATIONAL MODES

4.3.1. Configuring the FPGA.

4.3.1.1. FPGA modules

FPGA modules are populated by a switch selecting the configuration device.

It can be:

- JTAG
- Comport
- PROM/FLASH

The FPGA module seats on a TIM site of a carrier and can be configured:

- Via JTAG:
  - The FPGA module needs to have a JTAG connection.
  - The switch must be set up to select JTAG as the configuration device.
- Via Comport:
  - The switch must be set up to select the appropriate comport as the configuration device. The choice varies according to the module, but there is always comport 3 as a default.
  - This communication link to a host or a DSP TIM is used to download the bitstream.
  - The FPGA module seats on the first TIM site of a host carrier: in this case comport 3 provides a communication path and a host application sends the bitstream via that link to the module. Sundance provides software support.

- The FPGA module seats on a TIM site other than the root and is interconnected to a processor module via a comport: The processor module manages the loading of the bitstream. Sundance provides software support.

- Via PROM:
  - The bitstream needs be downloaded in the PROM.
  - The FPGA will configure at power up or after a reset pulse is received.
  - This option is only really interesting once the application is fully developed.

  - The carrier will provide a reset pulse at start up, nevertheless the reset on FPGA modules is controlled via a CPLD which will hold the FPGA reset active until an ENKEY is received on the configuration comport. The only way to allow JTAG configuration of the FPGA is then to deselect comport configuration via a switch on the board (see the User guide for that module) and select Flash/PROM configuration.
  - The reset connected to the FPGA must not remain active after power up which would prevent the FPGA design to start up.

4.3.1.2. Processor modules

Processor modules are equipped with a DSP, Flash memory and an FPGA.

The processor module seats on a TIM site of a carrier and its FPGA can be configured:

- Via JTAG: The FPGA of the module needs to have a JTAG connection.
- Via Flash: The bitstream needs be downloaded in the Flash (Using the SMT6001).
  - The FPGA will configure at power up or after a reset pulse is received.
  - This option is only really interesting once the application is fully developed.

4.3.2. Debugging

The debugging of the embedded processor design is done via JTAG.

4.4. DOCUMENTATION

The following documents shall be produced and reviewed as part of the design process:

- Hardware specification document for embedded processor systems.
- Hardware implementation document for embedded processors systems.

NOTES

None.