
# HARDWARE DESIGN
# TO IMPLEMENT
# A ZBT CONTROLLER WITH EDK

# APPROVAL PAGE

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# TABLE OF CONTENTS

# 1. SCOPE

This document explains how you can use the Xilinx's external memory controller (PLB EMC or OPB EMC) on Sundance's boards. Several reference designs allow you to implement these controllers on the OPB bus, on the PLB bus and with a PowerPC or a Microblaze processor.

## 1.1. INTRODUCTION

This design is implemented by Sundance on Xilinx's FPGA, V2, V2P, V4-FX60 targets custom features of these chips to reach maximum performances.

The core is validated on SMT339 modules with the Samsung K7N321801M device and GS8320Z18GT device.

Implementing the PowerPC design in a Sundance Module you will allow to run application specific systems which contain both hardware and software. Moreover, over 8Mbytes of high speed ZBT RAM can be connected to the PowerPC or the Microblaze processors with this design, allowing high speed storage.

## 1.2. PURPOSE

The purpose of this development is to implement an external memory controller to provide an interface between the PowerPC or the Microblaze processors and the ZBT memory. For that, we use an IP core provided by Xilinx.

## 1.3. APPLICABILITY

All the Sundance modules with a FPGA (V4, V2, V2P) and a ZBT memory are able to benefit from the implementation of that design.

# 2. APPLICABLE DOCUMENTS AND REFERENCES

## 2.1. APPLICABLE DOCUMENTS

### 2.1.1. External documents

None

### 2.1.2. Internal documents

None

### 2.1.3. Project documents

N.A

## 2.2. REFERENCES

### 2.2.1. External documents

N.A

### 2.2.2. Internal documents

N.A

### 2.2.3. Project documents

N.A

## 2.3. PRECEDENCE

In the event of conflict between the text of this document, and the applicable documents cited herein, the text of this document takes precedence. Nothing in this document however, supersedes applicable laws and regulations unless a specific exemption has been obtained and is identified in the text of this document.

# 3. ACRONYMS, ABBREVIATIONS AND DEFINITIONS

## 3.1. ACRONYMS AND ABBREVIATIONS

| | |
|---|---|
| TIM | Texas Instruments Module |
| ZBT RAM | Zero-bus turnaround Random access memory (RtRAM = No turnround Random Access Memory) |
| | |
| | |

## 3.2. DEFINITIONS

# 4. TOP LEVEL DESIGN

## 4.1. SUBSYSTEM BREAKDOWN

This tutorial demonstrates process to configure and to test a PowerPC design system with a ZBT external memory controller using the Embedded Development Kit.

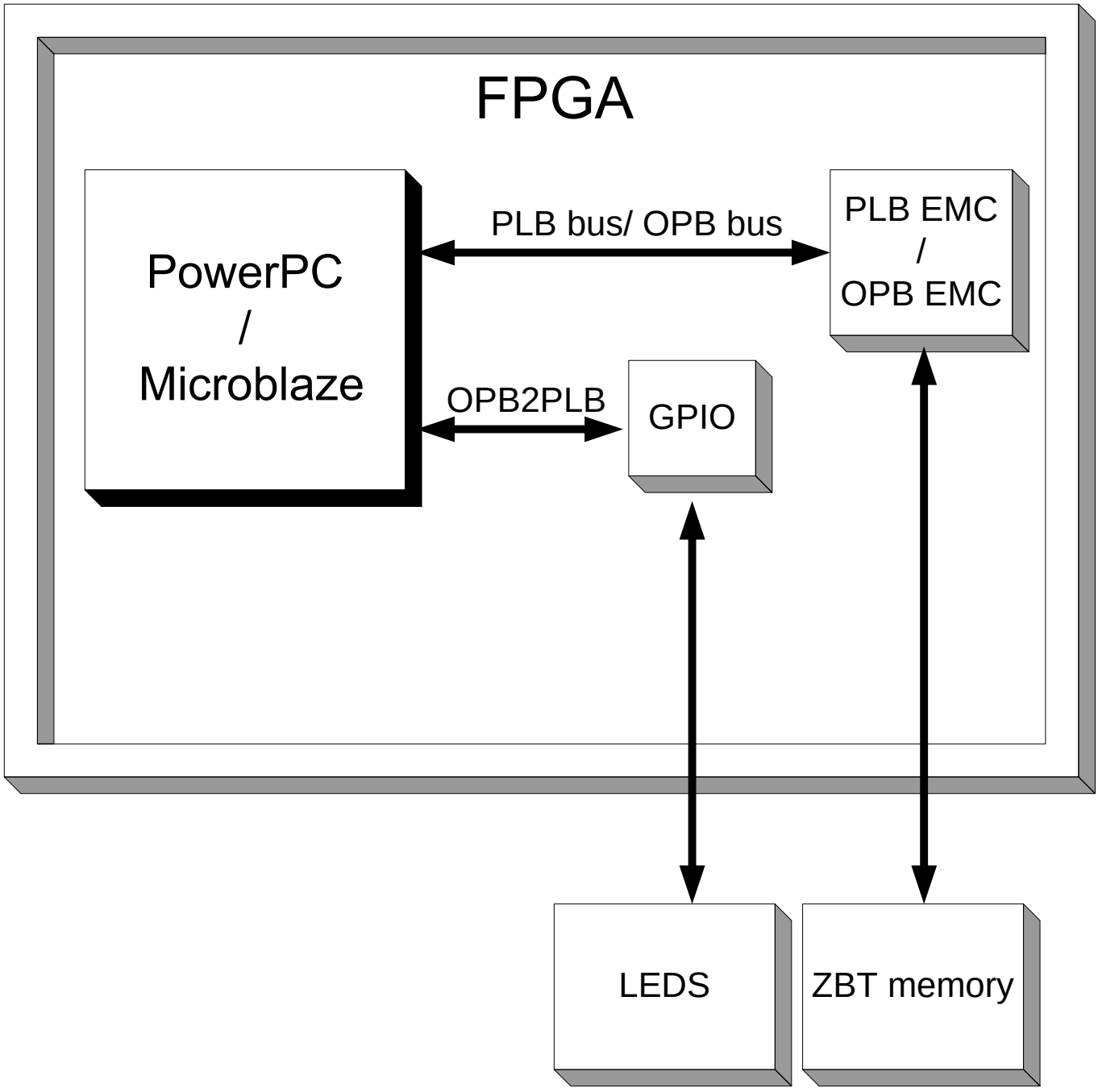



Figure 1 Top level block diagram

Both PowerPC and Microblaze processors can be used to implement the external memory controller. Thus, you can always implement this design independently of the target used.

## 4.2. SYSTEM STATES AND MODES

This application demonstrates data transfers between an embedded processor like the PowerPC and a ZBT memory. Moreover, a GPIO block is used to flash the LEDs on the board.

Sundance gives you an application to configure the Xilinx's EMC for the Sundance's boards. Thus, you can run your application in using the external memory controller.

This design includes following hardware components:

- PowerPC or Microblaze
- PLB Bus (Processor Local Bus)
  - Plb_bram_if_cntrl
  - Bram_block
  - PLB_EMC or OPB_EMC
  - PLB2OPB_bridge
- OPB Bus (On-chip Peripheral Bus)
  - OPBGPIO

All peripherals are described in the System Assembly view.

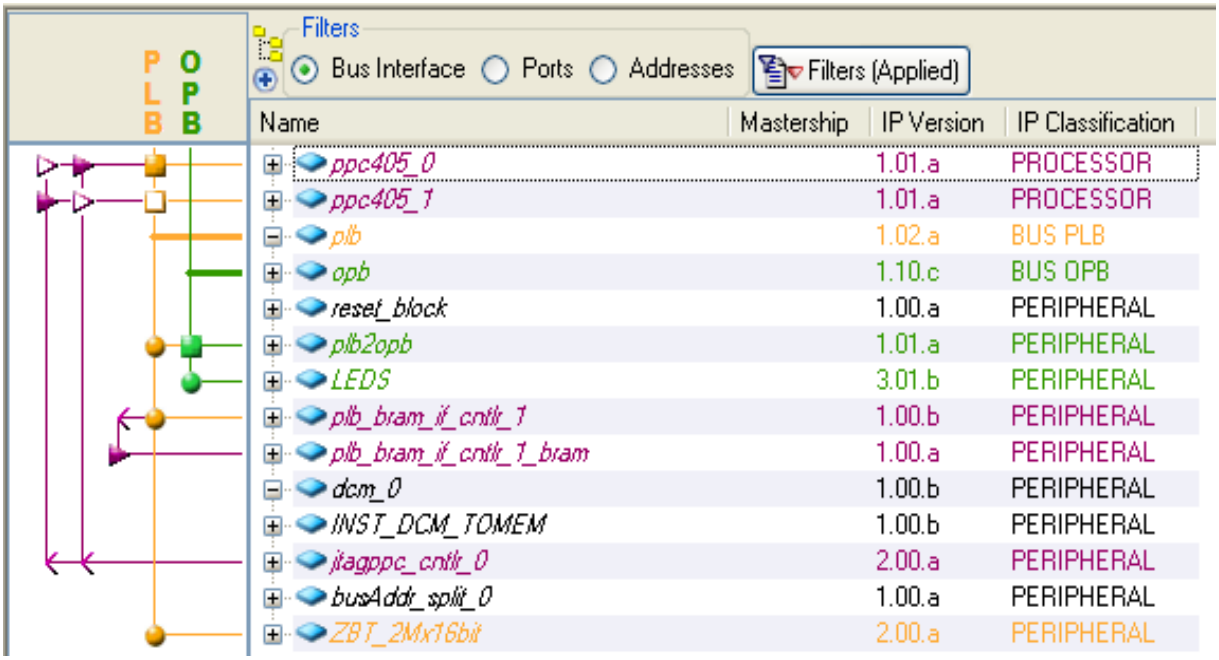



Figure 2 System Assembly view

The following is an explanation of the setting specified in this design:

- System Wide Setting
    - Reference clock frequency: this is the on board frequency of the clock (it is named “sys_clk_pin”)
    - Processor clock frequency: This is the frequency of the clock driving the processor system. (it named “proc_clk_s” for the PowerPC (**300MHz**) design and sys_clk_s for the microblaze design (**100MHz**)).
    - Bus clock frequency: this is the frequency of the clock driving the PLB, OPB and OCM buses.
- Processor Configuration
    - Reset active low
    - The PowerPC JTAG pins are included in the FPGA JTAG chain.
- IO devices configuration
    - OPB GPIO Leds: widht 3bits
    - External memory controller:
        - Number of memory banks: 1
        - Width of memory Bank 0 data bus : 16bits
        - Memory type is synchronous
        - Include data width matching
        - Data and control signals are input/output on the falling edge of the clock
        - Pipelined delay of 2 clocks

For more details about EMC configurations, open the “configure IP …” windows: **right click on ZBT_2Mx16bit → configure IP**

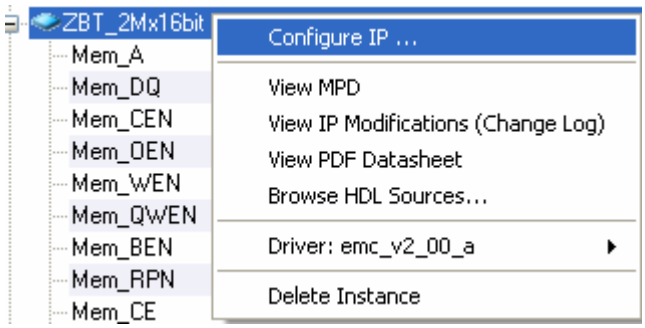



Figure 3 IP configuration

## 4.3. CLOCK MANAGEMENT

This reference design uses one dedicated input clock (the on-board oscillator). This input clock feeds two of the enhanced DCM in the Virtex 4.

The first DCM (DCM_0) boots the inputs clock and adjusts the phase of the clock of the PowerPC or Microblaze. This DCM provides the processor clock frequency and bus clock frequency for the PowerPC design.

To synchronise the synchronous memory clock to the internal clock FPGA, this design includes another DCM (INST_DCM_TOMEM). This one uses the synchronous memory clock input as the feedback clock as shown in Figure 4.

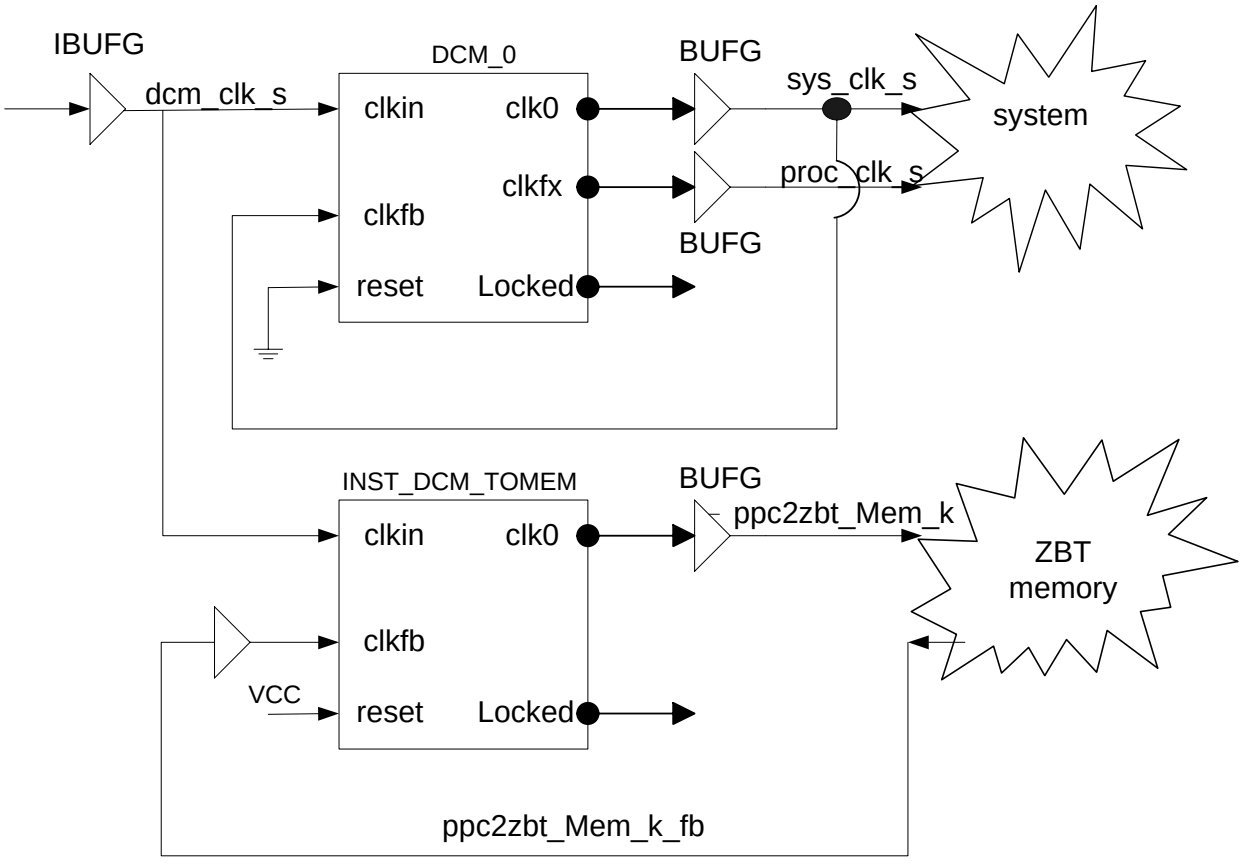



Figure 4 Clock management

This circuit is used to deskew a system clock between a Virtex chip and other non-Virtex chips on the same board.

The following table shows the clock domains for this design.

| | **PowerPC** | **Microblaze** |
|---|---|---|
| **Reference clock frequency** | 100MHz | 100MHz |
| **Processor Clock Frequency** | 300MHz | 100MHz |
| **Bus clock frequency** | 100MHz | 100MHz |

Table 1 Clock domains

# 5. DETAILED DESIGN

## 5.1. MODULE 1

This chapter explains how you can implement and use the external memory controller with a PowerPC or Microblaze processors.

### 5.1.1. Module's interface

The following table describes the pinout of this design.

| External ports | Direction | Comment |
|---|---|---|
| fpga_0_LEDS_GPIO_d_out_pin (0to2) | O | OPB GPIO to flash the LEDs on the board |
| sys_clk_pin | I | Reference clock frequency |
| sys_rst_pin | I | Active Low |
| ppc2zbt_Mem_DQ_pin (0to 15) | IO | Data Input and Output pin |
| ppc2zbt_Mem_Mem_A_pin (0 to 20) | O | Address output |
| ppc2zbt_Mem_CEN_pin (0 to 0) | O | Chip select (/CS1) |
| ppc2zbt_Mem_OEN_pin (0 to 0) | O | Output enable |
| ppc2zbt_Mem_BEN_pin (0 to 1) | O | Byte write inputs |
| ppc2zbt_Mem_CE_pin | O | Chip select (CS2) |
| ppc2zbt_Mem_ADV_LDN_pin | O | Address advance |
| ppc2zbt_Mem_LBON_pin | O | Burst mode control |
| ppc2zbt_Mem_CKEN_pin | O | Clock enable |
| ppc2zbt_Mem_WEN_pin | O | Read/Write control input |
| ppc2zbt_Mem_mem_Zz_pin | O | Power sleep mode |
| ppc2zbt_Mem_CE2_pin | O | Chip select (/CS2) |
| ppc2zbt_Mem_k_pin | O | clock |
| ppc2zbt_Mem_k_fb_pin | I | Clock feedback from the FPGA |

Table 2 Pinout

### 5.1.2. Functions

In this design, only one bank memory has been implemented but all of them are been tested. You can implement the ZBT memory banks in several kinds. Figure 5 illustrates several architectures to interface the banks of memory components.

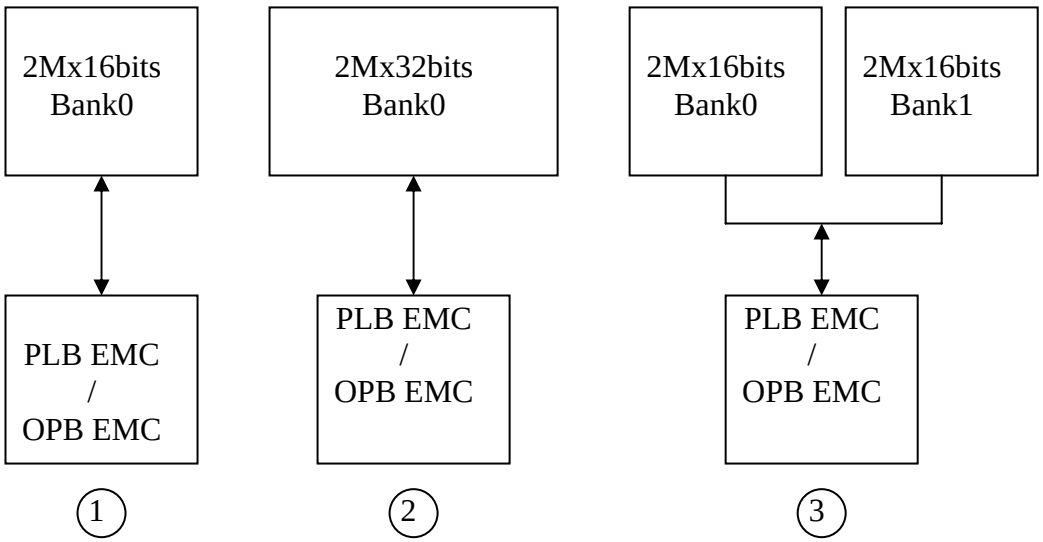



Figure 5 External memories architectures

The first case is implemented in this design. You can select one of them to increase the width of the memory.

### 5.1.3. Timing specification

The timing characteristics of this design are defined in the user constraint file. In this file, you could find all pinout for all ZBT memory banks.

### 5.1.4. Implementation

The PowerPC and Microblaze processors were designed about Big Indian architecture. From point of view of the memory, all signals are organised as little Indian. The following table explains the conversion between big Indian and little Indian.

| EMC signals (MSB LSB) | Memory device signal (MSB LSB) |
|---|---|
| ppc2zbt_Mem_DQ_pin (0 : 15) | DQ(15 : 0) |
| ppc2zbt_Mem_Mem_A_pin (0 : 20) | A(20:0) |
| ppc2zbt_Mem_BEN_pin (0 to 1) | BW(1:0) |
| ppc2zbt_Mem_CEN_pin (0 to 0) | /CS1 |
| ppc2zbt_Mem_OEN_pin (0 to 0) | /OE |
| ppc2zbt_Mem_CE_pin | CS2 |
| ppc2zbt_Mem_ADV_LDN_pin | ADV |
| ppc2zbt_Mem_LBON_pin | /LBO |
| ppc2zbt_Mem_WEN_pin | /WE |
| ppc2zbt_Mem_mem_Zz_pin | ZZ |
| ppc2zbt_Mem_CE2_pin | /CS2 |
| ppc2zbt_Mem_CKEN_pin | /CKE |

Figure 6 Connection between EMC and ZBT memory

In this design an utility bus split core has been implemented to split the "ppc2zbt_Mem_Mem_A_split(31:0)" bus into smaller bus: ppc2zbt_Mem_Mem_A(20:0). The following figure shows the memory map for this design.

| Instance | Name | Address | Base Address | High Address | Size | Lock | ICache | DCache | Bus Connection |
|---|---|---|---|---|---|---|---|---|---|
| opb | | | | | U | | | | |
| ppc405_0 | MDCR | IDCR | | | U | | | | No Connection |
| ppc405_1 | MDCR | IDCR | | | U | | | | No Connection |
| plb | SDCR | | | | U | | | | No Connection |
| plb2opb | SDCR | DCR | | | U | | | | No Connection |
| LEDS | SOPB | | 0x10000000 | 0x100003FF | 1K | | | | opb |
| plb_bram_if_cntlr_1 | SPLB | c_baseaddr:c_highaddr | 0xffffc000 | 0xffffffff | 16K | | | | plb |
| ZBT_2Mx16bit | SPLB | MEM0 | 0x00000000 | 0x001FFFFF | 2M | | | | plb |
| plb2opb | SPLB | RNG0 | 0x10000000 | 0x100003FF | 1K | | | | plb |
| plb2opb | SPLB | RNG1 | | | U | | | | plb |
| plb2opb | SPLB | RNG2 | | | U | | | | plb |
| plb2opb | SPLB | RNG3 | | | U | | | | plb |

Figure 7 Memory map

Caution: this controller does not support sleep mode, burst mode (/LBO), parity checking and parity generating.

### 5.1.5. Validation

You can download the bitstream to the FPGA. For that, you can use the SMT6001 package whether your board has the DSP module else you can use the 6500 package. You can also use the Parallel Cable IV from Xilinx.

Two files are generated by EDK: ZBT.bit and download.bit. The download.bit file contains both hardware and software. For more information, refer to the EDK documentations.The software application in specified in Application tab.

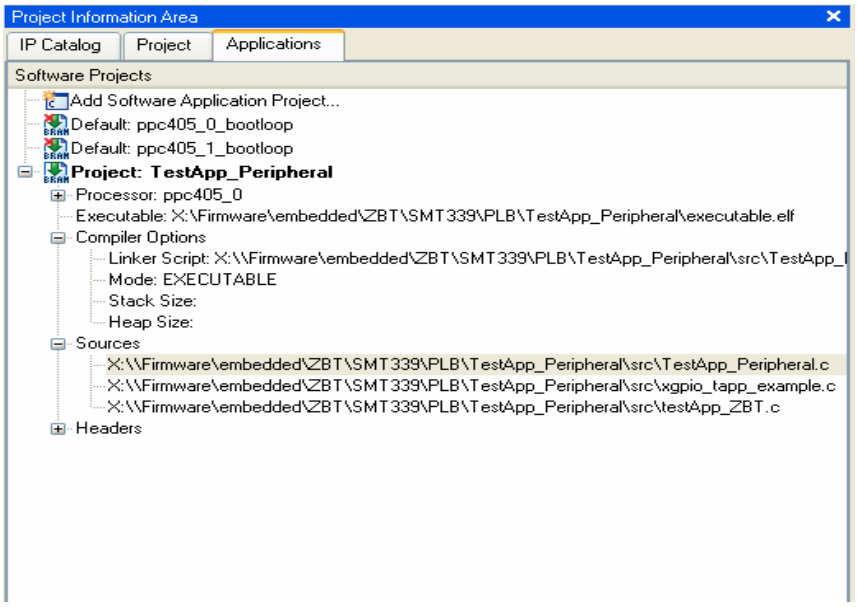



Figure 8 Software application

The TestApp_pheripheral.c file uses Xilinx's libraries to test the memory and the GPIO peripherals. The source code for the memory test utility function is contained in the following file:"microblaze_0\libsrc\common_v1_00_a\src\ xutil_memtest.c". For more information about these functions, refer to EDK documentations.

To test this design, you can use XMD/GDB debugger with the parallel cable IV from Xilinx.


Figure 9 debugger icons

The following figure shows XMD debugger configuration.

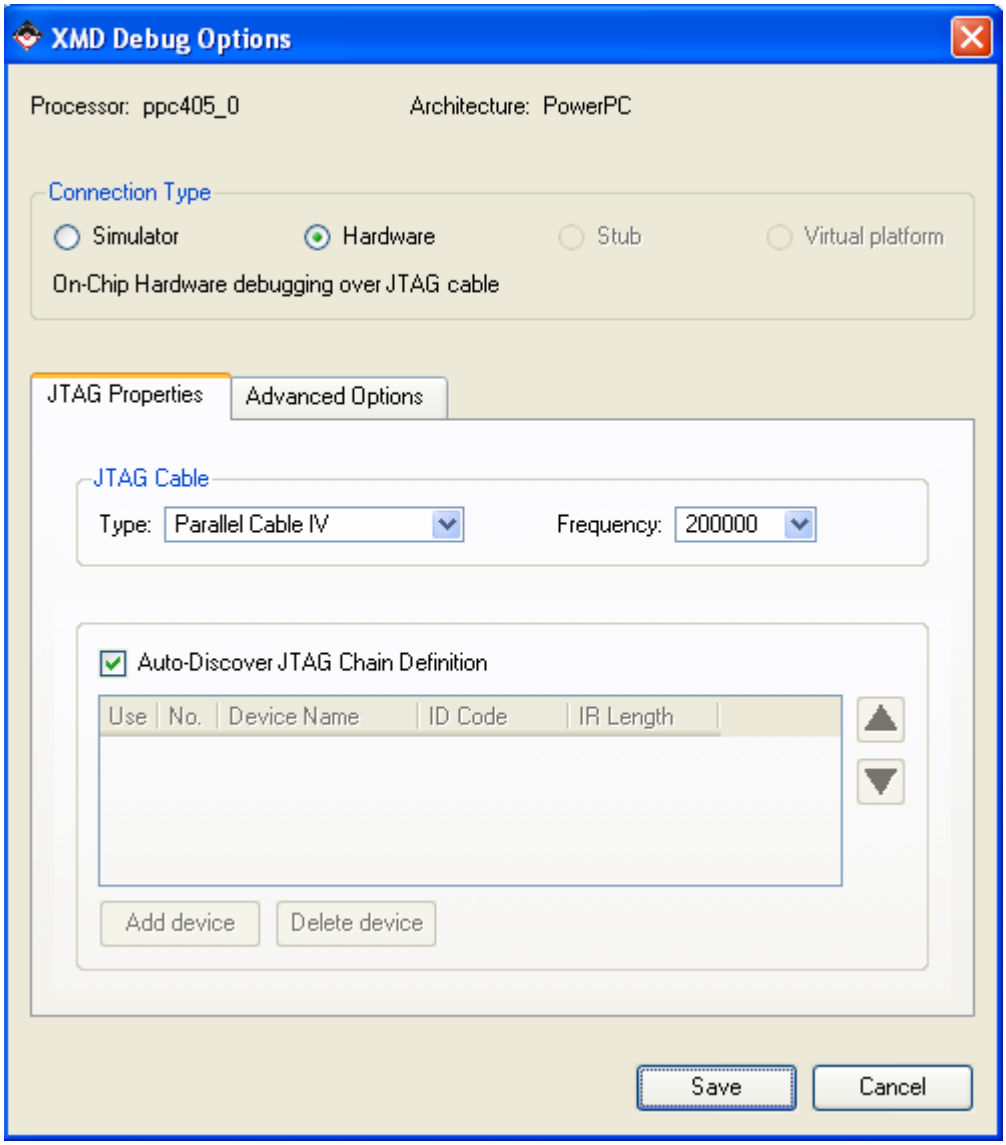



Figure 10 XMD Debug option

You have to download the bistream to the FPGA before to run the XMD debugger. For that, you should download the ZBT.bit file.

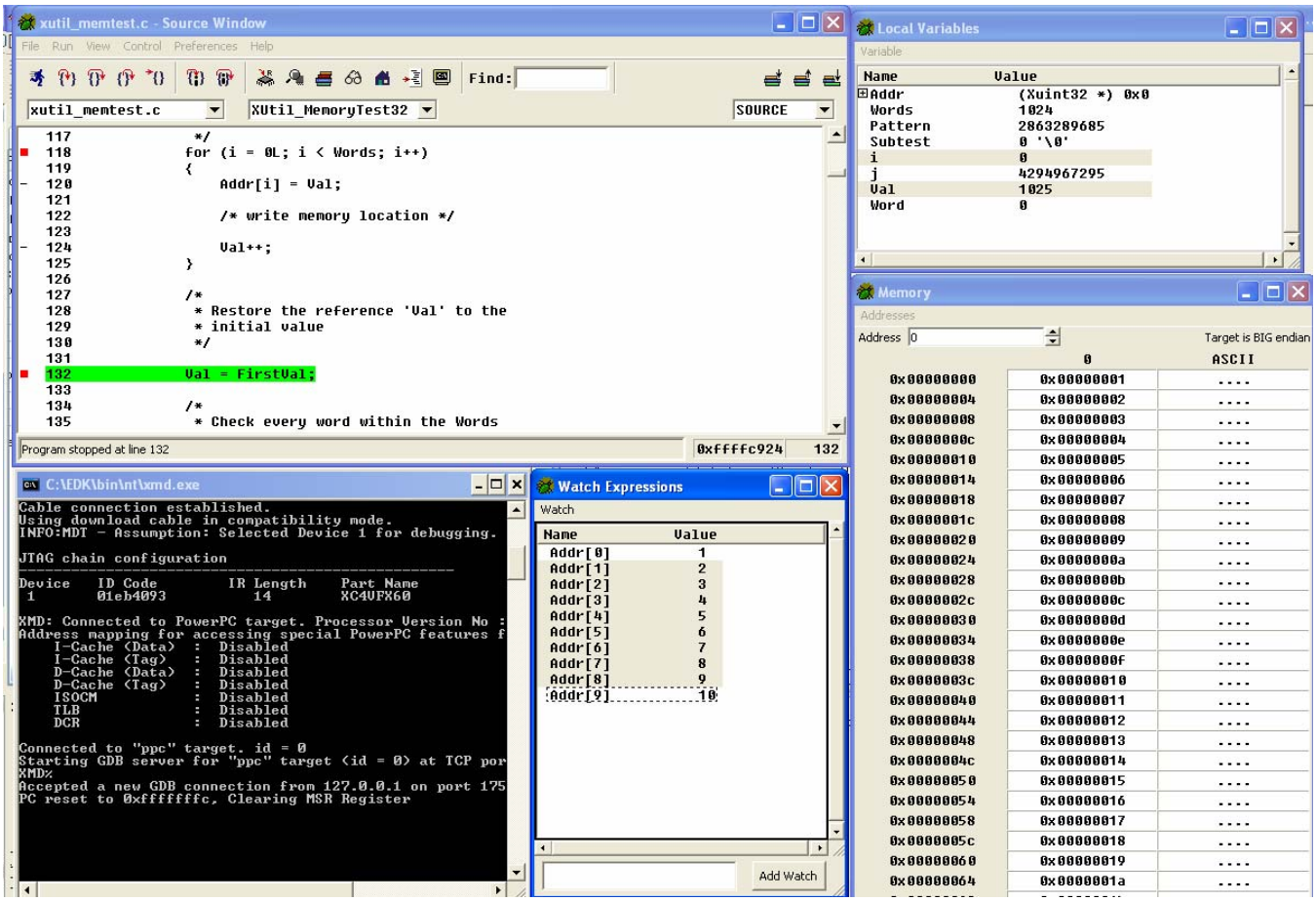
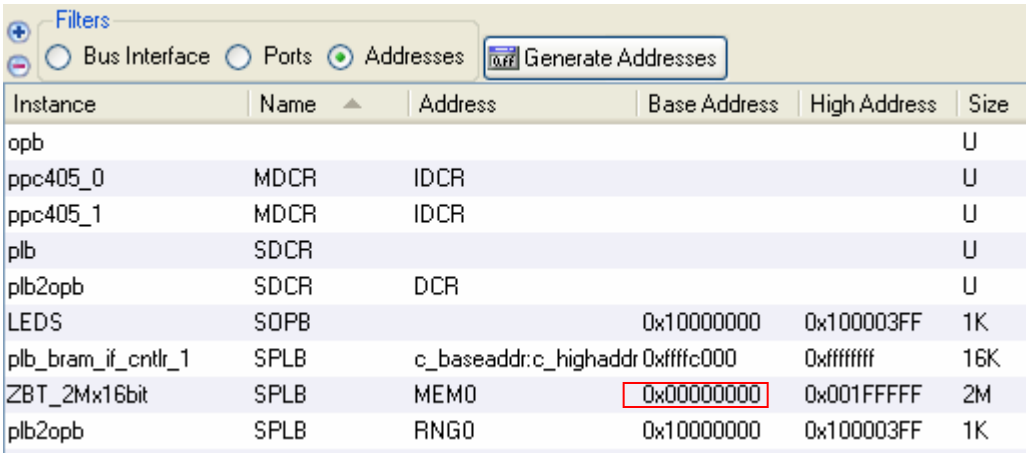



Figure 11 XMD debugger

To read the data from the ZBT in the Memory widows, you can initialise the address with the base address of the ZBT_2Mx16bit controller. This value can be read in the addresses filter.




| Instance | Name | Address | Base Address | High Address | Size |
|---|---|---|---|---|---|
| opb | | | | | U |
| ppc405_0 | MDCR | IDCR | | | U |
| ppc405_1 | MDCR | IDCR | | | U |
| plb | SDCR | | | | U |
| plb2opb | SDCR | DCR | | | U |
| LEDS | SOPB | | 0x10000000 | 0x100003FF | 1K |
| plb_bram_if_cntlr_1 | SPLB | c_baseaddr:c_highaddr | 0xffffc000 | 0xffffffff | 16K |
| ZBT_2Mx16bit | SPLB | MEM0 | 0x00000000 | 0x001FFFFF | 2M |
| plb2opb | SPLB | RNG0 | 0x10000000 | 0x100003FF | 1K |

Figure 12 EMC base addresses

If the application run correctly, three Leds have to flash.

# 6. DESIGN INTALLATION

## 6.1. DIRECTORY STRUCTURE

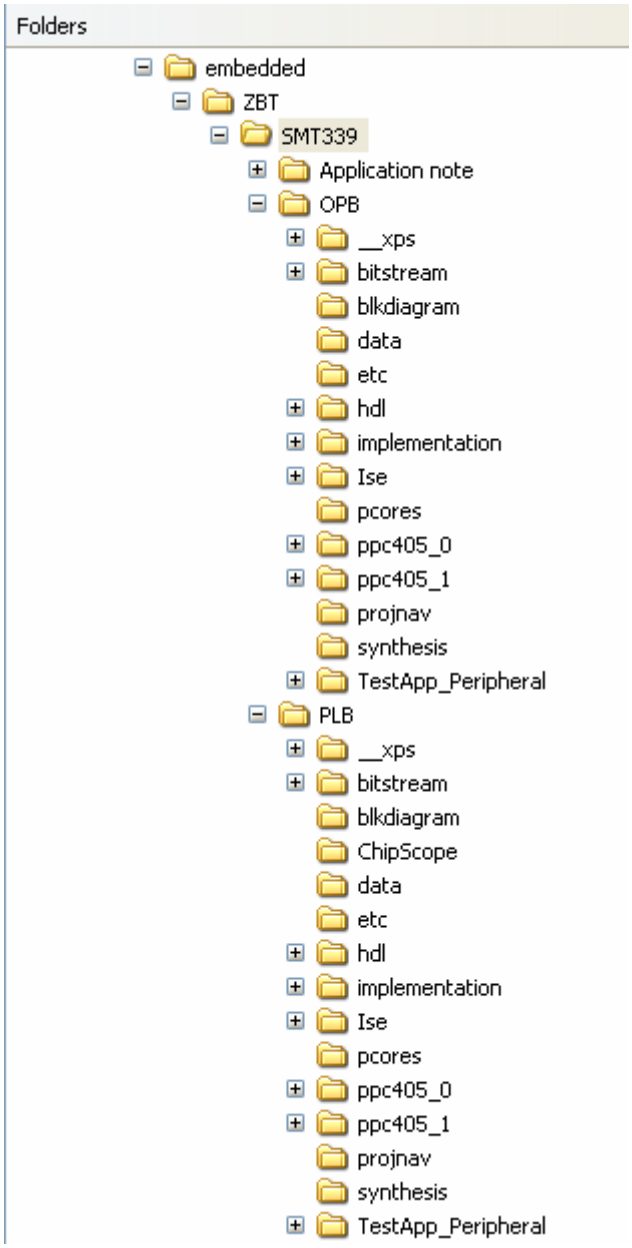



Figure 13 Project directory

- OPB folder: contains the design for OPB EMC
    - Bitstream: bitstream for this design
    - Data: contains the UCF file.
    - Etc: contains the settings for the JTAG
    - Implementation: contains the bitstream generated by XPS.
    - Ppc405_0: software programs for PPC0
    - Ppc405_1: software programs for PPC1
    - Synthesis :contains all synthesis files
    - TestApp_pheripheral: user application in C
- PLB folder: contains the design for PLB EMC
    - Bitstream: bitstream for this design
    - Data: contains the UCF file.
    - Etc: contains the settings for the JTAG
    - Implementation: contains the bitstream generated by XPS.
    - Ppc405_0: software programs for PPC0
    - Ppc405_1: software programs for PPC1
    - Synthesis :contains all synthesis files
    - TestApp_pheripheral: user application in C

## 6.2. SOFTWARES VERSION


Figure 14 Softwares version