Unit / Module Description:	Capture Demo For Intech
Unit / Module Number:	EVP6472-SMT391
Document Issue Number	1.1
Issue Data:	19th July 2012
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EVP6472 Intech Demo

Abstract

ADC demonstration application based on EVP6472 and SMT391

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1. Features and Requirements

To run the application:

1. Signal generator
2. Sundance hardware:

   SMT372T, SMT111 and SMT391
3. Sundance Software:

   SMT6002 (flash programing) and SMT111 driver
4. Cables:

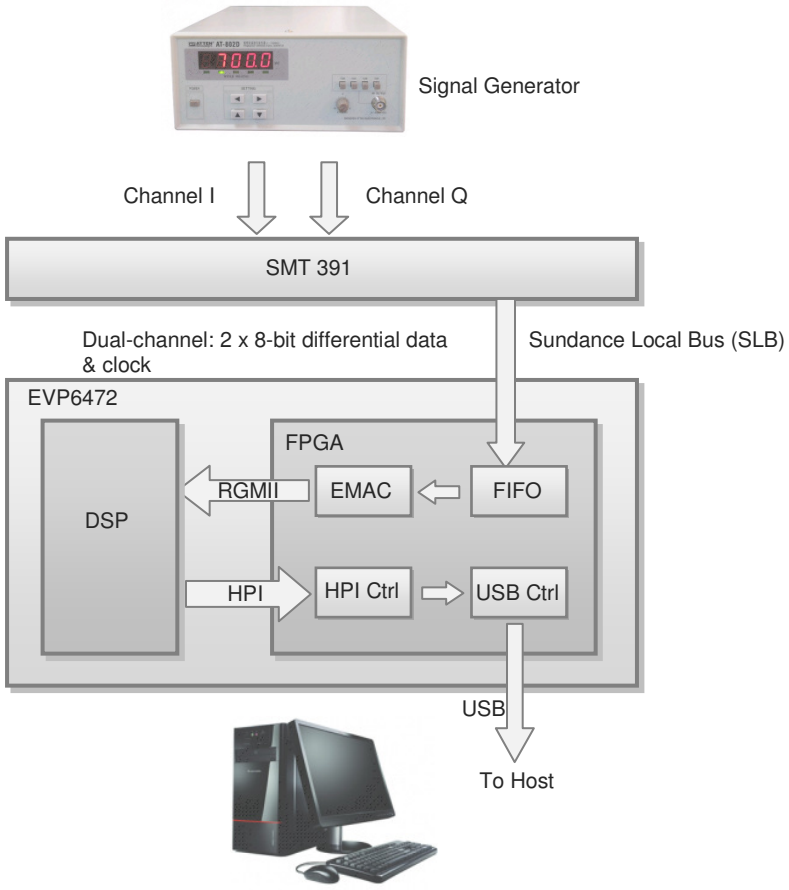
   Signal generator wires, USB cable, SMT111 power cable and Xilinx JTAG cable

To develop the application

1. Xilinx software tools: Xilinx EDK, SDK (12.3)
2. Taxes Instrument software tools: Code Composer Studio (CCS) (4.24)
3. Visual Studio 2008 (Compiled in WindowsXP OS)

   *Source code is generated with the version in the bracket

2. Data Path



1. Two channels of analog signal (between -0.3V to +0.3V) are sent to the SMT391 daughter board
2. The SMT391 using its internal clock (128MHz in default) to convert the analog inputs into 2 × 8-bit parallel differential data and sends it to the FPGA via the Sundance Local Bus (SLB)
3. The FPGA starts sampling two input channels and then buffer them in two FIFOs. Once the received data size meets the Ethernet package size, the data in each FIFO is transmitted to each DSP via the RGMII link.
4. The DSPs receive the data and stores it in their 256M DDR RAMs.
5. Once the required data amount is sampled (96, 000 bytes), the FPGA starts fetching data stored in the DDR RAMs through Host-Port Interface (HPI), and sends them to the host PC through the USB cable.

3. How the system works

After device configured:

1. After boot, the FPGA is automatically configured by the bitstream in the flash memory. The FPGA is configured as an embedded processor (MicroBlaze), and its peripherals used for accessing various interfaces.
2. MicroBlaze reads the DSP code from Flash memory.
3. MicroBlaze writes the DSP code to the DSP program memory through the HPI interface.
4. MicroBlaze sets up the DSP configuration through HPI interface.
5. MicroBlaze resets and starts the DSP.
6. MicroBlaze configures its ADC capturer peripheral e.g. EMAC package size and package numbers.
7. MicroBlaze starts the ADC capturer.
8. After one package size of data is sampled, the ADC capturer starts one EMAC transmission.
9. After the all required packages are transmitted (96, 000 bytes), DSPs can start processing the data.
10. MicroBlaze starts fetching the data stored in the DDR RAMs through the HPI and transmit to the host PC via USB.
11. The Host PC saves the incoming data (in binary), which can be viewed any plot software, e.g. MatLab.

4. How to run the demonstration

Every time the EVP6472 boots up, it is self configured by loading the application code (bitstream for the FPGA and binary code for the DSP) from the flash memory. Therefore we need to program the flash for the very first time.

After flash programmed, the EVP6472 automatically starts working every time it boots up.

4.1 First time flash programming/recovery

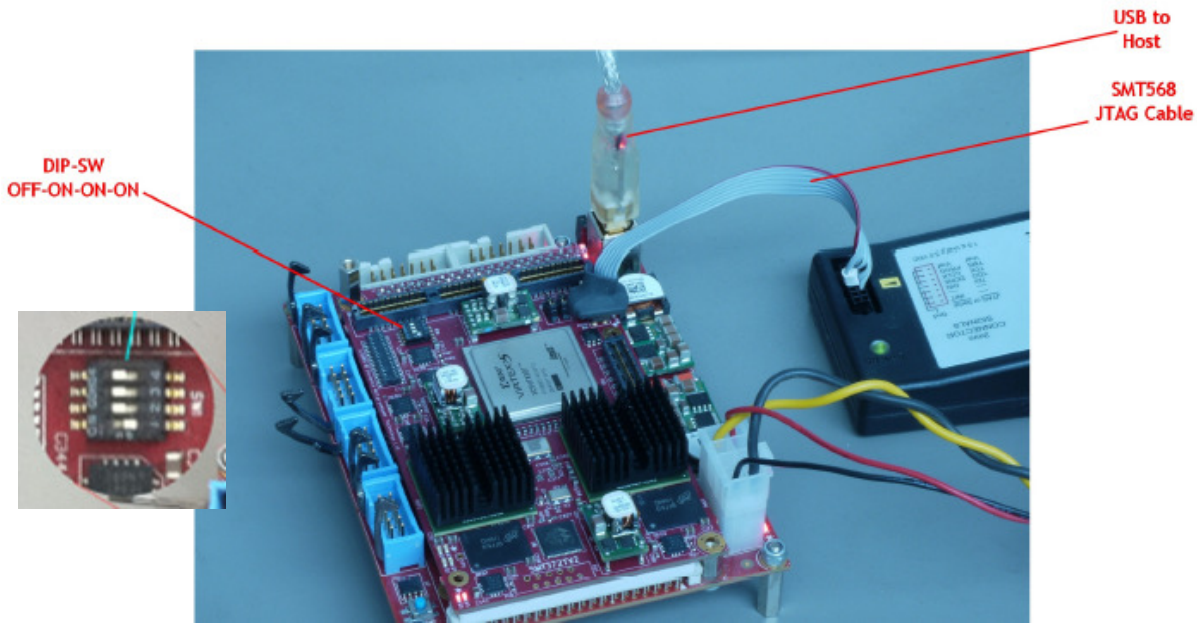
To program the flash, we use JTAG to load the bitstream to the FPGA, which communicates with the host through the USB.

The bitstream used for programming flash is the same one used for our normal application. It performs one of the actions depending on the first bit of the DIP switch (1 for programming flash and 0 for normal application). To programme the flash, steps are followed.

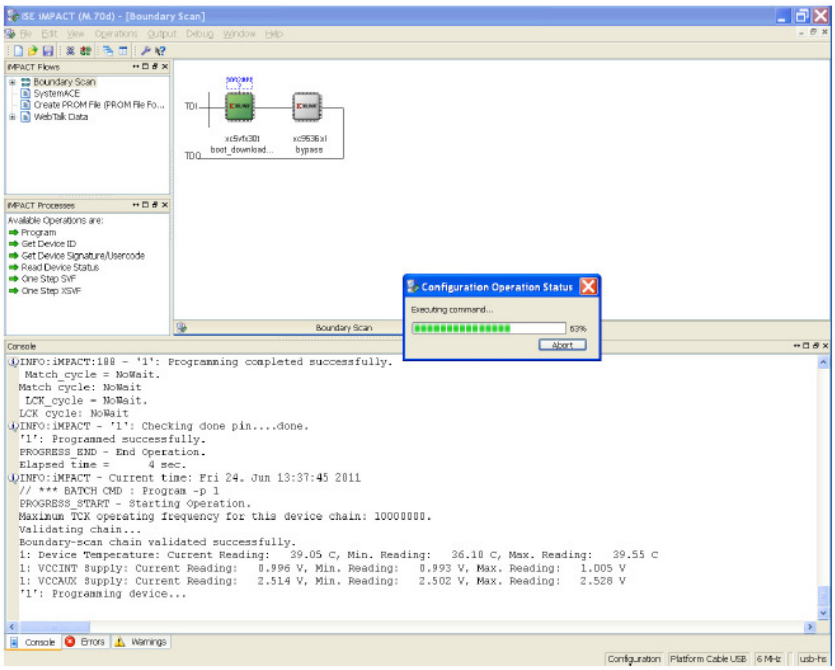
Ensure that the DIP-SW is set as shown above (position 1 OFF, the others ON).

Connect the USB cable from the SMT111 to the Host PC.

Connect the Xilinx programming pod to the SMT372T using an SMT568 JTAG cable.

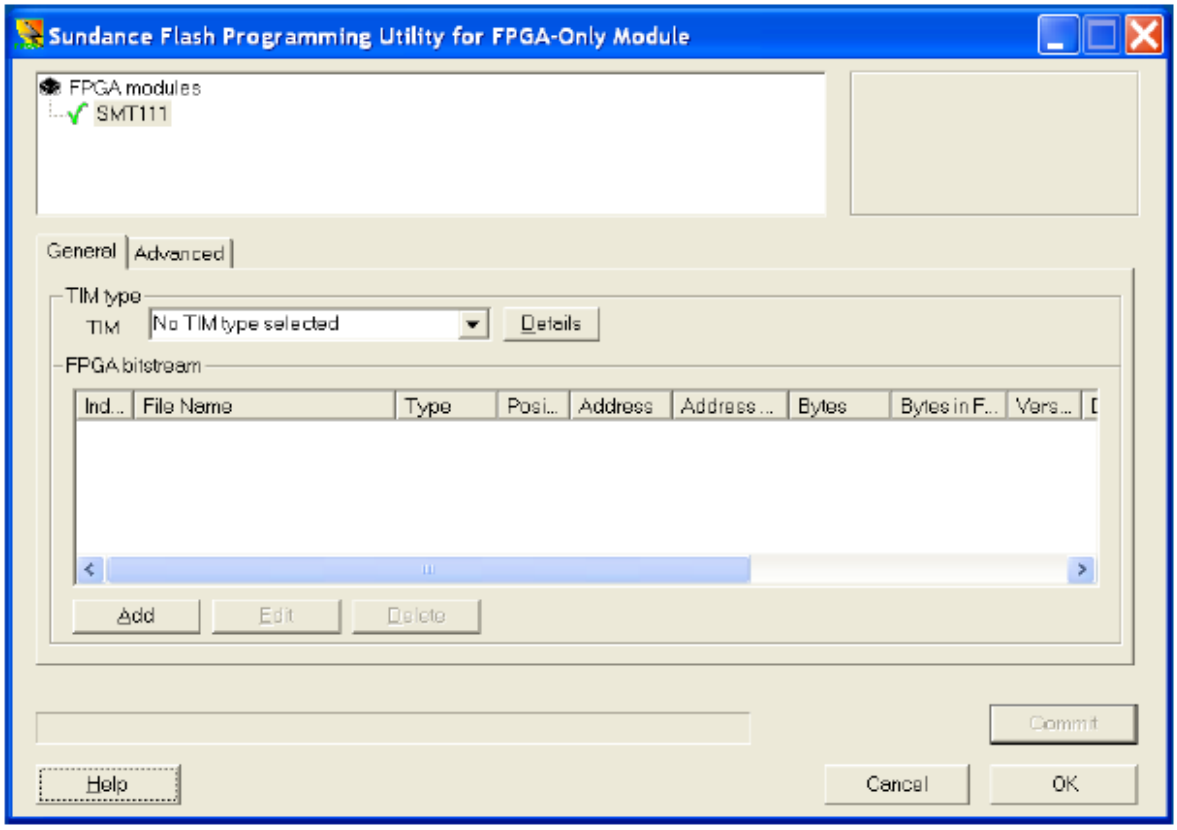


Run Xilinx impact programming tool and select boot_download.bit as the configuration file for the XC5VFX30T of the SMT372T.

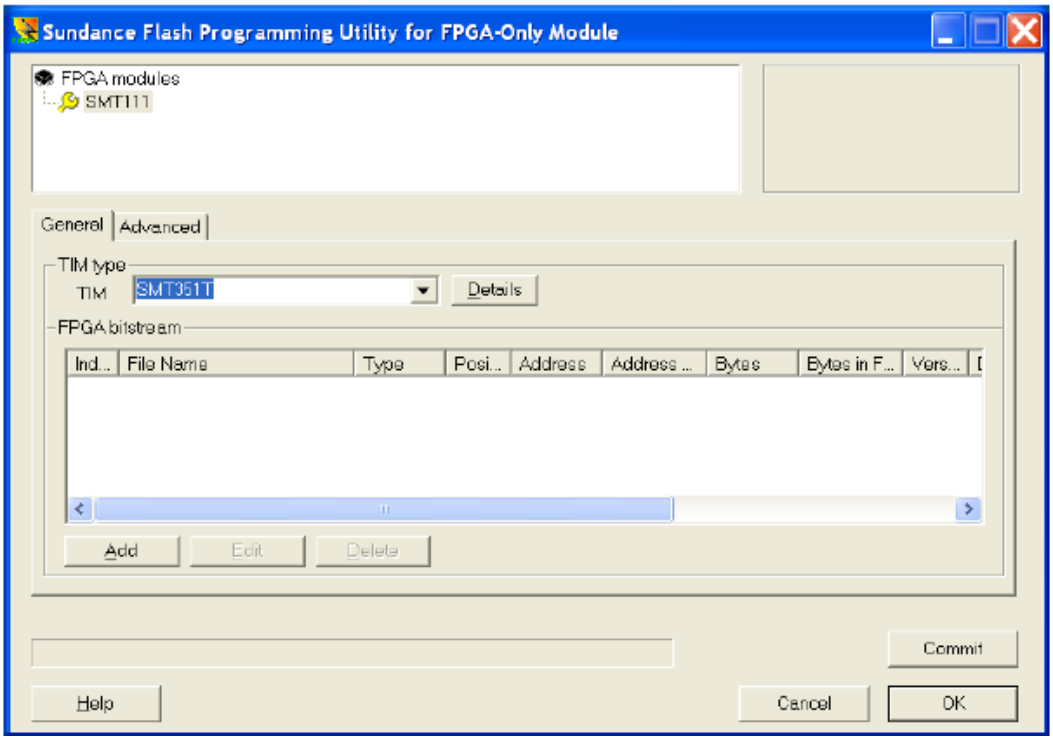


Configure the FPGA. When configuration is complete press the reset button on the SMT111. Do NOT power off the EVP system.

Run the SMT6002 application.



Select the TIM type as SMT351T.

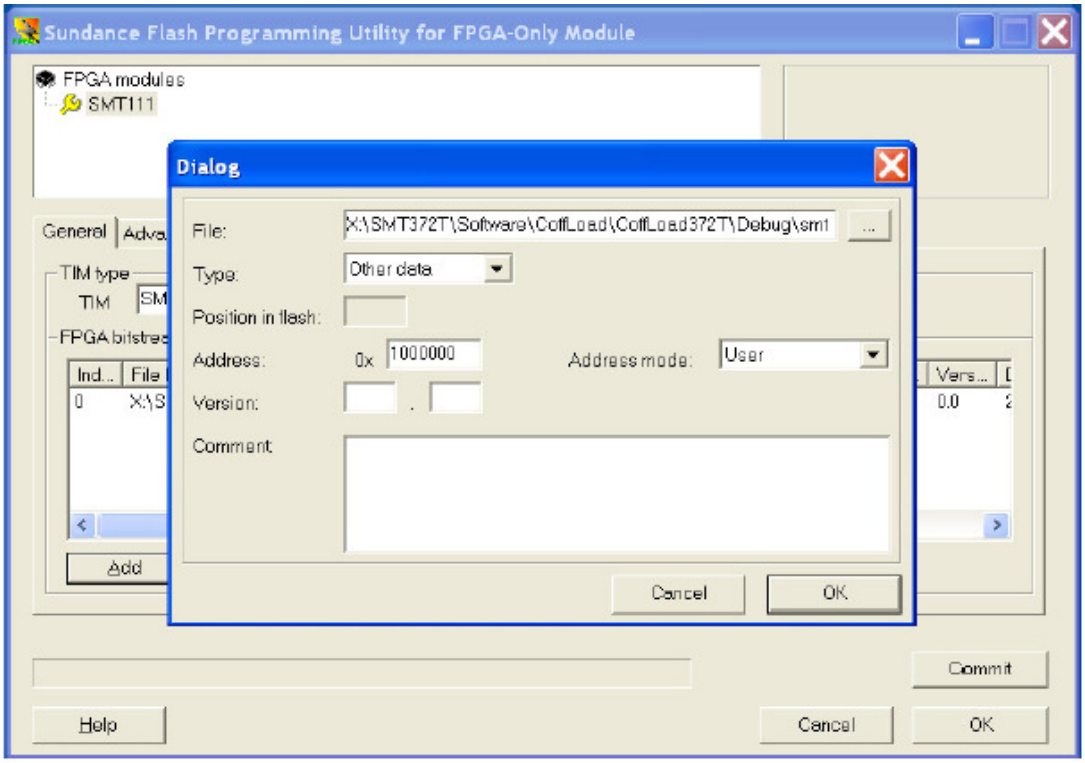


Add the “FPGA.bit” bitstream:

Type: Bitstream; address 0x0; address mode: basic.

Then add the “DSP.bin” DSP application:

Type: other data; address 0x1000000; address mode: user.



Click OK, then Commit. When programming has finished close SMT6002.

4.2 Run the application

Set the DIP-SW as “1111” for normal application.

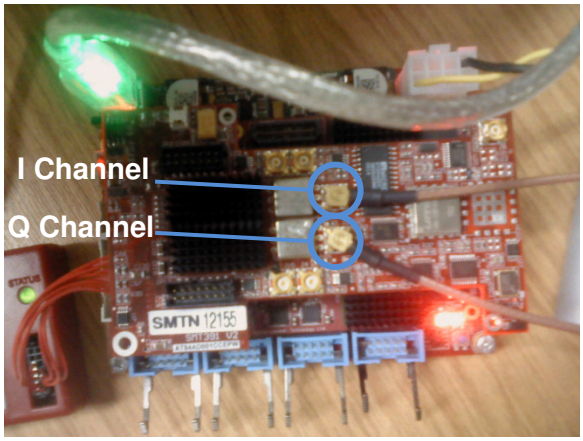
Power off the board, plug in SMT391, and connect with the signal generator, as shown in the picture.

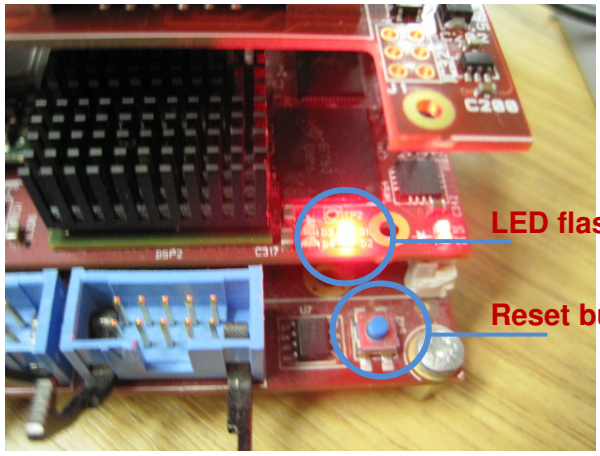
Power on the board, press the reset button to reset the DSP (if success, all of the 4 LEDs should flash for 1 second).

Run the host program (HostCmd.exe), after the command window close, two binary files should be generated.

Use plotting software to plot the data for viewing

To capture another amount of data, press the reset button (do not power off). The 4 LEDs should flash again, afterwards, re-open the host program. The binary file will be overwritten.





Below is a captured ADC example using signal generator with 100KHz frequency and 0.5V amplitude.