Serial ATA Host Controller XV5
VHDL *IP*

Product Brief

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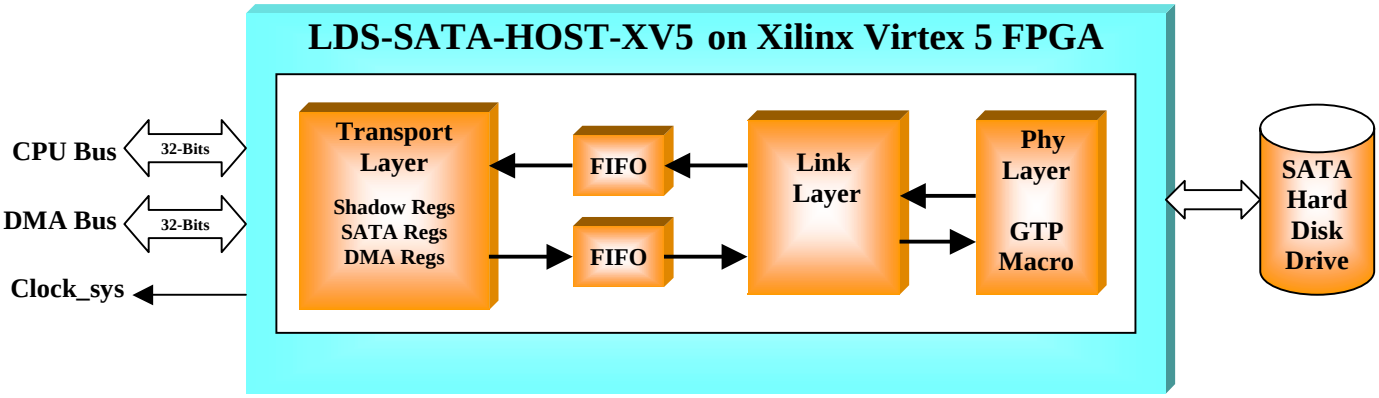

Features

The LDS-SATA_HOST_XV5 IP incorporates the Transport layer, the Link layer and the PHY layer on a Xilinx Virtex 5 FPGA. The LDS-SATA_HOST_XV5 IP is compliant with Serial ATA II specification and signaling rate is 1.5Gbps and scalable to GEN 2. The LDS-SATA_HOST_XV5 IP is fully synchronous with system frequency (Clock_sys) at 37.5MHz in case of GEN1 speed selection and 75MHz in case of GEN 2 speed selection. The VHDL source code format is available for ease of customization. The customization can be done by Logic Design Solutions and **DO254** documentation is available.

Physical Layer features

- Detect OOB and COMWAKE
- Detect the K28.5 comma character and provide a 16 bit parallel output
- Power management mode handled by state machine (shared between Phy and Link layer)
- Provides error indication to upper layers
- 8b/10b encoding and decoding in Xilinx Virtex 5 GTP Macro
- Auto Speed negotiation

Link Layer features

- Scrambling of tx data and descrambling of rx data
- CRC 32 calculation and check from Xilinx Virtex 5 hard macro
- Report transmission status and error to Transport Layer
- Enable BIST loopback and pattern generation modes
- Auto inserted hold primitive to avoid FIFO overflow and underflow
- Partial and slumber power management modes
- The interface between the link layer and the transport layer is 32-bit wide

Transport Layer features

- 48-bits sector address
- Programmed IO (PIO) and DMA modes
- Support BIST FIS transmission and reception
- Automatic error FIS retry capability
- Implement Shadow Registers and SATA SuperSet registers
- Simple synchronous CPU and DMA Interface for data transfers including DMA hold-off capability
- DMA interface can be connected easily to memory space or FIFOs
- Support DMA Abort primitive
- 128-Word Ingress and Egress FIFO between Transport and Link Layer

Verification

- The LDS-SATA_HOST_XV5 IP is available with module and global Test Bench
- The LDS-SATA_HOST_XV5 IP has been validated on the Xilinx ML505 Evaluation board and several hard drives

Design Package

Device Family	**Xilinx Virtex 5 FPGA – speed grade : 1**
Number of Slice Registers	1500
Number of Slice LUTs	2250
Number of LUT Flip Flop pairs used	2600
Number of occupied Slices	980
Package file	**Synthesis Netlist** Data Sheet User's guide . Constraint File
	VHDL Source code VHDL Test Bench Data Sheet Reference Guide User's guide . Constraint File
Design Tool Used	Xilinx XST VHDL synthesis. VHDL ModelSim simulation tool from ModelTech. Xilinx ISE Place and Route software.
Support	Support provided by Logic Design Solutions 1 year e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User Macro modifications. Maintenance Contracts available.

* Rounded Number.
****** Assuming all IP signals are routed off chip.

General Description

The LDS-SATA_HOST_XV5 IP implements a single-chip synchronous Serial-ATA macro which can be used to interface between memory and Serial-ATA devices. The LDS-SATA_HOST_XV5 IP is available only on Xilinx Virtex 5 FPGA.
This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with Serial ATA, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The IP can be easily integrated into hierarchical VHDL designs.

Available Support Products

Support products available from Logic Design Solutions.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Related Information

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