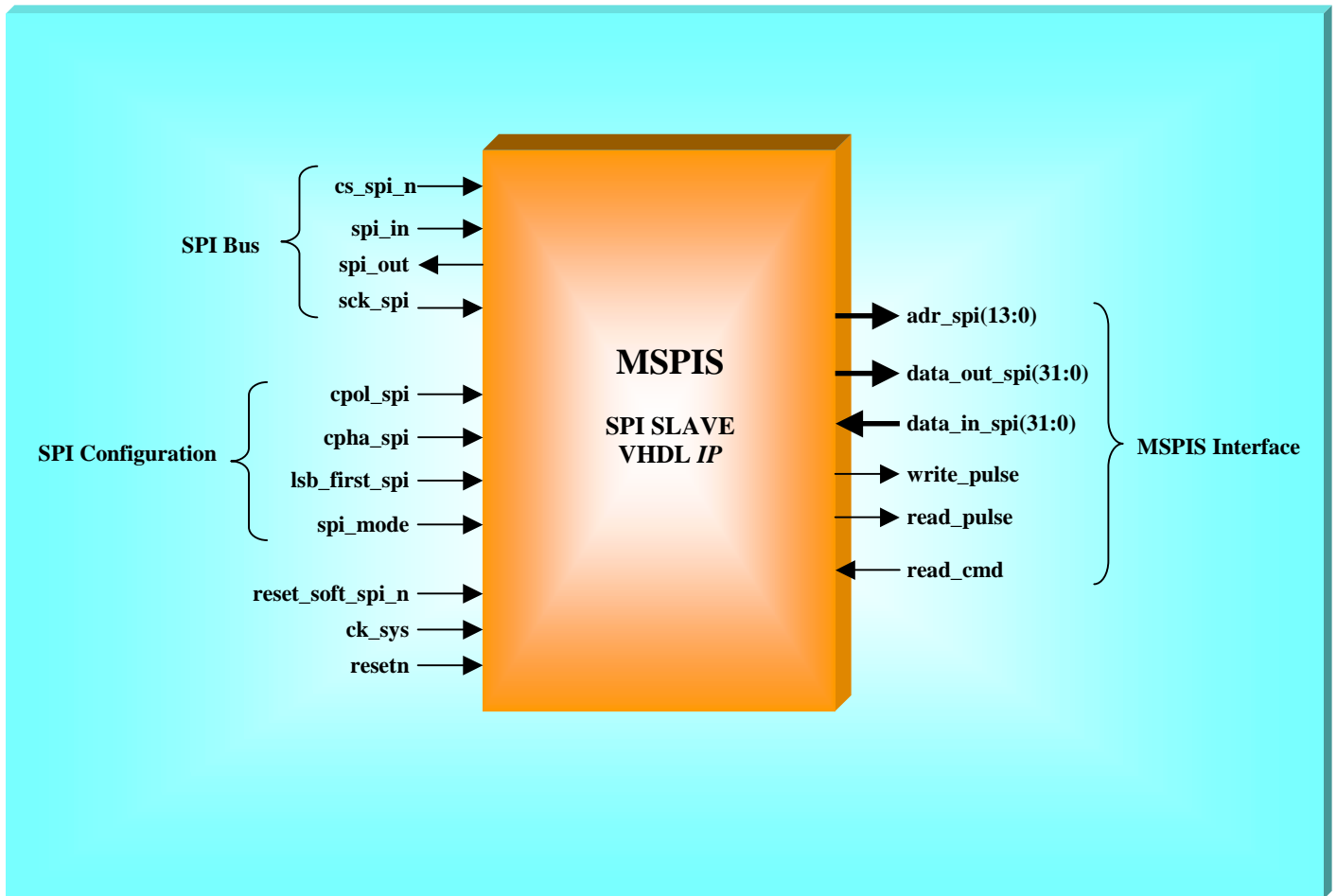


**SPI Slave
Serial Protocol Interface Slave
VHDL IP**

Product Brief

August 06 – Ver. 1.0



Features

- Single-chip synchronous SPI Slave IP in FPGA
- Designed to be included in high-speed and high-performance applications
- Direct Connection to CPU register set
- High frequency rate
- Two run-time mode : Standard SPI mode and Extended SPI mode
- Synchronised on system clock
- Serial clock programmable with polarity and phase
- FPGA speed grade operating frequency dependant : system clock up to 220 MHz
- Available in VHDL source code format for ease of customization
- Can be customised by Logic Design Solutions

Design Package

Device Family	Any FPGA	
LUT/FF	146 LUT4 / 170 FF *	220Mhz *
Tiles / Frequency ProAsic3	230 *	140Mhz *
Tiles / Frequency ProAsic+	368 *	100Mhz *
I/O	92 **	
Package file	VHDL Source code VHDL Test Bench for behavioural and gate level simulation. Data Sheet and Reference Guide User's guide : Simulation, Synthesis and Place and Route procedures. Constraint File	
Design Tool Used	VHDL synthesis Leonardo Spectrum. VHDL ModelSim simulation tool from ModelTech. Place and Route software according FPGA technology.	
Support	Support provided by Logic Design Solutions 6 months e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User Macro modifications. Maintenance Contracts available.	

* Rounded Number.

** Assuming all IP signals are routed off chip.

General Description

The MSPIS IP implements a synchronous a single-chip SPI Slave IP capable of high speed serial data transfer with one SPI master. The MSPIS IP can be programmed to run either in standard SPI mode where bidirectional one byte transactions are implemented, or in extended SPI mode where frame transactions are implemented through 14-bits address and 16 or 32-bits data. The MSPIS IP controls all SPI-bus specific sequences, protocol and timing. This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with Serial SPI, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The IP can easily be integrated into hierarchical VHDL designs.

Available Support Products

Support products available from Logic Design Solutions.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France. Logic Design Solutions also offers IP integration and design services on FPGA.

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