

Tuesday, July 2						
8:30 - 8:40 am Welcome Session: Stefan Krassin   PLC2 & Maria Beyer-Fistrich   Vogel Communications Group						
8:40 - 8:55 am Opening Speech: Ben Lee   Altera						
	Application	AI / ML	Language / Debug / Verification	Embedded	Tools & Methodologies	Tutorials
9:00 am - 10:30 am	Dr. Jörg Pospiech - AVT GmbH Ilmenau Fast data transmission with Artix UltraScale+ via various interfaces (40 min)	Alexander Flick - PLC2 Vitis AI based ML Inference Applications (40 min)	Marco Smutek - Arrow Central Europe GmbH AI generated VHDL code – Fit for practice? (40 min)	Konstantin Dobrosolets - Intel Deutschland GmbH altera Agilinx® 5 FPGAs for Video Solutions (40 min)	Baruch Mitsengendler - The MathWorks GmbH FPGA Verification as Part of Model-Based Design (40 min)	Nikolai Krassin - PLC2 Easy Start FPGA Vivado Part 1: Introduction to the FPGA Development Process (90 min)
	Alexander Daum & Matthias Kern - FH Oberösterreich Studienbetriebs GmbH 100GbE from FPGA to Disk (40 min)	Marco Höfle - Avnet EMG AG AI/ML for Dummies: Designing a hand written number recognition model for an AMD Zynq™ UltraScale+™ platform (40 min)	Jim Lewis - SynthWorks Design Inc The Things I Hate about VHDL (40 min)	Stanislaw Klinke - EBV Elektronik GmbH & Co. KG Unlocking Efficiency: Practical Image Processing with AMD Vitis™ (40 min)	Tom Richter - The MathWorks GmbH Linear Algebra on FPGA - From Theory to Implementation (40 min)	
10:30 - 11:15 am Coffee break						
11:15 am - 12:45 pm	Umran Yungucu - Bull Technologies Reed-Solomon(528,514) Encoder-Decoder Design on FPGA for Low Latency and High Throughput Requirements (40 min)	Stanislaw Klinke - EBV Elektronik GmbH & Co. KG Mastering Adaptable AI: A Deep Dive into AMD Vitis™ AI and Beyond (40 min)	Davide Cieri - Max Planck Institute for Physics Hog (HDL-on-git): handling HDL repositories with git (40 min)	David Kirchner - World of FPGA Video Streaming with Zynq SoC: A Hybrid ARM-FPGA Approach (40 min)	Dimitri Hamidi - The MathWorks GmbH Automating Frame-to-Sample Algorithms Conversion for Vendor-Independent FPGA Implementation (40 min)	Nikolai Krassin - PLC2 Easy Start FPGA Vivado Part 2: FPGA Design Techniques (90 min)
	Tomas Hudson - Monolithic Power Systems GmbH Exploring Efficient FPGA Power Delivery: Multiphase Converters & Integrated Modules (40 min)	Jerry Armao - AMD Polyphase Channelizer Design for AI Engine (40 min)	Dr. Hartmut Schorrig - Vishia Objectoriented FPGA-Hardware designs in Java (40 min)	Dr. Baris Konuk, Afef Zakhama & Francisco Perez Future Electronics S.A. Optimizing power efficiency in Embedded Vision Systems (40 min)	Ernst Wehlage - PLC2 Performing H/W and S/W Co-Simulation using Vitis Model Composer (40 min)	
12:45 - 1:30 pm Lunch break						
1:30 - 2:00 pm KEYNOTE: From FPGAs to Heterogeneous Adaptive SoCs — And the Evolving Developer Experience   Michael Hutchison - AMD						
2:00 - 2:15 pm Short break						
2:15 pm - 3:45 pm	Tomas Hudson - Monolithic Power Systems GmbH & Udo Blaga - Avnet Silica Simplifying Power Design for High-End AMD Xilinx FPGAs: Embracing Integrated Power Modules (40 min)	Jerry Armao - AMD Designing High-Performance DSP Using AI Engines on Versal Adaptive SoCs (90 min)	Markus Leiter - P2L2 OSVVM, Cocotb, VUnit, UVVM, GHDL, NVC – Which Open-Source Tool Should I Use? (40 min)	Anton Fogel & Mathias Sandner - Lauterbach GmbH Improving the Bugfixing of Heterogeneous Multicore Hard- and Softcore Implementations in FPGA SoCs (40 min)	Salma Hamdoun - Arrow Central Europe GmbH Open-Source FPGA Tools and Frameworks (40 min)	Nikolai Krassin - PLC2 Easy Start FPGA Vivado Part 3: VHDL Synthesis and Simulation (90 min)
	Leonardo Di Carlo - Microchip Technology GmbH Benefits of low-power devices at the intelligent edge, a case study (40 min)		Espen Tallaksen - EmLogic AS Making a really advanced, but simple-to-understand FPGA testbench for complex DUTs (40 min)	Ernst Wehlage - PLC2 Inter-Processor Communication and Open AMP (40 min)	Prof. Dirk Koch - Heidelberg University All FPGAs are equal, but some FPGAs are more equal (40 min)	
3:45 - 4:30 pm Coffee break						
4:30 pm - 6:00 pm	Karlo Mlakar - Xylon d.o.o. Configurable HDR ISP Pipeline with the RGB-IR Image Processing Capabilities (40 min)	Dr. Karsten Trott - AMD Adaptive SoC platform for Automotive AI applications (90 min)	Jim Lewis - SynthWorks Design Inc Why Should Our Team be Using VHDL+OSVVM for verification? (40 min)	Stefan Garcia - Intel Deutschland GmbH altera Agilinx® 5 FPGA Hardened Processor Subsystem (HPS) (40 min)	Alexander Wirthmueller - MPSI Technologies GmbH Vendor-agnostic probing of FPGA designs for efficient run-time debugging (40 min)	Nikolai Krassin - PLC2 Easy Start FPGA Vivado Part 4: VHDL Finite State Machines (90 min)
	Andreas Schuler - Missing Link Electronics GmbH FPGA Based 400Gbit/s Data Recorder - Insight into different pitfalls and design choices (40 min)		Sonja Schoissengaijer - FH Oberösterreich Studienbetriebs GmbH Supporting VHDL in Visual Studio Code (40 min)	Thomas Zerrer - Smartlogic GmbH Designing Co-Processor applications with PCI-Express (40 min)	Hans-Jürgen Schwender - TRIAS Mikroelektronik GmbH Introducing Sequential Logic Equivalence Checking (SLEC) (40 min)	
from 7:00 pm Evening Event @ Motorworld Inn in Munich sponsored by AMD						

Wednesday, July 3						
	Application	Basics	AI / ML	Architecture	Safety & Security / Board Design & Connectivity	Tutorial
9:00 am - 10:30 am	Andreas Kick - Siemens AG <b>FPGA Application to Control an Optical Scan Head</b> (40 min)	Ernst Wehlage - PLC2 <b>AMD Design Flows and the Build Formats</b> (90 min)	Dr. Aurang Zaib - Microchip Technology GmbH <b>Application-oriented Flow for Machine Learning on Microchip FPGAs</b> (40 min)	Thomas Siebert - Intel Deutschland GmbH <b>altera Agilex® 5 FPGA External Memory Interfaces (EMIF)</b> (40 min)	Oren Hollander - HandsOn Training <b>Modern FPGAs Security Features</b> (40 min)	Espen Tallaksen - EmLogic AS <b>Verifying a simple DUT (FPGA or module) from scratch with basic verification – for beginners</b> (90 min)
	Patrick Lehmann - PLC2 <b>Continuous Documentation for HDL Engineers</b> (40 min)		Daniel Spahr - Stream Analyze & Martin Kellermann - Microchip Technology GmbH <b>AI/ML Lifecycle Management on FPGA Chipsets with Dynamic Updates</b> (40 min)	Thomas Siebert - Intel Deutschland GmbH <b>Implementing High-Speed Serial Interfaces in altera Agilex® 5 FPGAs</b> (40 min)	Shivani Saravanan - Intel Deutschland GmbH <b>altera Agilex® 5 FPGA Advanced Security Features</b> (40 min)	
10:30 - 11:15 am	Coffee break					
11:15 am - 12:45 pm	Dr. Dmitry Eliseev - RWTH Aachen University <b>An open-source IP-Core to implement a 1GSPS multi-channel ADC within your FPGA</b> (40 min)	Nikolai Krassin - PLC2 <b>Introduction to AMD FPGA Architecture</b> (90 min)	Christian Färber - Intel Deutschland GmbH <b>Introduction to Intel® FPGA AI Suite for altera® FPGAs</b> (40 min)	Oren Hollander - HandsOn Training <b>Cortex-A and Nios V (RISC-V) in Agilex 5</b> (40 min)	Martin Kellermann - Microchip Technology GmbH & Jens Michaelsen - Avnet Silica <b>Embedded system design: know it, know someone, or get to know.</b> (40 min)	Espen Tallaksen - EmLogic AS <b>Verifying a complex DUT in a simple way from scratch</b> (90 min)
	Jorge André Gastmaier Marques - Analog Devices Inc. <b>Open Source I3C Controller, a full stack solution</b> (40 min)		Alexey Lopich - Intel Corporation <b>Camera Pipeline at the Edge: Designing End-to-End Image Signal Processing and AI on FPGAs</b> (40 min)	Dr. Aurang Zaib - Microchip Technology GmbH <b>Embedded Linux Support for Hardware Software Interaction in Microchip FPGA SoCs</b> (40 min)	Harald Friedrich - NewTec GmbH <b>FPGAs in safety critical applications – key considerations, challenges and opportunities in automotive and industrial designs</b> (40 min)	
12:45 - 1:30 pm	Lunch break					
1:30 - 2:00 pm	<b>KEYNOTE: Intelligent edge – empowering innovation by making open-source RISC-V development hardware affordable and accessible   Ted Speers - Microchip Technology Inc.</b>					
2:00 - 2:15 pm	Short break					
2:15 pm - 3:45 pm	Dirk van den Heuvel - Topic Embedded Systems <b>What challenges do we encounter while working at the edge of technology</b> (40 min)	Kamil Rudnicki - Brightelligence sp. z o.o. <b>Overview of highly efficient design techniques for FPGA firmware development flow</b> (40 min)	Martin Kellermann - Microchip Technology GmbH & Jens Michaelsen - Avnet Silica <b>Machine learning: flexible hardware to ease software design</b> (90 min)	Alexander Flick - PLC2 <b>Versal™ Adaptive SoC Architecture and Tool Flow</b> (40 min)	Lukáš Kekely - BrnoLogic <b>Challenges of FPGA-Based SmartNICs for 400 Gbps+</b> (40 min)	Christiaan Baaij - QBayLogic B.V. <b>FPGA design in a functional programming language</b> (90 min)
	Prof. Dr. Markus Pfaff - FH Oberösterreich Studienbetriebs GmbH - P2L2 GmbH <b>RTL on a Higher Level: Introducing the Hierarchical FSMD</b> (40 min)	Harald Flügel - Arrow Central Europe GmbH <b>LUT, logic element, logic cell, system logic cell – Comparing FPGA Complexity</b> (40 min)		Alexander Flick - PLC2 <b>Edge IOT Applications with Versal Adaptive SoCs</b> (40 min)	Dr. Thomas Kirchner - Keysight Technologies Deutschland GmbH <b>Transmitter Output Signal Integrity Tests for 400G and 800G Pluggable Transceivers Modules and Hosts</b> (40 min)	
3:45 - 4:30 pm	Coffee break					
4:30 pm - 6:00 pm	Martin Kellermann - Microchip Technology GmbH <b>Full steam ahead: power-efficient communication solutions</b> (40 min)	Patrick Lehmann - PLC2 <b>Constraining Multiple Clock Domains</b> (90 min)	Joachim Müller - Efinix Inc. <b>RISC-V with Hardware Accelerated AI for Low Power at the Edge</b> (40 min)	Jordan Davies - Avnet Silica <b>Utilising Versal™ HBM</b> (40 min)	Francesco Contu - Avnet EMG Italy Srl (Silica) <b>Designing with high-speed interfaces, debugging techniques and design considerations</b> (40 min)	Christian Michel - Lattice Semiconductor GmbH <b>Golden System Reference Design (GSRD) - a rapid implementation concept for Soft-CPU based designs.</b> (90 min)
	Harry Commin - Enclustra GmbH <b>Fixed-Point Python Co-simulation</b> (40 min)		Dr. Baris Konuk, Afef Zakhama & Francisco Perez - Future Electronics S.A. <b>Artificial Intelligence in Low Power environment</b> (40 min)	Ernst Wehlage - PLC2 <b>Using RAM Resources efficiently for UltraScale+ based Devices</b> (40 min)	Oren Hollander - HandsOn Training <b>Hyperflex FPGA Architecture for Agilex 5 Devices</b> (40 min)	

Thursday, July 4						
	Application	Board Design & Connectivity	Embedded	Tools & Methodologies	Architecture	Tutorials
9:00 am - 10:30 am	Patrick Urban - Cologne Chip AG GateMate FPGA Bitstream Copy Protection using SRAMs (40 min)	Shivani Saravanan - Intel Deutschland GmbH altera Agilex® 5 FPGA IO Architecture and Variable-Pitch BGA Packaging (40 min)	Ernst Wehlage - PLC2 & Jens Michaelen - Avnet Silica MicroBlaze V – the AMD way to do RISC-V (90 min)	Alexander Flick - PLC2 HLS and Vitis™ Libraries: A faithful companionship (40 min)	Nilesh Shilankar & Venu Madhav Ega - Synopsys Optimizing Functional Safety and High Reliability for FPGA-based Design	Jim Lewis - SynthWorks Design Inc Essential Steps to Simplify Testbenches Using OSVVM (90 min)
	Helmut Demel - Lattice Semiconductor GmbH Sensor Fusion applied to maximize accuracy for robots and lidar/radar applications (40 min)	Marco Smutek - Arrow Central Europe GmbH Comparing Power Consumption of FPGAs by altera Security (40 min)		Alain Darte - AMD Optimizing Your C++ Code to Implement High-Performance and Resource-Efficient Designs Using AMD Vitis™ High-Level Synthesis (HLS) Tool(40 min)	Konstantin Dobrosolets - Intel Deutschland GmbH altera Agilex® 5 FPGA Power and Performance Benefits (40 min)	
10:30 - 11:00 am Coffee break						
11:00 am - 12:30 am	Brian Colgan - Microchip Technology GmbH Keeping cool: how to solve challenges in medical applications (40 min)	Joachim Goertz - 3M Rising Demand for High-Speed and High Bandwidth Interconnection (40 min)	Salma Hamdoun - Arrow Central Europe GmbH RISC-V Ecosystem/Mi-V (40 min)	Ido Wermuth - Arrow Central Europe GmbH Advantages of System Design with Low Power FPGAs (40 min)	Tomasz Iwanski - Arrow Central Europe GmbH altera® Hyperflex™: Fixing timings the fast way with Agilex™ FPGAs (40 min)	Jim Lewis - SynthWorks Design Inc Using OSVVM's AXI4 Verification Component (90 min)
	Angelo Lo Cicero - Intel Deutschland GmbH Robotics in altera FPGA (40 min)	To follow shortly (40 min)	Klaus Kohl-Schöpe - Arrow Central Europe GmbH RISC-V® on FPGA (40 min)	Simon Heimbach - Universität Stuttgart Automatic Evaluation and Partitioning of Algorithms for Heterogeneous Systems (40 min)	Harald Werner - Efinix GmbH Modern architectures of programmable devices (40 min)	
12:30 - 1:30 pm Lunch break						
1:30 pm - 3:00 pm	Oliver Bründler - Enclustra GmbH All About AXI - Navigating Standards, Pitfalls and Implementation on Xilinx Devices (40 min)	Karan Kantharia - AMD Leveraging Kria SOMs for Faster Time to Market (40 min)	Alexander Flick - PLC2 & Michal Pacula - Aldec Creating a Versal AI Engine based Data Processing Design (PLC2) Part 1 (40 min)	Wolfgang Loewer - El Camino GmbH Unlocking the Full Potential of Platform Designer from Intel (40 min)	Fabian Kluge - Efinix GmbH High Speed Interfaces (40 min)	Adam Taylor - Adiuvo Engineering & Training Ltd Perfecting PetaLinux – a hands on tutorial Part 1 (90 min)
	Prof. Dr. Bernhard Lang - Hochschule Osnabrück High Performance Pipeline Processing with AXI-Streaming Components (40 min)	Ernst Wehlage - PLC2 The KRIA SOM Family and Design Flows (40 min)	Michal Pacula - Aldec & Alexander Flick - PLC2 Verifying Versal AI Engine based Designs for Optimal Performance (Aldec) Part 2 (40 min)	Shivani Saravanan - Intel Deutschland GmbH What's new In Quartus Pro (40 min)	Maximilian Werner - Efinix GmbH How to use and integrate MIPI CSI-2/DSI with Efinix FPGAs (40 min)	
3:00 - 3:30 pm Coffee break						
3:30 pm - 5:00 pm	Krzysztof Czyz - Embevity sp.zo. O Optimizing FPGA Systems: A Case Study of employing SpinalHDL and VexRISCv core in Commercial Application. (40 min)	Jordan Davies & Jens Michaelen - Avnet Silica Enhance your compute density :- Efficient hardware design, using SOM, SIP, IMC. (40 min)	Fabian Heinrici - Efinix GmbH Efinix RISC-V Solutions from soft to hard (40 min)	Salma Hamdoun - Arrow Central Europe GmbH FPGA Verification and Testing (40 min)	Martin Kellermann - Microchip Technology GmbH Intelligent and reliable industrial designs (40 min)	Adam Taylor - Adiuvo Engineering & Training Ltd Perfecting PetaLinux – a hands on tutorial Part 2 (90 min)
	Pablo Leyva Camacho - Citrobts GmbH MIPI CSI2 on FPGAs, the unexpected challenges (40 min)	Hüseyin Anaç - NCAB Group Germany GmbH Ultra HDI PCBs – all you need to know about it (40 min)	Dr. Riadh Ben Abdelhamid - Heidelberg University Spanning an entire multi-die FPGA with 1,024 RISCv cores/16K Threads at 400MHz? yes you can! (40 min)	Dr. Harald Simmler - Ing. Buero Harald Simmler Efficient High Level Co-Simulation for HDL Designs (40 min)	Bernhard Wandl - FH Oberösterreich Studienbetriebs GmbH - P2L2 GmbH. High Performance Digital Radar on an AMD RFSoc FPGA (40 min)	