
Delivering
Programmable Innovation
Intel FPGA Technology Roadshow 2023

Agenda

- 10:00 Introduction / Welcome
- 10:15 Leading Edge Strategy (rebrand, Intel investments, roadmap, supply update)
- 10:45 Coffee break
- 11:00 Key Features – Agilex® 5 E series
- 12:00 Lunch Break
- 12:30 Update - Secure Device Manager (SDM)
- 13:00 Arrow/Intel Devkit overview: Agilex® 5 FPGA E-series & Solutions
- 13:30 Software : Quartus Prime Pro Edition – New Features & Nios® V Processor (RISC V)
- 14:15 Coffee break
- 14:45 IP / AI Suite / OneAPI
- 15:15 Q&A / Wrap and Closing

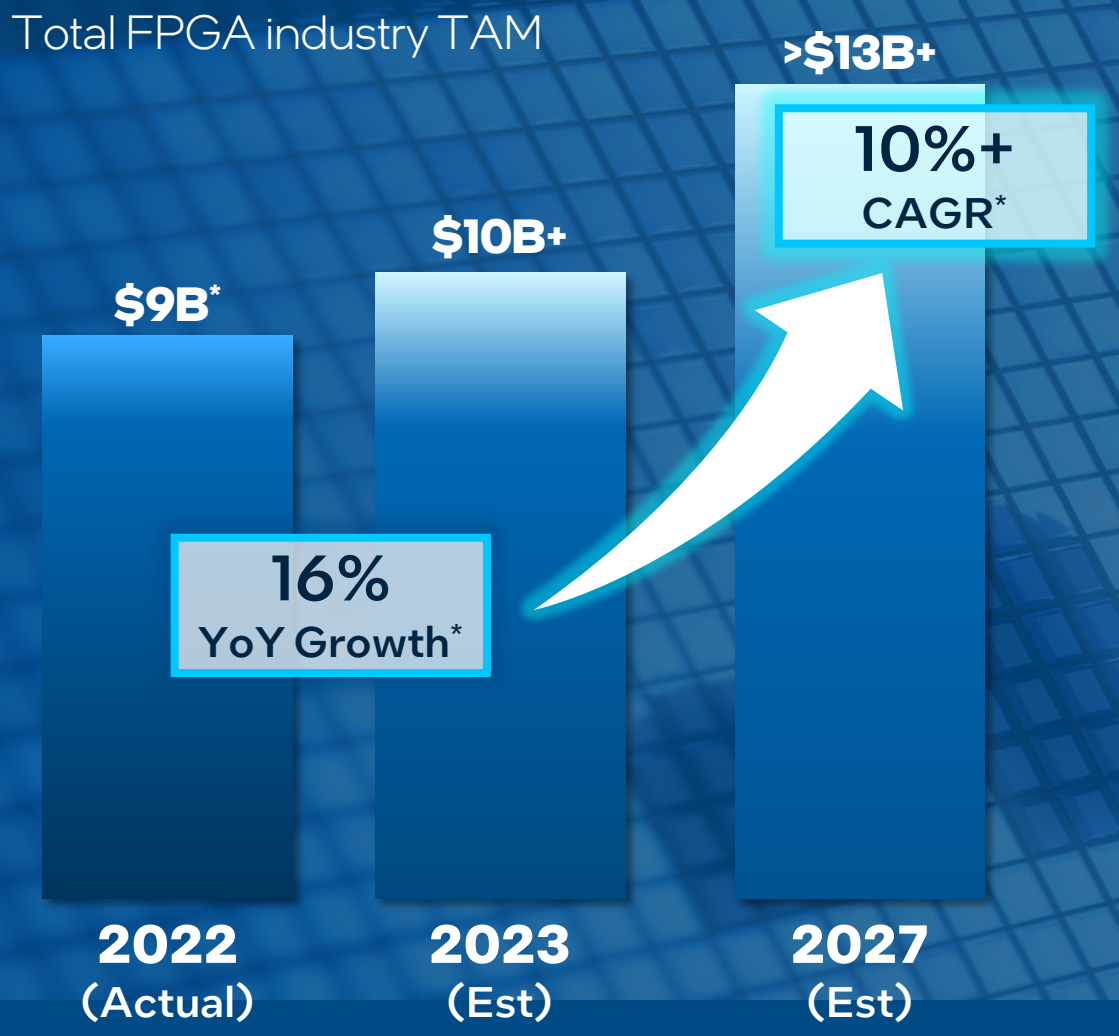
A Message from Intel CEO

Pat Gelsinger Intel CEO

This video is available here: https://www.intel.com/fpgaleadership

PSG Driving the FPGA Industry Momentum

Growth Across Cloud, Enterprise, Network, Edge, and Embedded Markets



- Intel Agilex® FPGA Portfolio
- Workload Diversity from Data Center to the Edge
- Intel Manufacturing Excellence & Supply Resilience
- Intel Portfolio Value

FPGA TAM Sources: AMD/Xilinx, Microchip, Lattice, Achronix, and QuickLogic public statements and PSG analysis

State of Industry

While supply catches up to the short-term demand, traditional supply chain approaches must evolve for the long term

Demand will continue to grow, supply challenge will continue

Digital transformation continues

Macro-environment increasingly complex and less predictable

Delivering Programmable Innovation

Focused on proven execution and delivery of leadership products through a resilient supply chain

Delivering Leadership FPGA and Custom Logic

Q4'22

intel STRATIX 10

intel AGILEX 9

Breakthrough Leadership

FPGAs with industry-leading wideband data converter

NEW

intel AGILEX 7

Performance Leadership

World's first 116 Gbps XCVR & PCIe 5.0 & CXL in production Intel Agilex® 7 FPGA F/R-Tile and 224 Gbps demo

NEW

intel AGILEX 7

intel eASIC

intel IPU

Acceleration Leadership

400G Enhanced Connectivity Intel Agilex® 7 FPGA AGI041 & Intel® eASIC™ N5X080 Device

NEW

intel AGILEX 5

intel AGILEX 3

Expanded Intel Agilex®

Providing Performance & Power Efficiency for All

Extending product leadership in performance per watt and bandwidth across all broad markets

Best-in-Class Developer Experience

Focus on what matters with an enhanced platform and IP automation

Lower TCO

- One speed grade advantage
- Fit into a lower-cost device

Faster TTM

- Intel® Quartus® Prime Software v23.1
- oneAPI Toolkit for IP centric flows
- Intel ® FPGA AI Suite and OpenVINO™ Toolkit

Fits Your Design Flow

- Nios® V/g processor and RISC-V ecosystem
- Open source support

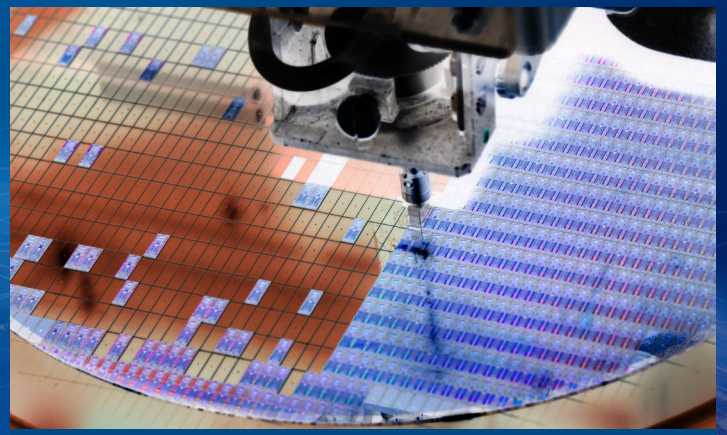
Delivering Leadership Manufacturing: IDM 2.0

Leveraging Intel's leading-edge packaging, process technology, and world-class IP portfolio

Internal Factory Network

Intel's global, internal factory network for at-scale manufacturing

External Foundries



Expanded use of third-party foundry capacity

Intel Foundry

Building a world-class foundry business, Intel Foundry Services

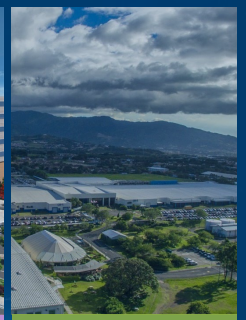
Geographically Diverse Manufacturing Capacity


Oregon


Arizona


New Mexico


Ohio


Costa Rica


Chengdu


Vietnam


Malaysia


Ireland


Germany


Israel

> Intel's ability to combine multiple process technologies – both internal and external – with novel packaging technologies and resilient supply will power the rapid and timely deployment of **L3 Harris** tactical communication devices critical to supporting global security needs

Industry-Leading Products and Supply Chain

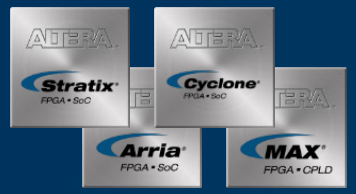
Broad Portfolio Of Programmable Solutions

Best-in-Class Performance and TCO with Supply Resilience

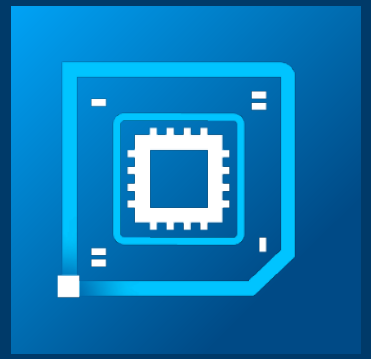
Predictable Supply Commitment

Extended Product Lifecycle

Intel's manufacturing excellence enables supply resilience and product leadership

Before 2015	2015	2017+	2020+	2022+	2023+	Future
	intel ARRIA 10	intel STRATIX 10	intel AGILEX 7	intel AGILEX 9	intel AGILEX 5	intel AGILEX 3
TSMC 28nm & older	TSMC 20 nm	Intel 14 nm	Intel 10 nm SuperFin Intel Agilex® 7 FPGA F-Series, I-Series Intel 7 Intel Agilex 7 FPGA M-Series	Intel 10 nm SuperFin Intel Agilex® 9 FPGA Direct RF-Series	Intel 7 Intel Agilex® 5 FPGA D-Series, E-Series	Intel xx Node disclosure coming soon!

Committed to Delivering Programmable Innovation



Leadership FPGA & Custom Logic

Best-in-Class Developer Experience

Industry-Leading Supply Chain

Lifetime Extensions

intel®

Intel PSG Product Life Cycle Extension

Intel is committed to support long life cycle for its FPGA product families, with the legacy devices at 15 years or more since introduction.

Now, our customers will be even more assured as we announce the life cycle extension for all product families to at least 2035*.

With extended product longevity that mitigates risk of obsolescence and minimizes cost of redesigns, customers will have a peace of mind design-in our products.

Please contact Intel Sales Representatives to learn more about this latest announcement.

* *Intel is committed to provide long life cycle support for all product families (except for HBM2 based devices of Stratix 10 MX, NX, DX and Configuration Devices [EPCQ-A]) until 2035. However, in the event of unforeseen supply disruption such as vendor discontinuance, change in government regulations or production tools obsolescence, Intel will inform its customers.*

Intel PSG Product Life Cycle Extension Summary

	Next Annual EOL Review	
Product Family	Current	New
Intel Agilex® 7 FPGA F-Series or I-Series	2034	2035*
Intel® Stratix® 10 FPGA**	2031	
Intel® Arria® 10 FPGA	2032	
Intel® Cyclone® 10 FPGA	2032	
Intel® MAX® 10 FPGA	2032	
Stratix® III FPGA	2024	2035*
Stratix® IV FPGA	2025	
Stratix® V FPGA	2027	
Arria® II FPGA	2025	
Arria® V FPGA	2028	
Cyclone® II FPGA	2024	
Cyclone® III FPGA	2032	
Cyclone® III LS FPGA	2027	
Cyclone® IV FPGA	2032	
Cyclone® V FPGA	2032	
MAX® II CPLD	2032	
MAX® V CPLD	2032	

** Unforeseen supply disruptions may impact Intel's ability to offer the products*
*** Excluding HBM2 based devices of Stratix 10 MX, NX & DX*

The Intel Agilex® FPGA Portfolio is Growing

Intel Agilex® FPGA Portfolio

Comprehensive

- Intel Agilex® FPGAs cover all levels of performance, power, logic capacity, and form factor
- Addresses wide range of workloads and a full breadth of programmable logic needs across many application areas, including cloud, network, edge and embedded

Optimized

- Advanced chiplet-based architecture delivers first-to-market capabilities for customer innovation:
  - 116 Gbps transceivers
  - PCI Express 5.0
  - Compute Express Link (CXL)
- Leadership performance and power:
  - 50% higher performance[1]
  - 2X better fabric performance per watt[1]
- Optimized form factors across families

Unified

- Unified architecture for ease of adoption and design migration
- Enabled by a powerful, intuitive tool offering best-in-class developer experience:
  Intel® Quartus® Prime Software
- Leveraging Intel manufacturing for reliable supply and supply resilience

Note (1) : Compared to competitive 7 nm FPGAs. See www.intel.com/performanceindex for more info

Intel Agilex® FPGA Product Families

	Description	Series
intel AGILEX 9	Pushing beyond the limits of mainstream programmable logic—these FPGAs provide unprecedented capabilities and optimization for their target applications	Direct RF-Series
intel AGILEX 7	Highest performance FPGAs delivering industry-leading fabric and I/O speeds, ideal for the most bandwidth- and compute-intensive applications	M-Series
		I-Series
		F-Series
intel AGILEX 5	Midrange FPGAs optimized for applications requiring high performance, lower power, and smaller form factors	D-Series
		E-Series
intel AGILEX 3	Power- and cost-optimized FPGAs in compact form factors—essential building blocks targeted for a wide range of applications across many markets	Coming Soon

Intel® FPGA Portfolio and Roadmap

	Today				Coming Soon	
	intel STRATIX	intel STRATIX 10	intel AGILEX 7	intel AGILEX 7	intel AGILEX 7	intel AGILEX 9
	Stratix® V Devices	GX / SX / TX / MX / DX / NX / AX	F-Series	I-Series	M-Series	Direct RF-Series
	intel ARRIA	intel ARRIA 10			intel AGILEX 5	intel AGILEX 5
	Arria® V Devices	GX / SX / GT			E-Series	D-Series
	intel MAX	intel CYCLONE			intel AGILEX 3	
	II / V / 10	IV / V / 10			TBA	

	Intel Agilex® 9 FPGAs Direct RF-Series	Intel Agilex® 7 FPGAs F-Series / I-Series / M-Series	Intel Agilex® 5 FPGAs E-Series / D-Series	Intel Agilex® 3 FPGAs
Logic Capacity Range (logic elements)	1.4M – 2.7M	573k – 4M	50k – 656k	Coming Soon
Memory (Max)	287 Mb	485 Mb (32 GB HBM2e option)	69 Mb	
DSP Type	Variable-Precision DSP Blocks	Variable-Precision DSP Blocks	Enhanced DSP With AI Tensor Blocks	
18x19 Multipliers (Max)	17,056	25,584	3,680	
Hard Processor Options	Quad-Core Arm Cortex-A53	Quad-Core Arm Cortex-A53	Dual-Core Arm Cortex-A76 Dual-Core Arm Cortex-A55	
High-Speed Interfaces (max data rate)	58 Gbps XCVRs 64 Gsps ADC/DAC	116 Gbps XCVRs	28 Gbps XCVRs	
Processor Interfaces	PCIe 4.0	PCIe 4.0/5.0, CXL	PCIe 4.0	
Memory Interfaces	DDR4, QDR IV	DDR4/5, LPDDR5, QDR IV	DDR4/5, LPDDR5, QDR IV	
I/O Count (Max)	660	768	504	
XCVR count (Max)	32	120	32	
Package Size (Min)	45x32mm	37.5x34mm	15x15mm	

Unprecedented Capabilities and Optimization for Target Applications

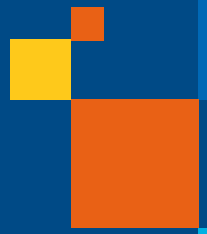
Higher Performance
More Features and Capabilities
Increasing Logic Capacity
Greater IO Bandwidth

Lower Power
More Cost Optimizations
Less Logic Capacity
Smaller Form Factors

Intel Agilex® 5 FPGA vs. similar existing Intel products

	Cyclone® V E/GX/GT/SE/SX/ST	Arria® V GX/GT/GZ/SX/ST	Intel Agilex® 5 FPGAs E-Series / D-Series	Intel Agilex® 3 FPGAs
Logic Capacity Range (logic elements)	25K – 300K	75k – 504K	50k – 656k	Coming Soon
Memory (Max)	14Mb	39Mb	69 Mb	
DSP Type	Variable-Precision DSP Blocks	Variable-Precision DSP Blocks	Enhanced DSP With AI Tensor Blocks	
18x19 Multipliers (Max)	684	2,312	3,680	
Hard Processor Options	Dual-Core Arm Cortex-A9	Dual-Core Arm Cortex-A9	Dual-Core Arm Cortex-A76 Dual-Core Arm Cortex-A55	
High-Speed Interfaces (max data rate)	6 Gbps XCVRs	12.5 Gbps XCVRs	28 Gbps XCVRs	
Processor Interfaces	PCIe 1.0/2.0	PCIe 2.0/3.0	PCIe 4.0	
Memory Interfaces	DDR2/3, LPDDR2	DDR3	DDR4/5, LPDDR5, QDR IV	
I/O Count (Max)	560	704	504	
XCVR count (Max)	12	36	32	
Package Size (Min)	11x11 mm	27x27 mm	15x15 mm	

Key Features – Intel Agilex® 5 E-Series



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Intel Agilex® 5 FPGAs

Midrange FPGAs optimized for applications requiring high performance, lower power, and smaller form factors

HPS

FPGA industry's first asymmetric applications processor system

SDM

device security

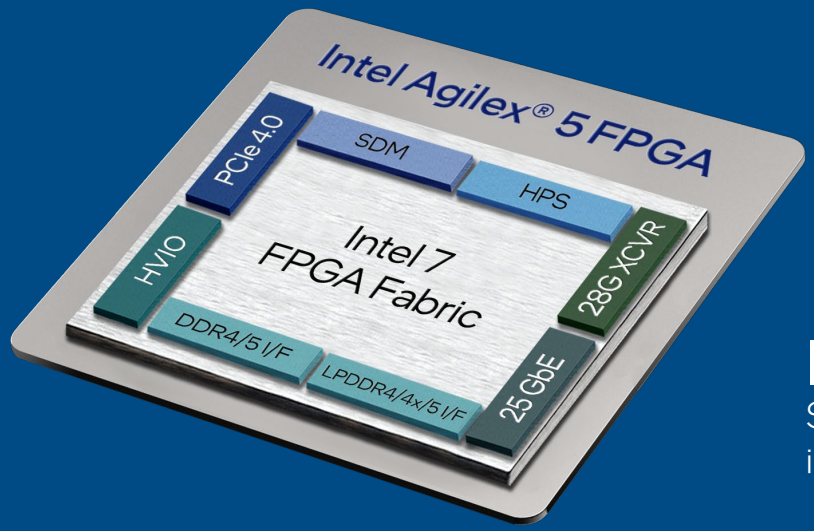
MIPI D-PHY

CSI-2 up to 8 lanes at 2.5 Gbps
DSI-2 up to 4 lanes at 3.5 Gbps

NEW

Advanced Memory Interface Support

Support industry standard DDR4, DDR5, LPDDR4, and LPDDR5



Enhanced DSP with AI Tensor Block

Three new modes: Tensor Mode, Complex Mode, INT9 vector Mode

Time-Sensitive Network

TSN MAC controller or end point

HPS has 3 TSN end point 10M-2.5G

Integrated XCVR (28G)

Supports up to 32 x 28 Gbps data rates for data-intensive applications

PCIe

Supporting up to PCIe 4.0 x8 bandwidth and PCI-SIG compliant

Functional safety

IEC 61508 SIL 3

Ethernet

Configurable networking support including hard Ethernet media access control (MAC), physical coding sublayer (PCS),

Intel Agilex® 5 Product Portfolio

Common Features

- Multi-Core Arm processor* (2xA55+2xA76)
- USB 3.1 /3-TSN endpoints*
- 2nd Generation Intel Hyperflex™ Architecture
- 3.3V I/O, 1.6 Gbps LVDS MIPI @2.5G
- DDR41, LPDDR4, LPDDR5

E-Series FPGAs Device Group B

- Logic Density 50kLE–656kLE
- Fabric Speed: 350 MHz
- 17G Transceivers*
- PCIe 3.0/4.0+ x4 and 10GbE (MAC+PCS) Hard IP*
- DDR4-32b @ 2,400 Mbps LPDDR4-32b @ 2,667 Mbps LPDDR5-32b @ 2,400 Mbps

E-Series FPGAs Device Group A

- Logic Density 138kLE–656kLE
- Fabric Speed: 500 MHz
- 28G Transceivers
- PCIe 4.0 x4 and 25GbE (MAC+PCS) Hard IP
- DDR4-32b @ 3,200 Mbps LPDDR4-32b @ 3,733 Mbps LPDDR5-32b @ 3,733 Mbps DDR5-32b @ 3,600 Mbps
- MIPI @3.5G

D-Series

- Logic Density 103kLE–644kLE
- Fabric Speed: 600 MHz
- 28G Transceivers
- PCIe 4.0 x4/8 and 25GbE (MAC+PCS) Hard IP
- DDR4-64b @ 3,200 Mbps LPDDR4-32b @ 4,267 Mbps LPDDR5-32b @ 4,267 Mbps DDR5-32b @ 4,000 Mbps
- DDR4 DIMM, QDR IV
- MIPI @3.5G
- Increased DSP/M20K Ratio

Smaller Form Factor/ Lower Power ⟷ **Higher Performance / More Capabilities**

1 DDR4 Component Only (except Agilex 5 D-Series devices)
+ PCIe 4.0 support in -4S speed grade only
* Some SKUs in E-Series Device Group B are available as I/O only devices (no HPS or txvr option 50-70 KLEs)

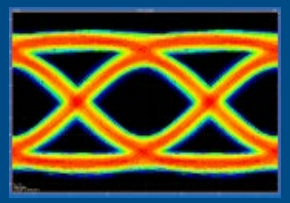
Intel Agilex® 5 FPGAs Technology Enablers for Power-Efficient Performance

Intel® 7 Process Technology

- Advanced process technology with interconnect innovations

2nd Generation Intel® Hyperflex™ FPGA Architecture

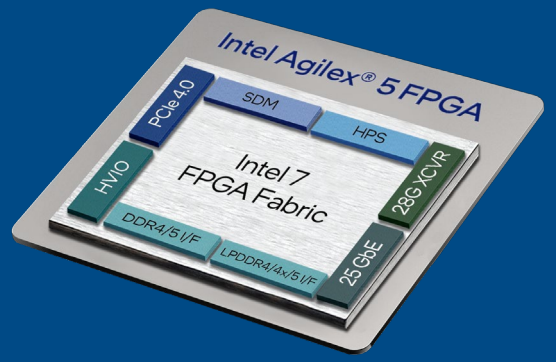
- Delivers higher performance than Cyclone® V FPGAs while minimizing power



High level of system integration

- High-speed transceiver I/O, DDR memory I/O, GPIO, and Hard Processor Systems (HPS)

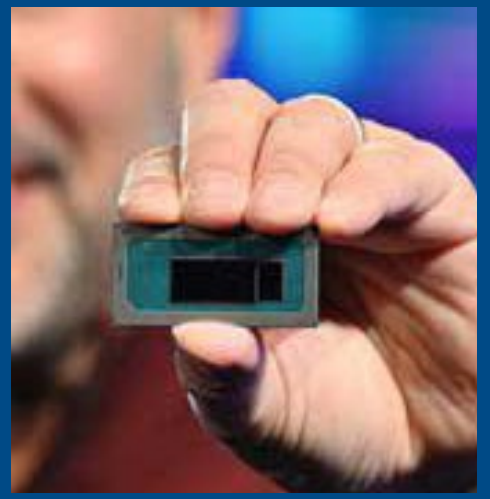
Intel 7 Technology



Intel Agilex® 7 M-Series FPGA
Intel Agilex® 5 FPGA

Intel 7

- ~10% improvement in performance per watt
- More thick metal layers and MIMs, new lower-k dielectric
- Novel high-density patterning and thin barrier



Used in 12th Gen Intel Core (Alder Lake) Processors

Intel 7 now in volume production

*Graphics for illustrative purposes only and is not to scale
Internal estimates, results may vary. Process readiness timing does not necessarily indicate product production timing. Learn more at www.intel.com/PerformanceIndex. Results may vary.

Intel Agilex® 5 FPGAs E-Series Family Table

Device SKU options:
A = No HPS, No XCVR
B =Quad HPS, No XCVR
C= No HPS, XCVR
D= Quad HPS, XCVR
E =Dual HPS (2xA55), No XCVR
G= No HPS, No XCVR, Crypto Services (enabled) – for B18A package only

Product Line		A5E005B	A5E007B	A5E008B	A5E013B	A5E028B	A5E043B	A5E052B	A5E065B	A5E013A	A5E028A	A5E043A	A5E052A	A5E065A
Device Group		B								A				
Logic	kLEs	50	69	85	138	282	434	524	656	138	282	434	524	656
Options	Specification	A,G	A,G	A,C,D,E,	A,B,C,D,E	A,B,C,D,E	C,D	C,D	C,D	C,D	C,D	C,D	C,D	C,D
Embedded RAM	M20K	130	179	229	358	716	1050	1288	1611	358	716	1050	1288	1611
	M20K (Mb)	2.54	3.50	4.47	6.99	13.98	20.51	25.16	31.46	6.99	13.98	20.51	25.16	31.46
	MLAB (Mb)	0.52	0.71	1.09	1.43	2.92	4.10	5.13	6.79	1.43	2.92	4.10	5.15	6.79
DSP	18x19 Mults.	130	188	232	376	752	1128	1352	1692	376	752	1128	1352	1692
Peak INT8	Tera Operations / Second [TOPS]	1.70	2.34	3.00	4.69	9.38	13.76	16.87	22.10	5.78	11.55	17.33	20.78	25.99
GPIO (HVIO)	HVIO	160	160	200	200	200	120	120	120	200	200	120	120	120
GPIO (HSIO)	HSIO (1.05V -1.3 V)	96	96	192	192	192	384	384	384	192	192	384	384	384
	1.3 V LVDS pairs @1.6Gbps	48	48	96	96	96	192	192	192	96	96	192	192	192
	DDR4/LPDDR4/ DDR5*/LPDDR5	1x -32b	1x -32b	2x -32b	2x-32b	2x-32b	4x-32b	4x-32b	4x-32b	2x-32b	2x-32b	4x-32b	4x-32b	4x-32b
	MIPI D-PHY	7	7	14	14	14	28	28	28	14	14	28	28	28
Serial IO & Protocol HIP	Transceivers Max rate (Count)	-	-	17G (4)	17G (4)	17G (12)	17G (16)	17G (24)	17G (24)	28G (4)	28G (12)	28G (16)	28G (24)	28G (24)
	PCIe 4.0 Instances	-	-	4.0 1(x4)	4.0 1(x4)	4.0 3(x4)	4.0 4(x4)	4.0 4(x4)	4.0 6(x4)	4.0 1(x4)	4.0 3(x4)	4.0 4(x4)	4.0 6(x4)	4.0 6(x4)
	Ethernet (MAC & PCS)	-	-	1x10GbE	1x10GbE	3x10GbE	4x10GbE	4x10GbE	6x10GbE	1x25GbE	3x25GbE	4x25GbE	4x25GbE	6x25GbE
HPS	Hard Processor	-	-	2xA76 up to 1.4 GHz + 2xA55 up to 1.25 GHz						2xA76 up to 1.8 GHz + 2xA55 up to 1.5 GHz				
	Cache Sizes	-	-	A55: L1/L2$: 32KB/128KB, A76:L1/L2$: 64KB/256KB, LLC: 2MB						A55: L1/L2$: 32KB/128KB, A76:L1/L2$: 64KB/256KB, LLC: 2MB				

Note: Device Group A FPGAs only supported with SmartVID, Device Group B FPGAs only supported with fixed voltage (0.75V, 0.78V, 0.8V)

Package Size, Min Ball pitch, Grid Array Pattern	HVIO/ HSIO/Transceivers												
B15A (15mmx15mm, 0.65mm, balls anywhere)	80/62	80/62											
M16A (16mmx16mm, 0.5mm, standard)			40/192/4	40/192/4	40/192/8								
B18A (18mmx18mm,0.65mm,balls anywhere)	160/52	160/52											
B23B (23mmx23mm, 0.65mm, balls anywhere)	160/96	160/96	160/192	160/192	160/192								
B23A** (23mmx23mm, 0.65mm, balls anywhere)			120/96/4	120/96/4	120/96/12	120/96/12	120/96/12	120/96/12	120/96/4	120/96/12	120/96/12	120/96/12	120/96/12
B32A**(32mmx32mm, 0.65mm, balls anywhere)			200/192/4	200/192/4	200/192/12	120/384/16	120/384/24	120/384/24	200/192/4	200/192/12	120/384/16	120/384/24	120/384/24

** Conditional migration path, please refer to Intel® Agilex™ 5 FPGAs E-Series Device Migration Guidelines Application Note (to be published in Q2'23) for migration details

*Product table is preliminary and subject to change. Resource counts will vary by package options.*Performance specs may vary by speed grade. HPS and Transceivers available on select OPNs*

Intel Agilex® 5 FPGAs D-Series Family Table

Device SKU options:
C= No HPS, XCVR
D= Quad HPS, XCVR

Product Line		A5D010	A5D025	A5D031	A5D051	A5D064
Logic	KLEs	103	254	318	515	644
SKU Options	Specification	C,D	C,D	C,D	C,D	C,D
Embedded RAM	M20K	534	1281	1602	2563	3204
	M20K (Mb)	10.43	25.02	31.29	50.06	62.58
	MLAB (Mb)	1.09	2.09	3.30	5.15	6.67
DSP	18x19 Mults	552	1472	1840	2944	3680
Peak INT8	Tera Operations / Second [TOPS]	8.48	22.61	28.26	45.22	56.22
GPIO (HVIO)	HVIO (1.8 V - 3.3 V)	60	60	60	60	60
GPIO (HSIO)	HSIO (1.05 V -1.3 V)	384	384	384	384	384
	1.3V LVDS pairs @1.6 Gbps	192	192	192	192	192
	DDR4/LPDDR4/DDR5/LPDDR5	4x-32b/2x-64b	4x-32b/2x-64b	4x-32b/2x-64b	4x-32b/2x-64b	4x-32b/2x-64b
	MIPI D-PHY	28	28	28	28	28
Serial IO & Protocol HIP	Transceivers Count (28G)	16	16	16	24	32
	PCIe 4.0 HIP	2(x8), 4(x4)	2(x8), 4(x4)	2(x8), 4(x4)	3 (x8), 6(x4)	4 (x8), 8(x4)
	Ethernet (MAC & PCS)	8x25GbE	8x25GbE	8x25GbE	12x25GbE	16x25GbE
HPS	Hard Processor	2xA76 up to 1.8 GHz + 2xA55 up to 1.5 GHz				
	Cache Sizes	A55: L1/L2$: 32 KB/128 KB, A76:L1/L2$: 64 KB/256 KB, LLC: 2 MB				

Note: Intel® Agilex™ 5 FPGAs D-Series only supported with SmartVID

Package Size, Min Ball pitch, Grid Array Pattern	HVIO/ HSIO/Transceivers				
B23A (23 mm x23 mm, 0.65 mm, balls anywhere)	60/192/8	60/192/8	60/192/8		
B32A (32 mm x 32 mm, 0.65 mm, balls anywhere)	60/384/16	60/384/16	60/384/16	60/384/24	60/384/32

*Product table is preliminary and subject to change. Resource counts will vary by package options.*Performance specs may vary by speed grade. HPS and Transceivers available on select OPNs*

Architecture and Features

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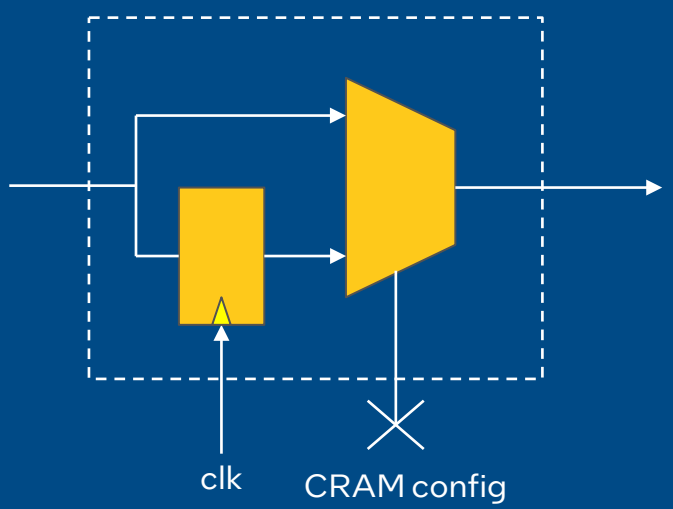
2nd Gen Intel® Hyperflex™ FPGA Architecture

- Intel Agilex® 5 FPGAs have Hyper-Registers throughout the core fabric
- Bypassable Hyper-Registers in every routing segment
- Bypassable Hyper-Registers on all block inputs
  - ALMs, M20K blocks, DSP blocks, I/O cells
- Register location is fine-grained
  - Throughout the interconnect
  - Available in optimal locations

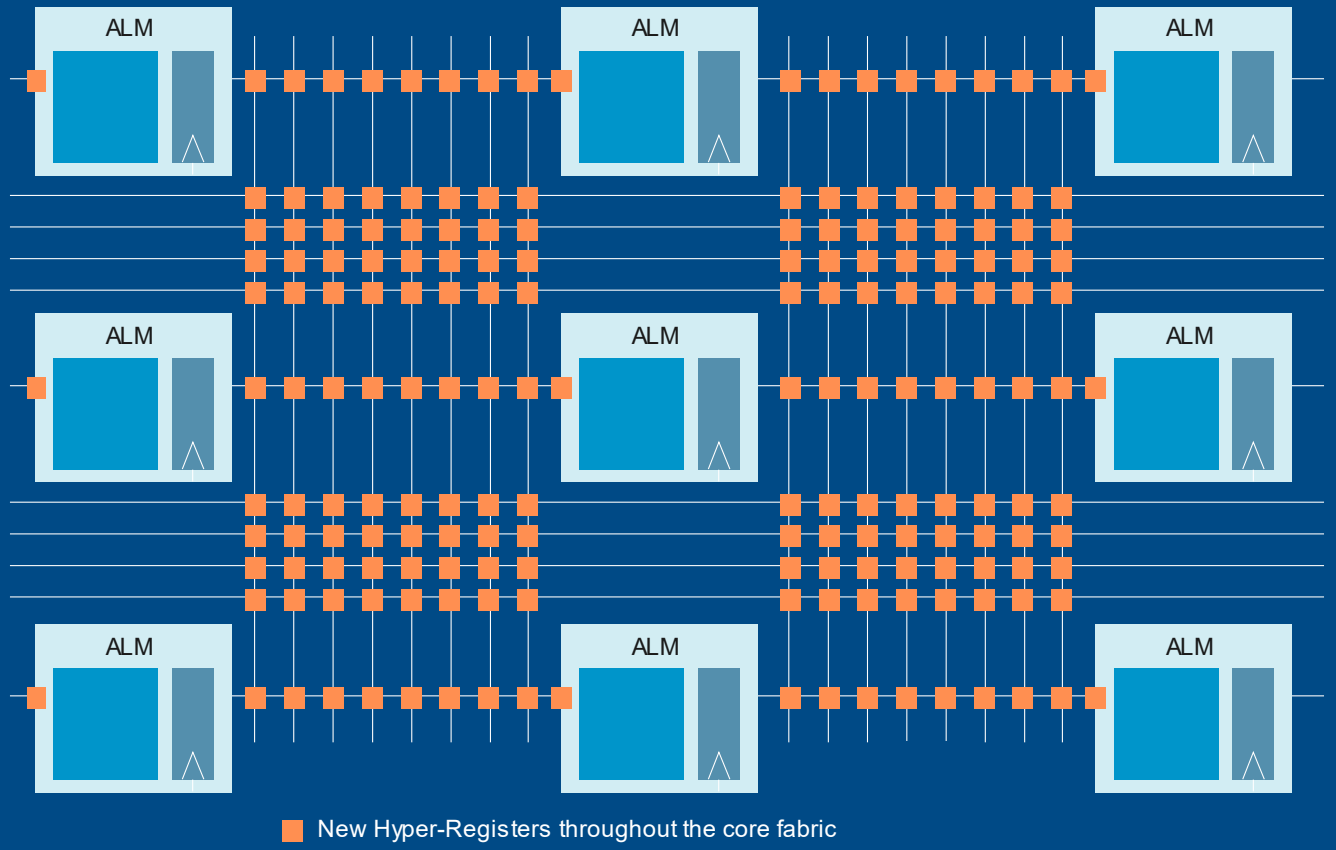


Bypassable Hyper-Register

Available "everywhere" throughout user logic and interconnect

2nd Gen Intel® Hyperflex™ FPGA Architecture

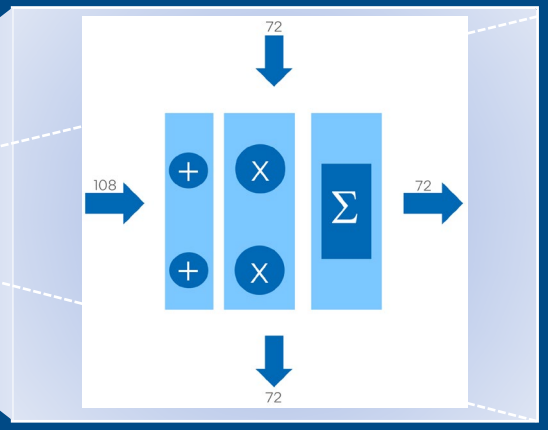
- Hyper-Registers in all routing segments
- Design tools utilize registers for retiming and fitting optimizations:
- *Retiming*
- *Pipelining*



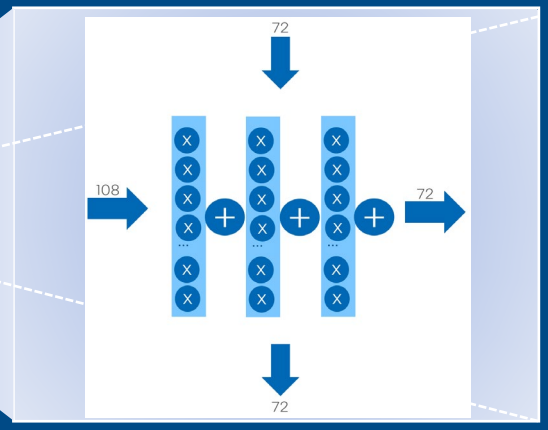
Registers Everywhere

Intel Agilex® 5 FPGA Enhanced DSP with AI Tensor

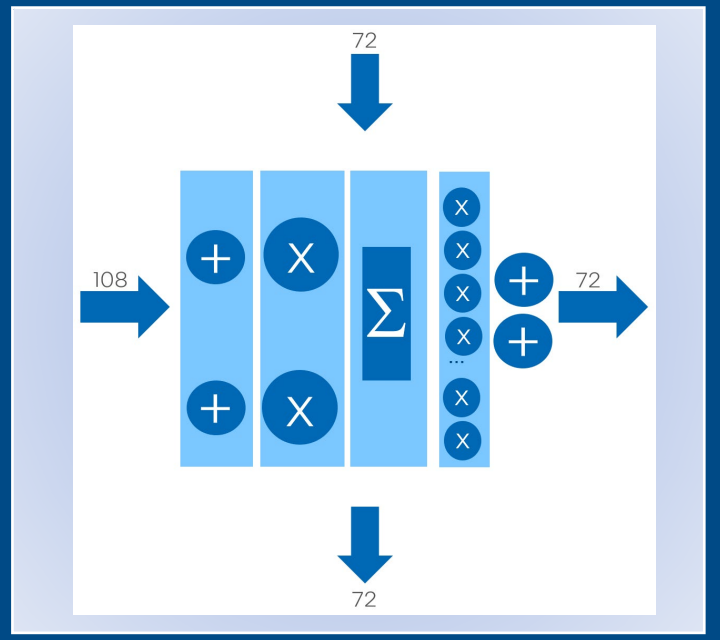
Intel Agilex® 7 FPGA DSP Block



Intel® Stratix® NX FPGA Tensor Block



Intel Agilex® 5 FPGA DSP and Tensor Block



- Standard Intel Agilex® 7 FPGA features supported
- Enhanced complex number support
- Enhanced for AI/ML & dot product support

DSP with AI Tensor

- Variable Precision DSP
  - Trades precision with compute performance
    - More computation units when configured for lower precision
  - Each DSP individually configurable
  - Each DSP chainable
- Continued High-Precision DSP performance
  - Support for 4X lower precision and 2X complex mults
- Dense AI processing support for compact data types
  - Support for multiple AI industry standard data types
- Tight Fabric Coupling
  - Ensures no data bottlenecks

Number of Operations per DSP

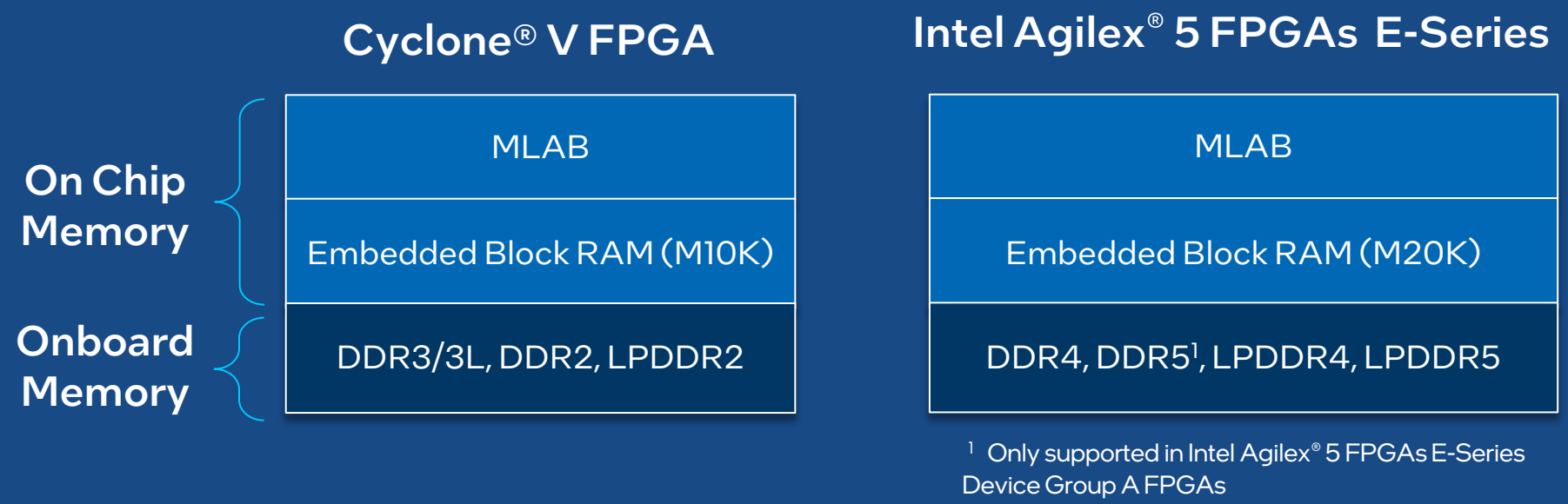
Data Type	Intel Agilex® 5 FPGA	DSP	AI
INT4	20		✓
INT8	20		✓
INT9	6	✓	
INT16	2		✓
CINT16	1	✓	
INT18x19	2	✓	
INT24	1		✓
INT27	1	✓	
INT32	0.5		✓
Bfloat16	2		✓
FP16	1		✓
FP19	1		✓
FP32 Add	1	✓	✓
FP32 Mult	1	✓	✓

Agilex® 5 vs Agilex® 7

- 100% compatible with Agilex 7
- Improved Performance over Agilex 7
  - 5X INT8 performance
  - 1.5X 9x9 performance
  - 2X 16x16 Complex performance
    - Single DSP per 16-bit Complex multiplication
  - 2X Half-precision performance
  - 2X support for industry standard TF32 data types
    - A 19-bit FP type used in AI
- Equal Support in All Other cases

Data Type	Agilex® 5		Agilex® 7
INT8	20	↑	4
INT9	6	↑	4
INT16	2	↔	2
CINT16	1	↑	0.5
INT18x19	2	↔	2
INT24	1	↔	1
INT27	1	↔	1
Bfloat16	2	↔	2
FP16	2	↑	1
TF32 (1)	2	↑	1
FP32 Add	1	↔	1
FP32 Mul	1	↔	1

Expanded Memory Hierarchy and Capacities



[1] Only supported in Intel Agilex® 5 FPGAs E-Series Device Group A FPGAs

Wide range of memory options to address edge-optimized applications' need for low latency, high throughput, low-power high-density needs

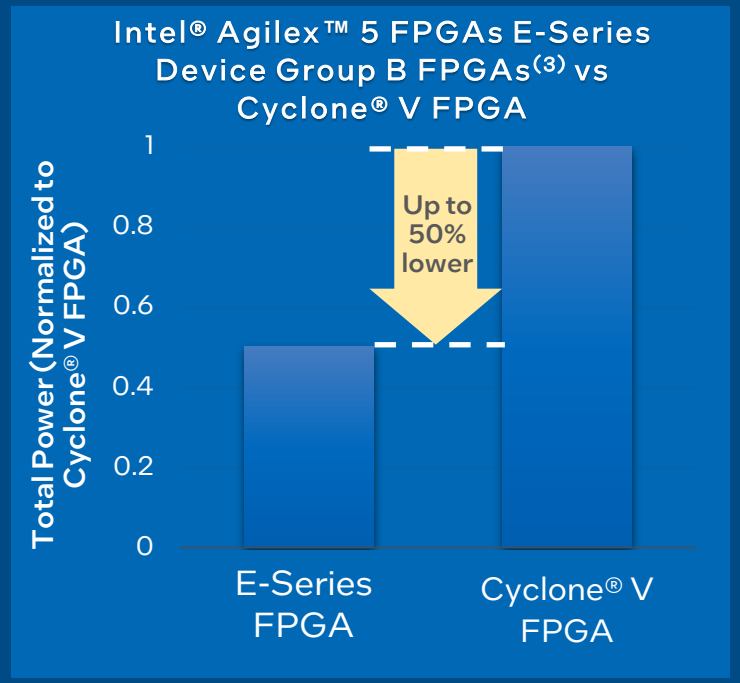
Onboard Memory Speeds

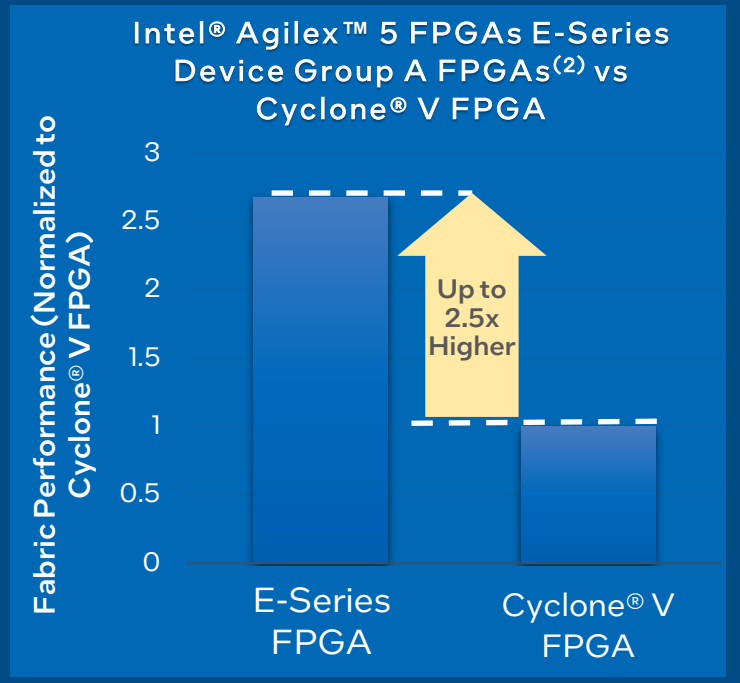
Intel Agilex ® 5 FPGAs E-Series–Device Group B FPGAs (MT/s)	Intel Agilex® 5 FPGAs E-Series– Device Group A FPGAs (MT/s)
DDR4 (2,400)	DDR4 (2,667)
LPDDR4 (2,667)	LPDDR4 (3,733)
	DDR5 (3,600)
LPDDR5 (2,400)	LPDDR5 (3,733)

All max performance numbers are projected for mid-speed grade devices

Fabric Performance and Total Power

- Intel Agilex® 5 FPGAs E-Series is up to 2.5X higher fabric performance or up to 50% lower total power compared to Cyclone® V FPGA(1)

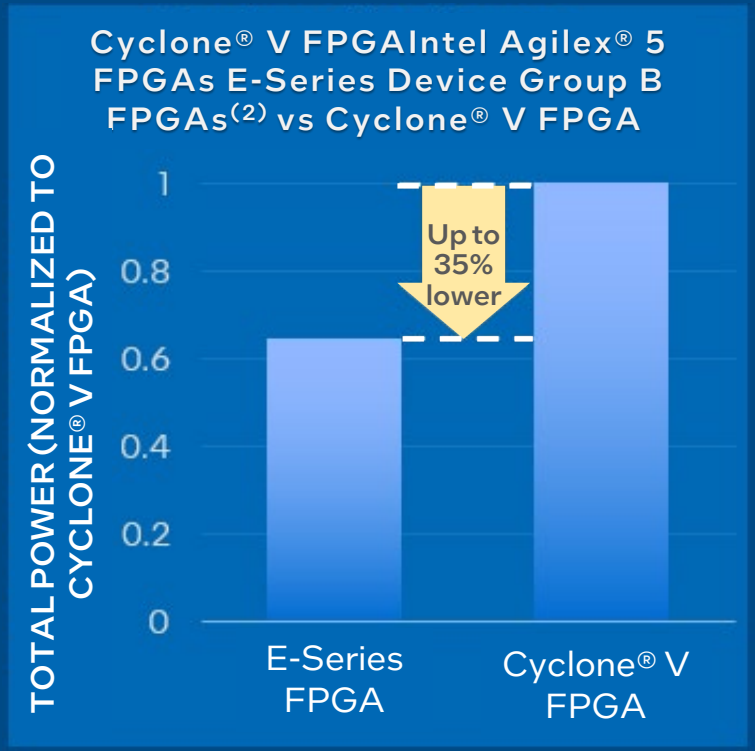


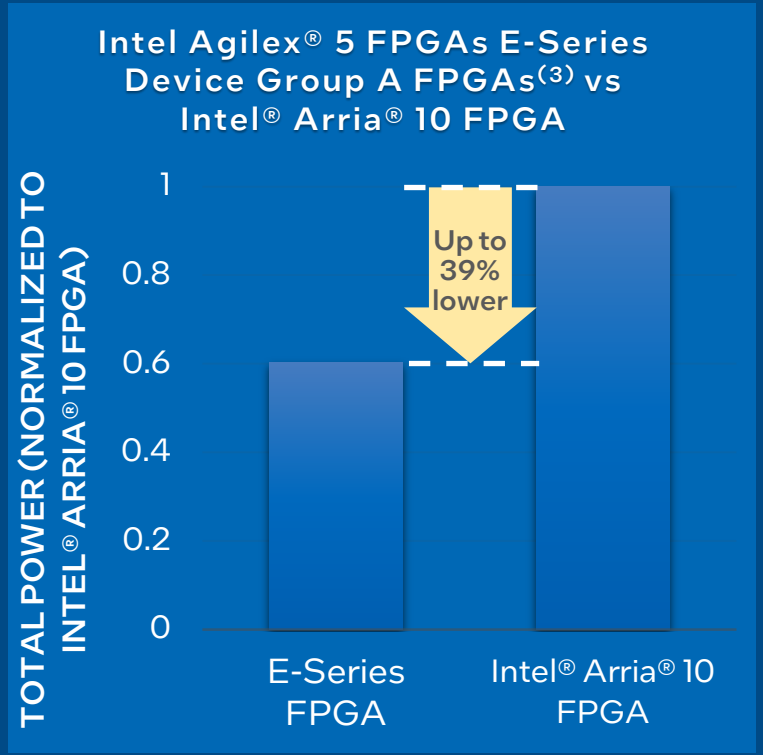


Notes:

1. Fabric performance comparison is done on mid speed grades for E-Series FPGA and Cyclone® V FPGA, while total power comparison is done on the equivalent speed performance for E-Series FPGA and Cyclone V FPGA.
2. Device Group A FPGAs is at 0.8 V when compared with Cyclone V FPGA.
3. Device Group B FPGAs is at 0.75 V, 100% fabric utilization, and 350 MHz when compared with Cyclone V FPGA.

Total Power Comparison[1]

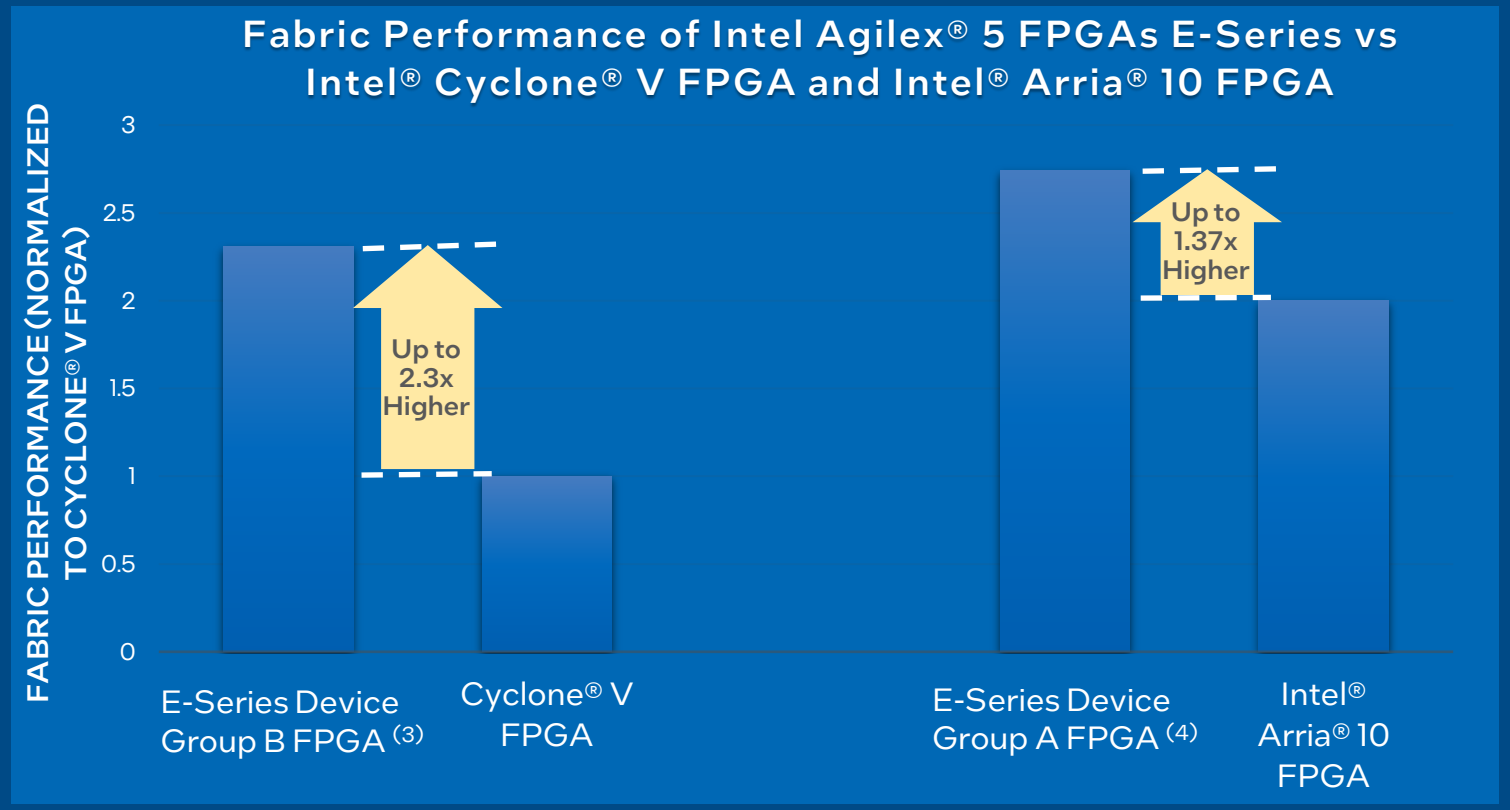




Notes:

1. Comparison is done on equivalent speed performance for E-Series FPGAs and previous generation FPGAs
2. E-Series FPGAs with 0.75 V when compared with Cyclone V FPGA, both at 80% fabric utilization and 150 MHz.
3. E-Series FPGAs with 0.85 V when compared with Intel® Arria® 10 FPGA, both at 80% fabric utilization and 300 MHz.

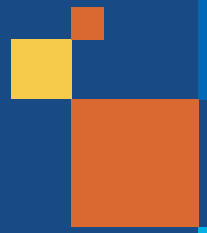
Fabric Performance Comparison(1,2)



Notes:

1. Comparison is done on mid speed grades for E-Series FPGAs and previous generation FPGAs
2. Comparison methodology is based on Intel® Quartus® Prime Software Quality of Result (QoR) Fmax
3. Intel Agilex® 5 FPGAs E-Series Device Group B FPGAs is at 0.8 V when compared with Cyclone® V FPGA
4. Intel Agilex® 5 FPGAs E-Series Device Group A FPGAs is at 0.8 V when compared with Intel® Arria® 10 FPGA.

I/O and Memory Support



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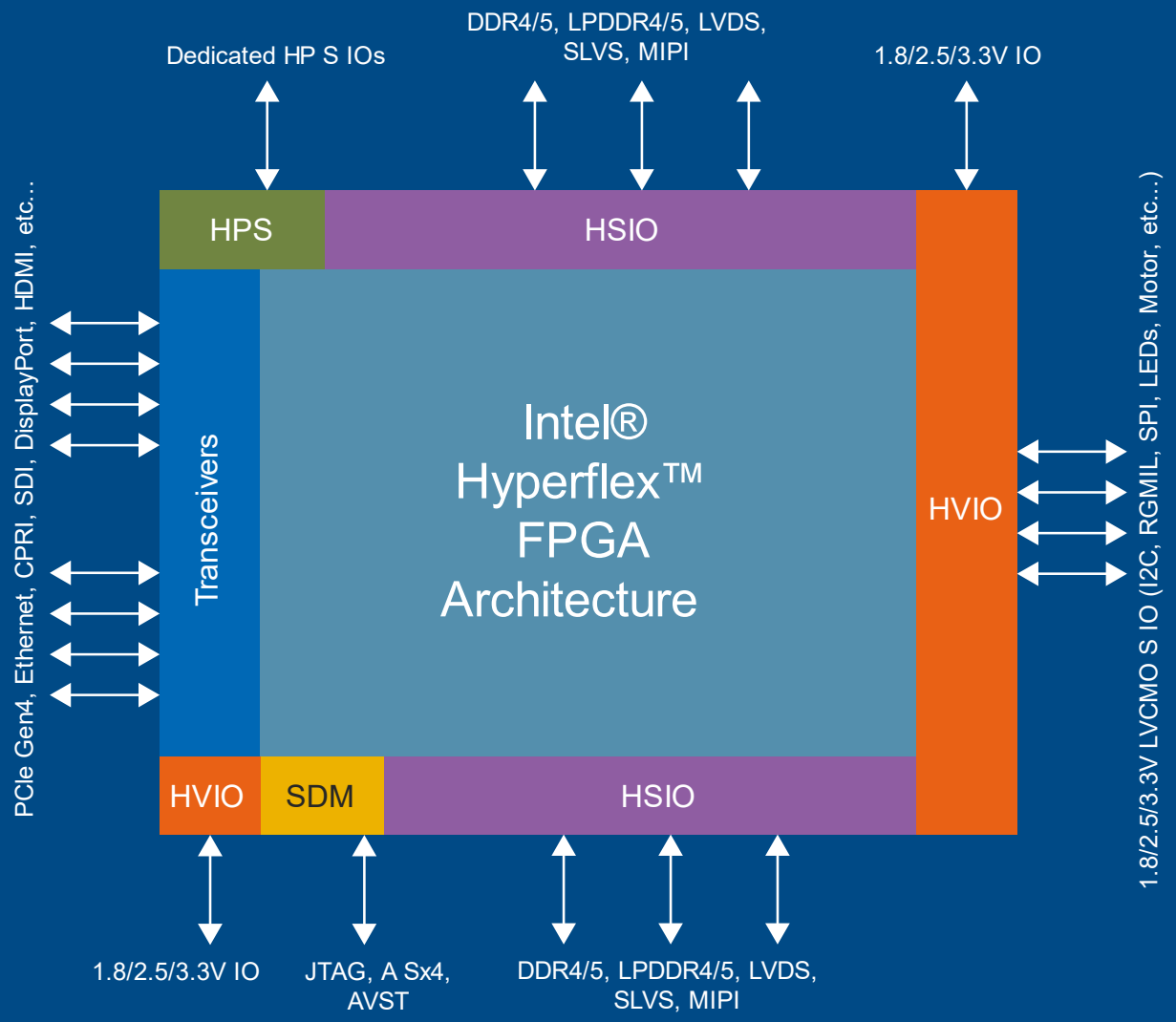
Intel Agilex® 5 FPGA I/O Support



I/O Support–Types of Banks

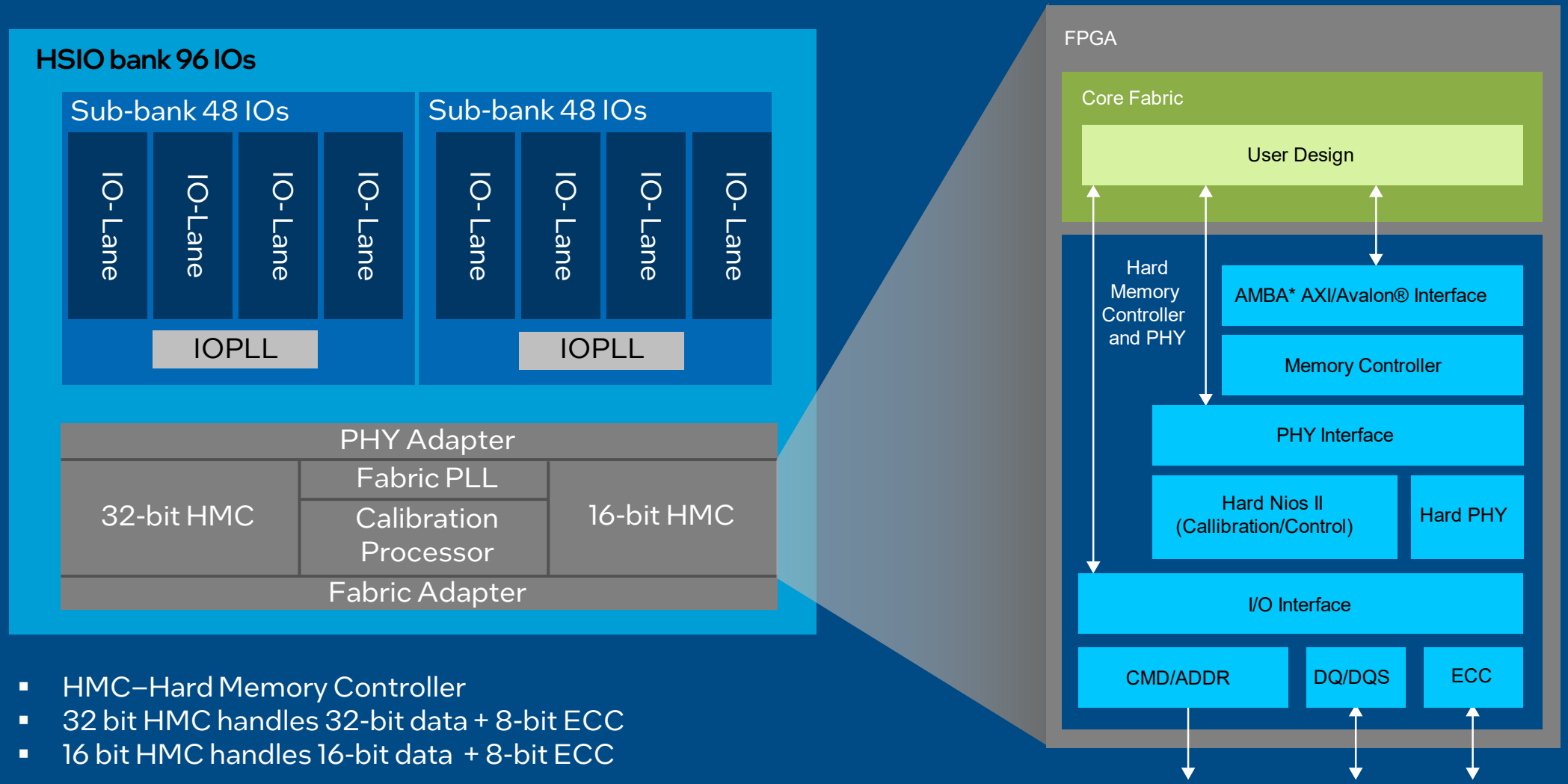
High-speed I/O (HSIO) (96/bank)	Specification	Comments
Low Voltage CMOS (LVCMOS)	1.05 V and 1.2 V single-ended	-
1.3 V LVDS	1.6 Gbps	Vicm: 0.5 to 1.375 V Vocm: 0.9 to 1.1 V
MIPI D-PHY 2.5	3.5 Gbps (HS/LP)	2D+C, 4D+C or 8D+C
SGMII (LVDS)	1.25 Gbps	Add AC coupling if required

High Voltage I/O (HVIO) (20/bank)	Specification	Comments
1.8 V single-ended LVCMOS	0.250 Gbps (125 MHz DDR)	RGMII supported at 1.8 V
2.5 V / 3.3 V single-ended LVCMOS	0.200 Gbps (100 MHz DDR)	

Intel Agilex® 5 GPIO Feature Comparison

Feature	Intel Agilex® 7 FPGA F-Series or I-Series GPIOs	Intel Agilex® 5 FPGAs E-Series GPIOs
Supply Rail Count	One supply rail	Two independent supply rails, one per I/O Bank
Phase-locked loop (PLL) Count	Two IOPLL + one CorePLL	Two IOPLL+ one CorePLL
Pseudo LVDS - Transmit and Receive I/O	TX only or RX only pins	TX and RX pins
LVDS – Max. Data Rate	1.6 Gbps	1.6 Gbps
LVDS Width	Up to 24 within an IO48	Up to 24 within an IO48
LVDS direction	NA	At compile time
MIPI D-PHY Data Rate	NA	3.5 Gb/s
MIPI D-PHY Configuration	NA	2D+C, 4D+C or 8D+C

Intel Agilex® 5 FPGA I/O Bank Overview



- HMC–Hard Memory Controller
- 32 bit HMC handles 32-bit data + 8-bit ECC
- 16 bit HMC handles 16-bit data + 8-bit ECC

Transceivers and Transceiver Protocol Support

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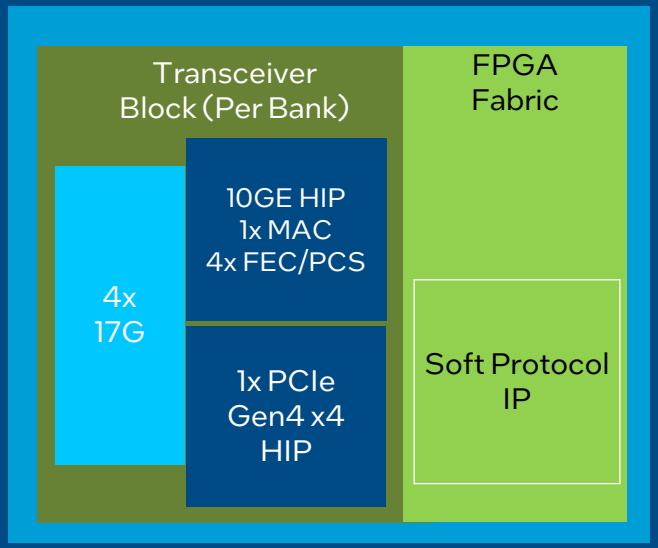
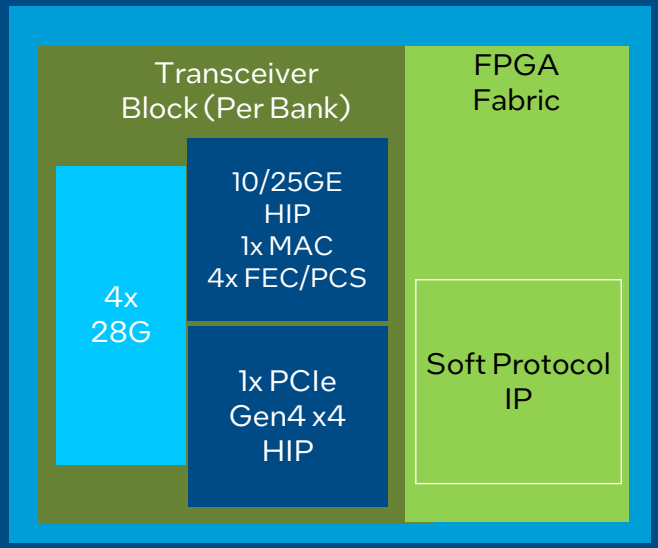
Intel Agilex® 5 Transceiver Features

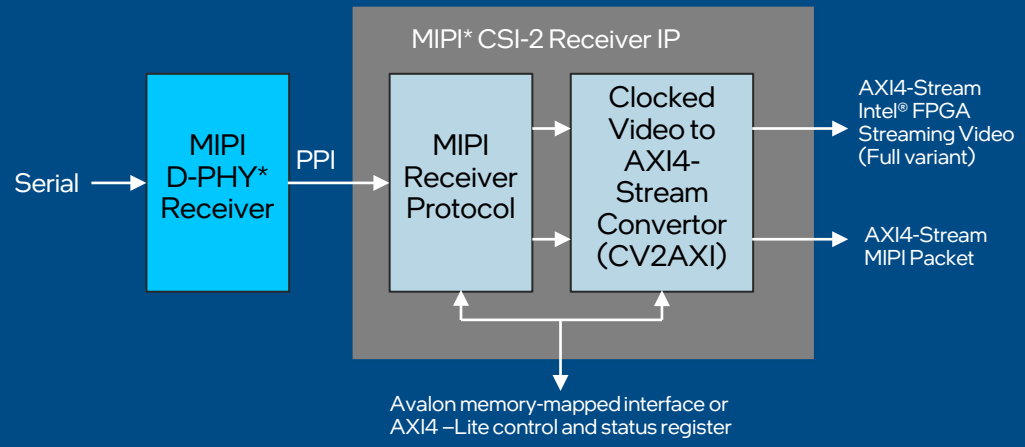


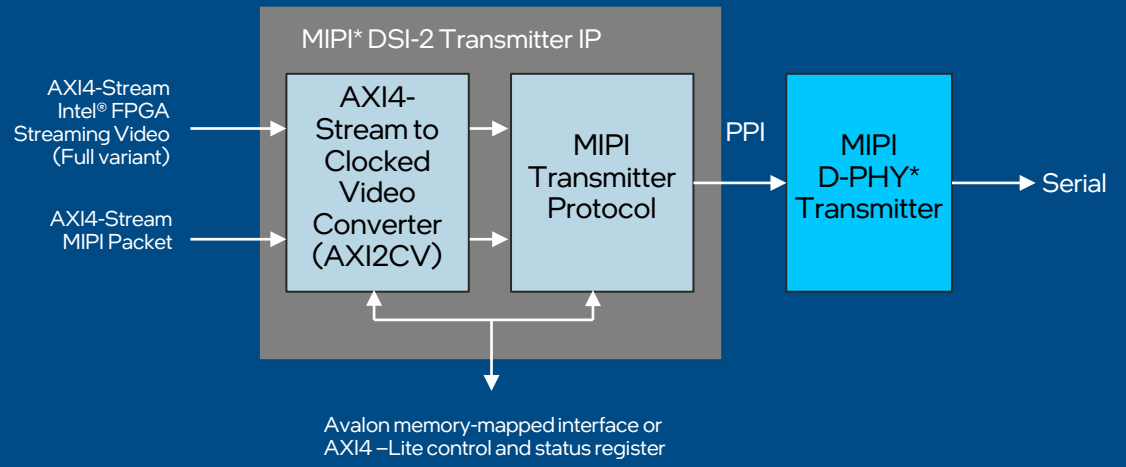


Intel Agilex® 5 FPGAs E-Series Device Group B FPGAs	Intel Agilex® 5 FPGAs E-Series Device Group A FPGAs
4 x 17G NRZ (Continuous 1- 17 Gbps)	4 x 28G NRZ (Continuous 1- 28 Gbps)
4x 10G Ethernet FEC Direct (IEEE 802.3 Clause 74 Firecode FEC HIP)	4x 10G/25G Ethernet FEC Direct (Clause 74 Firecode FEC and Clause 108 RS-FEC HIP)
4x 10G Ethernet PCS Direct (64b/66b HIP)	4x 10G/25G Ethernet PCS Direct (64b/66b HIP)
PCIe 4.0 x4 Controller HIP	PCIe 4.0 x4 Controller HIP
Independent Channels: Two reference inputs per quad and two fabric PLLs per quad	
Independent TX and RX to support combining simplex protocols	
4x PMA Direct (bypass Ethernet and PCIe HIP)	

Intel Agilex® 5 MIPI Support

Protocol	Device Group A	Device Group B
CSI-2	▪ CSI-2 version 3, up to eight lanes ▪ D-PHY v2.5 at up to 3.5 Gbps	▪ CSI-2 version 3, up to eight lanes ▪ D-PHY v2.5 at up to 2.5 Gbps
DSI-2	▪ DSI-2 version 2, up to four lanes ▪ D-PHY v2.5 at up to 3.5 Gbps	▪ DSI-2 version 2, up to four lanes ▪ D-PHY v2.5 at up to 2.5 Gbps





Intel Agilex® 5 JESD204B/C and Serial Lite IV Overview

IP Protocol	Performance		SIP/HIP*
	Intel Agilex® 5 FPGAs E-Series Device Group B FPGAs	Intel Agilex® 5 FPGAs E-Series Device Group A FPGAs	
JESD204B	2-8x Up to 16G	2-8x Up to 19.2G	SIP
JESD204C	2-8x Up to 16G	2-8x Up to 28G	SIP
Serial Lite IV	1-8 x Up to 16G	1-8 x Up to 28G	SIP: MAC
			HIP: PCS, FEC

*SIP: Soft IP, HIP: Hard IP

Intel Agilex® 5 Ethernet Hard IP/Soft IP Support

Intel Agilex® 5 FPGAs E-Series Device Group B FPGAs	Intel Agilex® 5 FPGAs E-Series Device Group A FPGAs
10G Ethernet HIP (Up to 6 MAC instances)	10/25G Ethernet HIP (Up to 6 MAC instances)
• MAC, PCS, and IEEE 802.3 Clause 74 Firecode FEC, CR/KR • SyncE and IEEE 1588	• MAC, PCS, and Clause 74 Firecode FEC and Clause 108 RS-FEC, CR/KR • SyncE and IEEE 1588

IP Protocol	Performance		SIP/ HIP*
	Intel Agilex® 5 FPGAs E-Series Device Group B FPGAs	Intel Agilex® 5 FPGAs E-Series Device Group A FPGAs	
Ethernet MAC, PCS	1-24 x 10M/100M/1G, 1-N x 10M/100M/1G/2.5G/10G		SIP
Interlaken	2-8 x Up to 12.5G	2-8 x Up to 25.78G	SIP

*SIP: Soft IP, HIP: Hard IP

Intel Agilex® 5 PCI Express Support

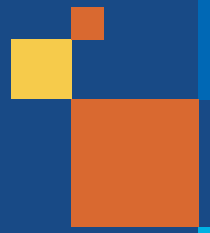
- Available as integrated hard IP (HIP) on all family variants
- Planned companion soft IPs
  - Multichannel DMA:

    For direct data transfers between FPGA-device and host memory for multiple host clients simultaneously
  - Switch IP:

    Increase fanout of the Host PCIe connection by using FPGA-based PCIe HIPs as down ports

Device Family	PCIe IP Configuration	Bandwidth / IP	HIPs/device	Network Capacity	Remarks
Intel Agilex® 5 FPGAs E-Series Device Group B FPGAs	4.0 x4	64 Gbps	Up to 6	50GE	Double PCIe bandwidth / ports compared to Intel® Cyclone® V FPGA
Intel Agilex® 5 FPGAs E-Series Device Group A FPGAs	4.0 x4	64 Gbps	Up to 6	50GE	Double PCIe bandwidth / ports compared to Intel® Cyclone®10 FPGA/ Intel® Arria® 10 FPGA

Hard Processor System (HPS), Peripherals, and Embedded Software



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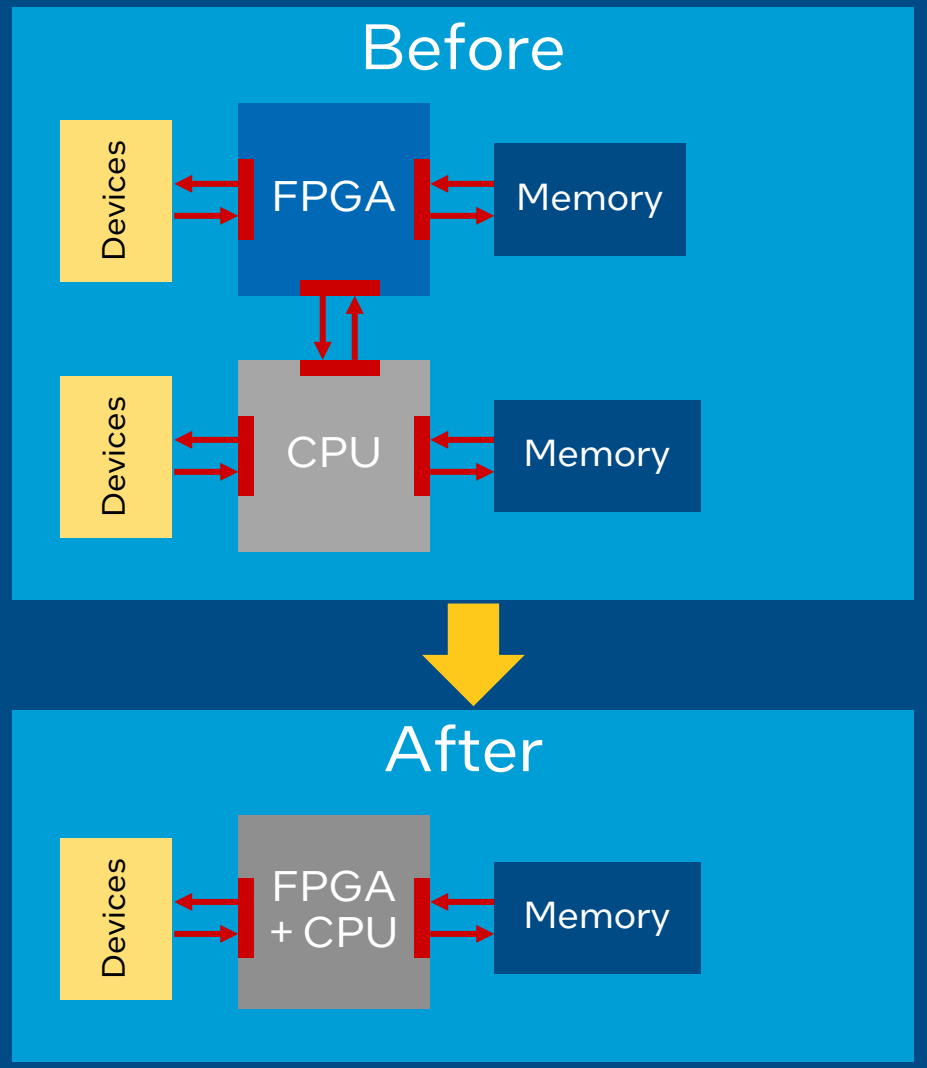
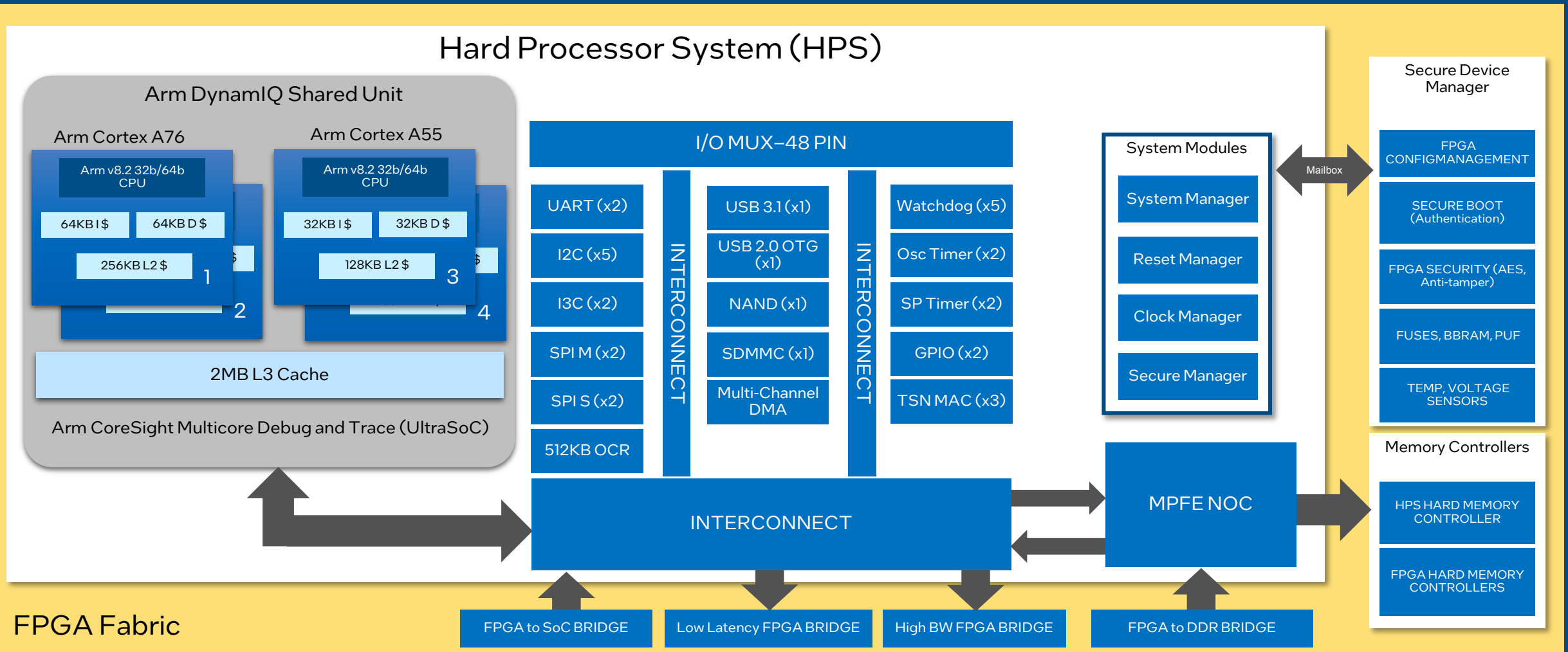
SoC FPGA–Benefits of Integration

- Increased system performance
- Reduced power consumption
- Reduced board size
- Reduced system cost



Hard Processor System



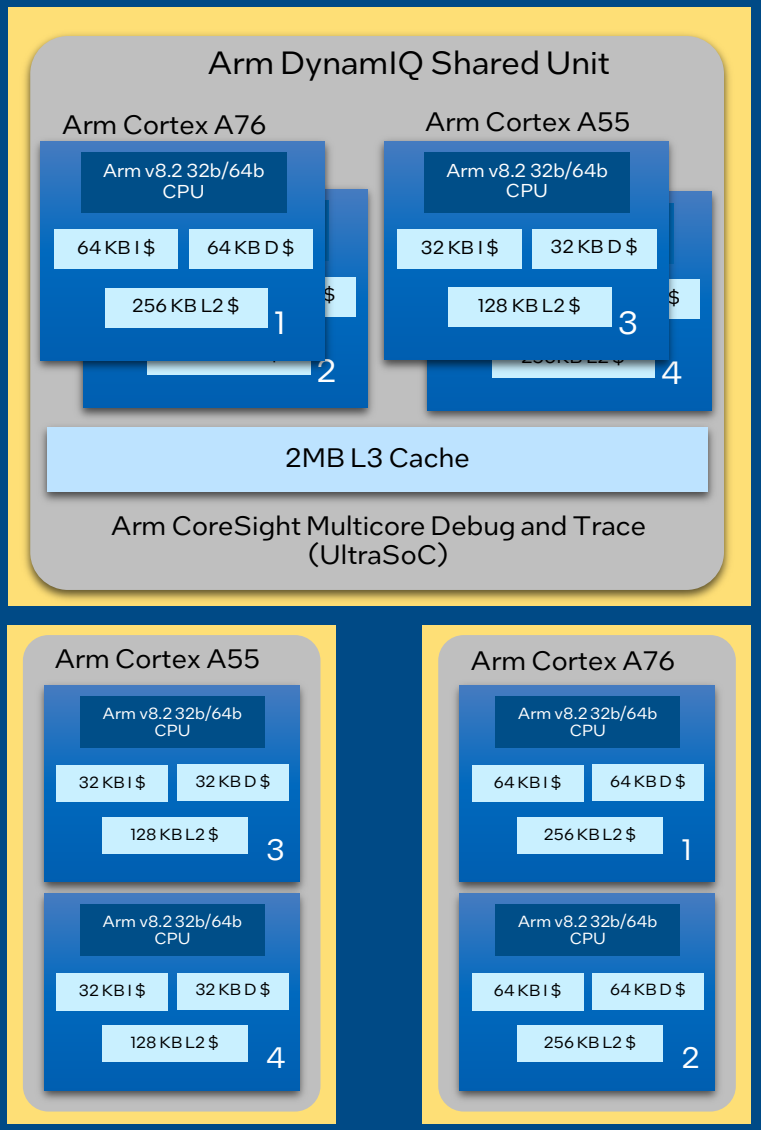
High-Speed Transceivers PHY, PCS, Device I/O, Hard PCIe 4.0

Scalable Performance and Power

Isolated power allows unused cores to be powered down.

Configurable operating frequencies to meet target performance:

- 2xA55 @ 1,500 MHz + 2xA76 @ 1,800 MHz
- 2xA55 @ 800 MHz + 2xA76 @ 400 MHz
- 2xA55 @ 1,500 MHz
- 1xA76 @ 1,800 MHz



Upgraded Microprocessor Unit (MPU)

Dual Arm Cortex-A76 Processor

- Targeted for up to 2 GHz operation
- 64 K L1 I-cache and 64 K L1 D-cache per core
- 256 K shared L2-cache per core

Dual Arm Cortex-A55 Processor

- Targeted for up to 1.5 GHz operation
- 32 K L1 I-cache and 32 K L1 D-cache per core
- 128 K shared L2-cache per core

Arm DynamIQ Shared Unit (DSU)

- Snoop Control Unit (SCU) for full coherency among cores
- CoreSight debug and trace
- One CHI-B memory interface port
- Peripheral port for lower latency access to PSS
- 2MB L3 cache

Upgraded Application Processor Subsystem

Arteris NCore3 Cache Coherent Unit

- Manages I/O coherency with fabric accesses to SDRAM
- 2X 32 KB system level cache (SLC)
- Used to support atomic CHI commands
- ACE5-lite port from fabric and CHI.B port to DSU supports direct allocation from fabric into L1, L2, and L3 caches using new command types

Arm Cortex GIC-600 for interrupt support

- Supports GIC V3 architecture
- ACE-lite host port to support Interrupt Translation Service (ITS)
- ACE-lite agent port for access to the entire register map

Arm Cortex MMU-600 for system MMU support

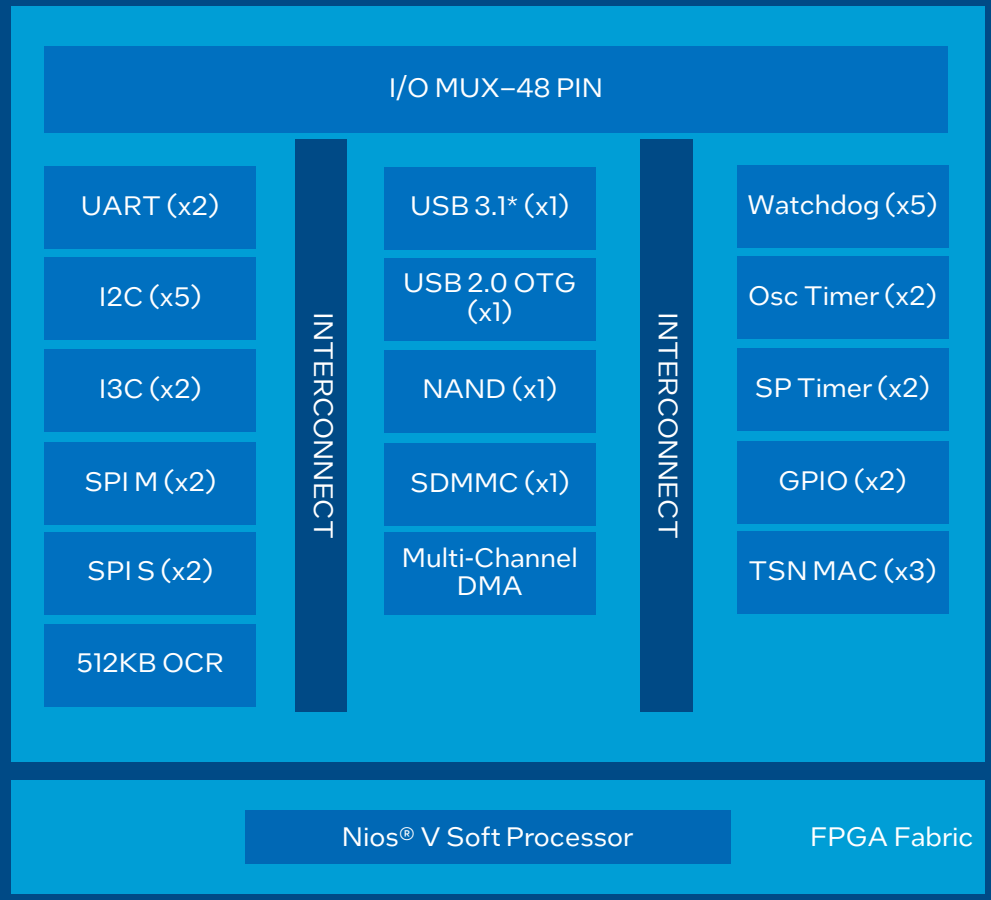
- Supports SMMU architecture V3.1
- Two-stage translation process to support multiple virtual machines
- ACE-lite host port for page table walks and distributed virtual memory

APB agent interface for register accesses

- 512 KB of on-chip RAM (OCRAM)
- A mini-FlexNoc has been added between the NCore3 and OCRAM to support the exclusive monitors and firewalls previously implemented in NCore2.

Upgraded Peripheral Subsystem

- Improved SDMMC, NAND
- Multi-channel DMA controller
- USB 3.1* / USB 2.0 OTG
- I3C / I2C: Current and future connectivity
- TSN MAC: 1GbE to 2.5 Gb* with TSN endpoint support
- Nios® V processor, RISC-V based, soft processor



* Feature available in transceiver enabled devices only

Embedded Software Leadership

Bootloaders

- Up streamed and latest U-Boot, Arm Trusted Firmware, UEFI

Operating System Support

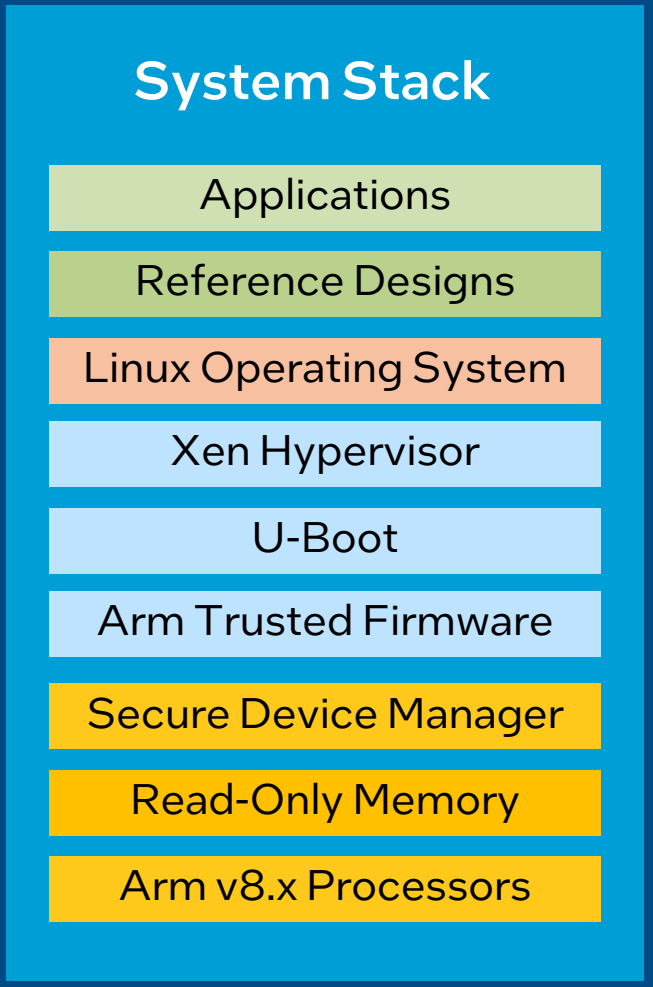
- Hard Processor Subsystem: Latest Linux Mainline & LTS kernels & Zephyr
- Hard Processor Subsystem: VxWorks, QNX
- Soft Core (NiosV): bare metal, uCOS/II, Zephyr, FreeRTOS

Xen Hypervisor

Yocto Project Build tool

Debuggers

- Continued support for Arm* Development Studio for Intel® SoC FPGA
- New RiscFree, a heterogeneous debugger for soft and hard processors



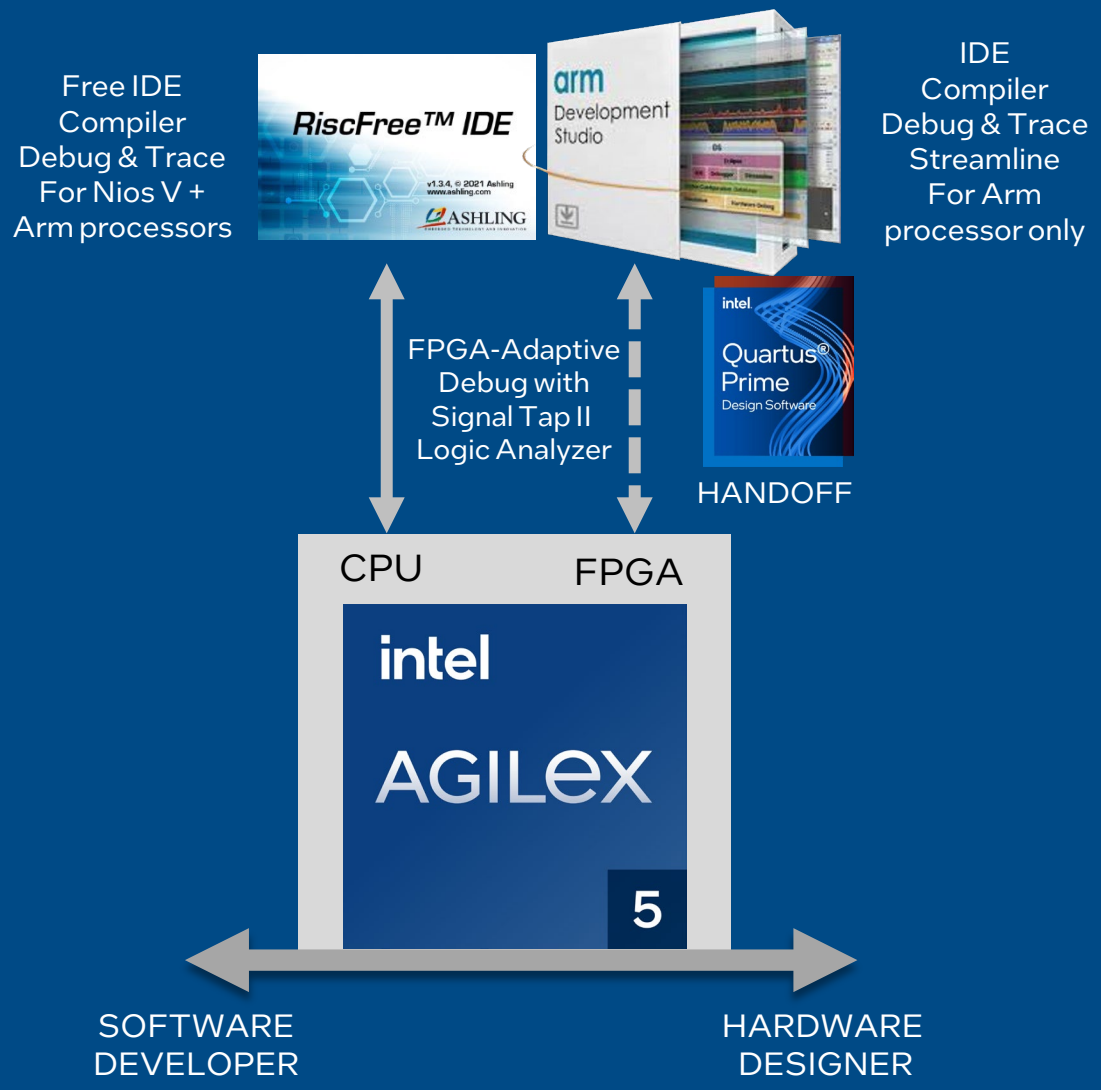
IDE for Intel Agilex® 5 FPGAs E-Series

RiscFree* IDE for Intel® FPGAs

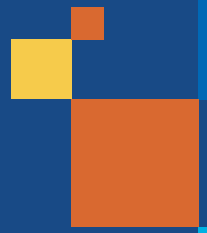
- Compiler, Debug, and Trace for Nios® V and Arm processors
- Heterogeneous debug on Nios V and Arm processors
- Free IDE

Arm* Development Studio for Intel® SoC FPGA

- Continue enabling premium Arm* Development Studio for Intel® SoC FPGA tools
- Arm industry standard
- Single vendor version



Intel Agilex® 5 FPGA Package Design



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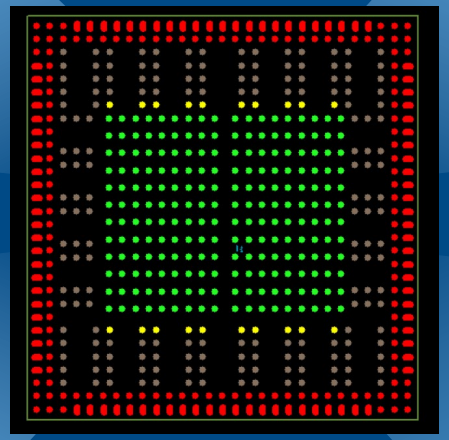
Intel Agilex® 5 FPGA New Packages

Reduce Design Complexity

Reduce Board Size/Space



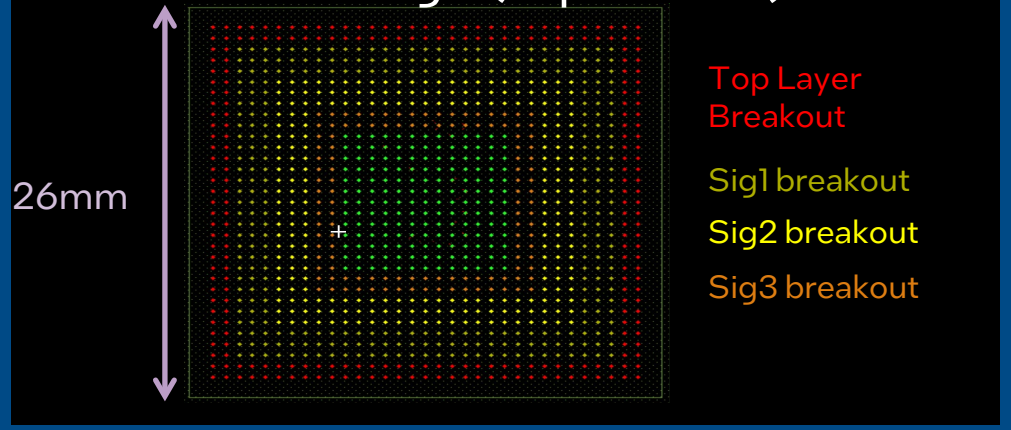
Reduce Board Development Time

Reduce Board Cost

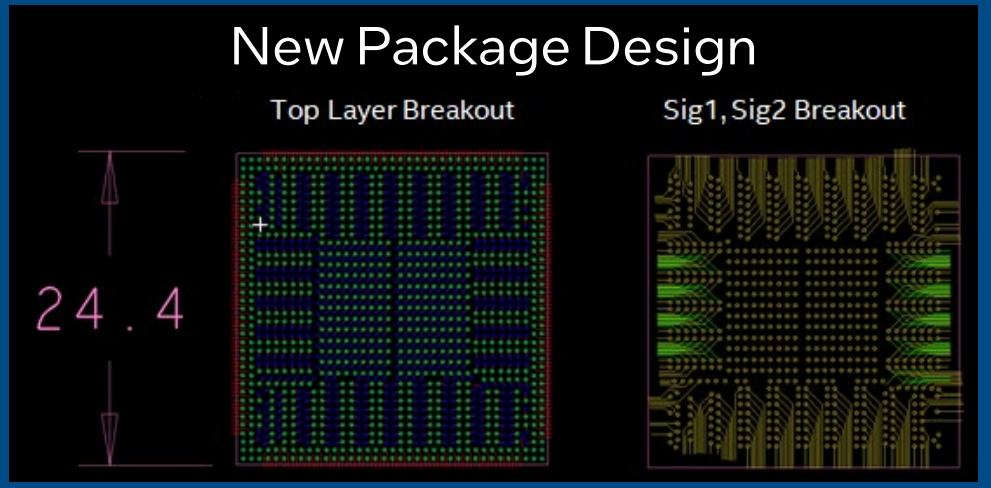
Intel Agilex® 5 FPGA
New Variable Pitch BGA Packaging

Enables smaller form factors than standard BGA with the same I/O count and design rules

BGA Package (equivalent)

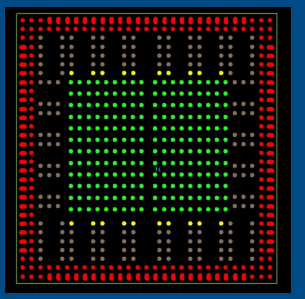


New Package Design



	Standard BGA	Variable Pitch BGA
Pad type	Circular	Circular
Ball pitch	0.8 mm grid	Min 0.65 mm Variable Pitch BGA
Total pins	961	961
Routable I/O	702	702
Package FF	26 mm x 26 mm	~24.4 mm x 24.4 mm
I/O Route Layer	4L	3L
PCB layers	8L	6L

New Variable Pitch BGA Packaging Layout

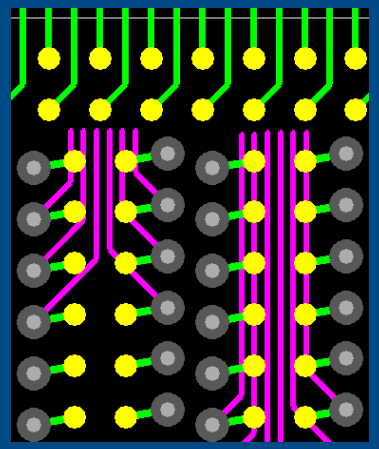


- Variable pitch ball grid pattern:

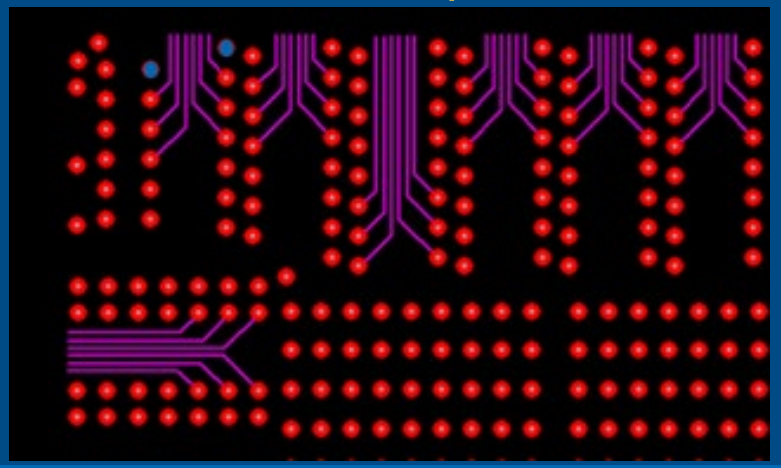
Ease the trace routing → Reduce design complexity → Reduce PCB layer count, board thickness → Reduce board cost and development time

Example of board routing

Top layer



Inner layer



Intel Agilex® 5 FPGA Collateral

Fully access to technical information on next generation FPGAs.

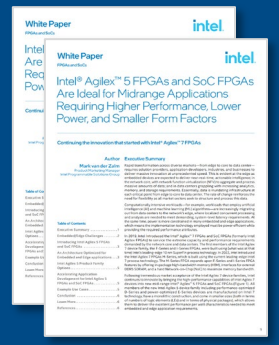
8 Product Information Docs

- Datasheet
- Device Overview
- Product Tables
- Advance Information Brief

18 Architecture & Technology Briefs

- High-Speed Serial Interface (HSSI)
- General Purpose I/Os
- Delivering Power-efficient Performance for Edge applications
- Time-Sensitive Networks

4 White Papers



- Ideal for Midrange Applications

2 Case Studies

- 4K Camera Design
- Drive-on-Chip

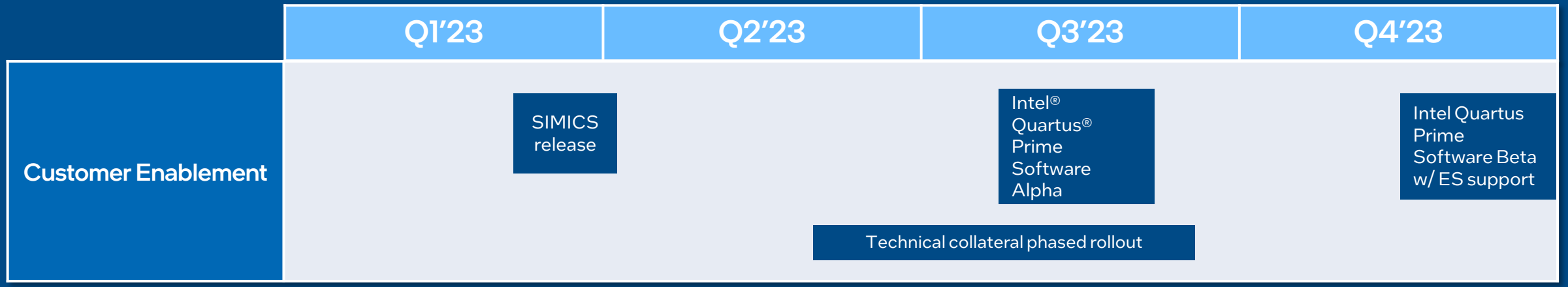
5 Application Briefs & Brochures

- Video and Vision
- Test & Measurement
- Industrial
- Military
- Medical

15 Development User Guides

- HPS
- Simics
- Configuration
- Transceiver
- Power Management
- I/O
- LVDS
- CvP

2023 Intel Agilex® 5 FPGA Customer Enablement
(Software/Docs)



Software Status

Software Milestone	Quarter	Field deployed
SIMICS	Q2	Limited to Alpha (22)
Alpha customer	Q3	Alpha (22)
Beta customers	Q4	Beta (150+)
General Release	Q1'24	All

Technical Collateral

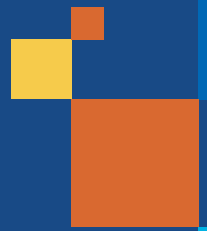
Phased rollout of technical collateral

Bundle 0 and 1
- Information documents, AIP documents

Bundle 2a and 2b
- Key enablement for EAP customers
- PTC, Initial UGs, design guides

Bundle 3
- Broad information and enablement for all customers
- GSRD/GHRD
- Development Kit User Guide

Advanced Security Features



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Advanced Security Features

Confidentiality, Integrity, Availability

Encryption, Authentication, Attestation, Secure Boot, User Access to Crypto Functions, Secure Debug

Key Protection

Side Channel Mitigation, Physical Anti-Tamper Detection and Response

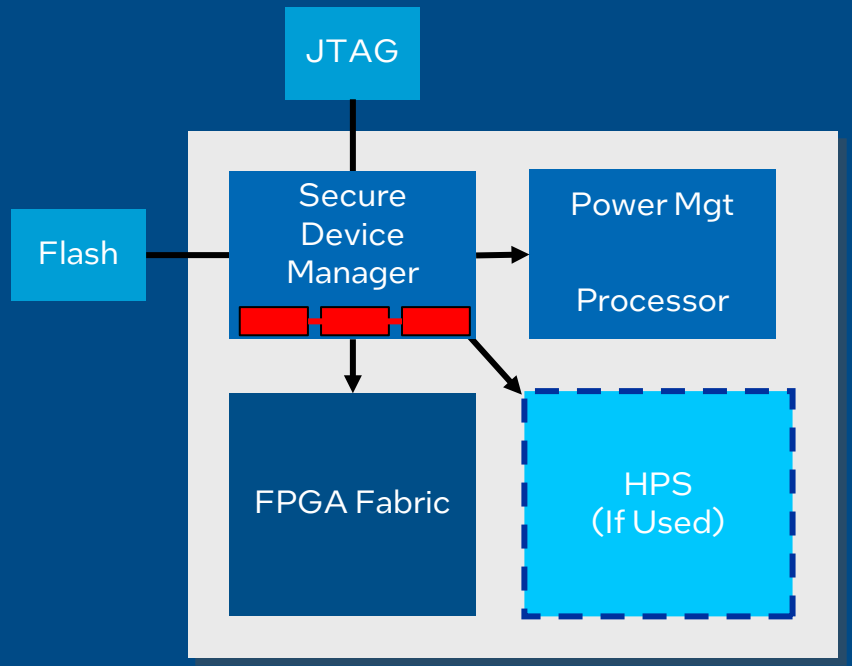
Secure Manufacturing

Black Key Provisioning

Secure RMA

Secure Device Manager (SDM) Highlights

- Built-in error correction code (ECC) memory
- Operations priority over fabric and other uPs
- Manages tamper sensors, and scripted device erasure
- Manages boot process, encryption, authentication, and all keys
- Secure boot support:
- Private key root of trust on FPGA
- Public key only on FPGA (external Root of Trust)
- Physically unclonable function (PUF)-based keys



Dedicated Secure Device Manager and Firmware

Confidentiality and Integrity

Encryption

- Multiple root keys
- AES-GCM 256, BBRAM, eFUSE, intrinsic ID PUF

Authentication

- Secure Hash Algorithm 2 (SHA-2) 256/384/512 NIST, ECDSA 256/384 NIST & Brainpool

Vendor Authorized Boot

- U-Boot authenticated boot with Crypto
- Linux/application authentication using Crypto
- FW attestation

Secure Debug

- Debug certificates for HPS debug
- Active until FPGA power cycle, or canceled

Bitstream and Platform Attestation

- SPDM 1.2

User access to hard crypto blocks

- FIPS 140-3 L2 certifiable

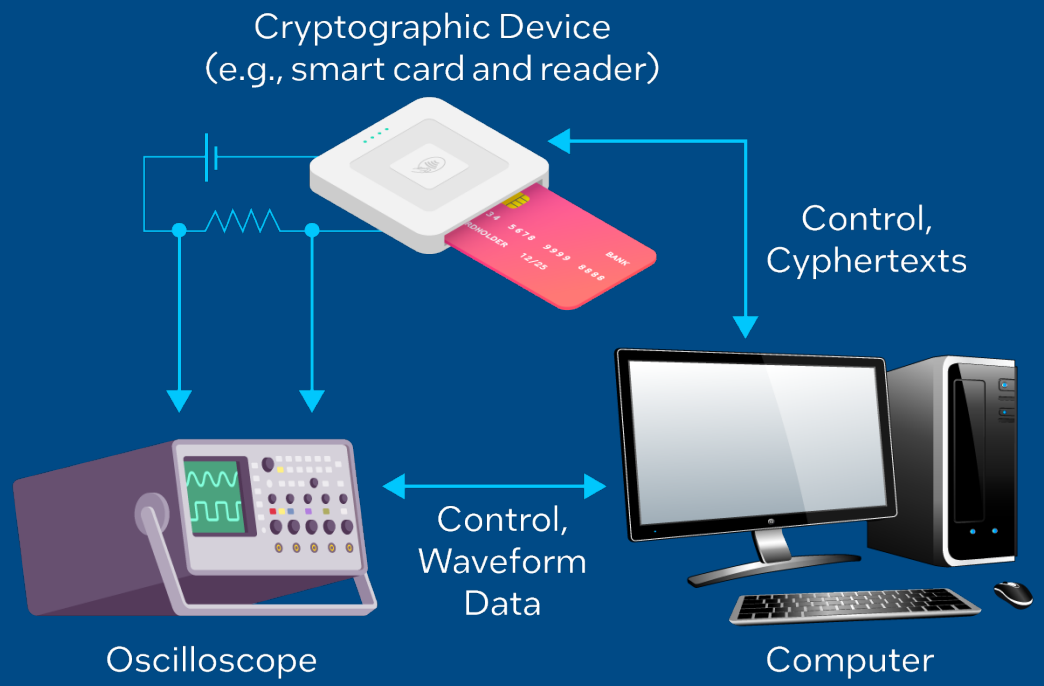
Availability and Key Protection

Side Channel Mitigation

- Key rotation
- Key protection
- Configuration data protection
- Increased resistance to side channel attacks in hardware block

Physical Anti-Tamper Detection and Response

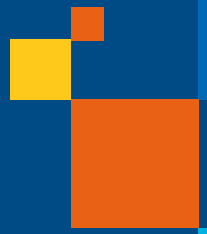
- Voltage, temperature, and clock attack
- Full-chip cleaning
- Full-chip zeroization
- BBRAM cleaning
- Kill eFuse



Secure Manufacturing

- Black Key Provisioning
  - Secure Communications Channel for Provisioning Root Key at Manufacturer
    - Manufacturer can program FPGA, but does not see encryption key
    - Prevents contract manufacturer from being able to “overbuild” the customer’s product
  - eFuse based black key provisioning
  - PUF based black key provisioning
  - 128-bit or greater security
- Secure Returned Merchandise Authorization (RMA)
  - Ability to return secure devices to Intel for debug

Intel Agilex® 5 FPGA Development Kits



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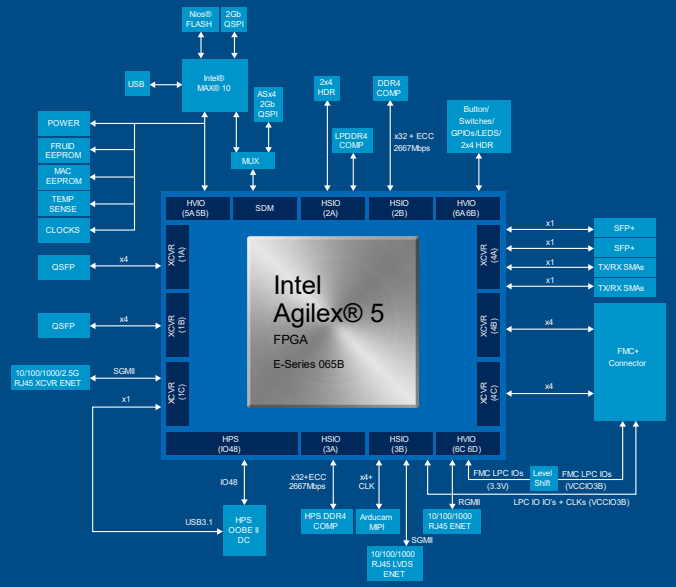
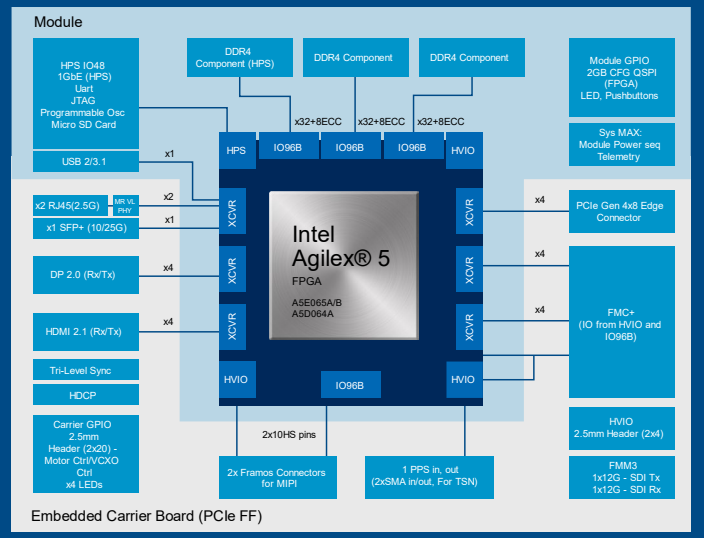
Intel Agilex® 5 FPGA Development Kits

Premium Development Kit



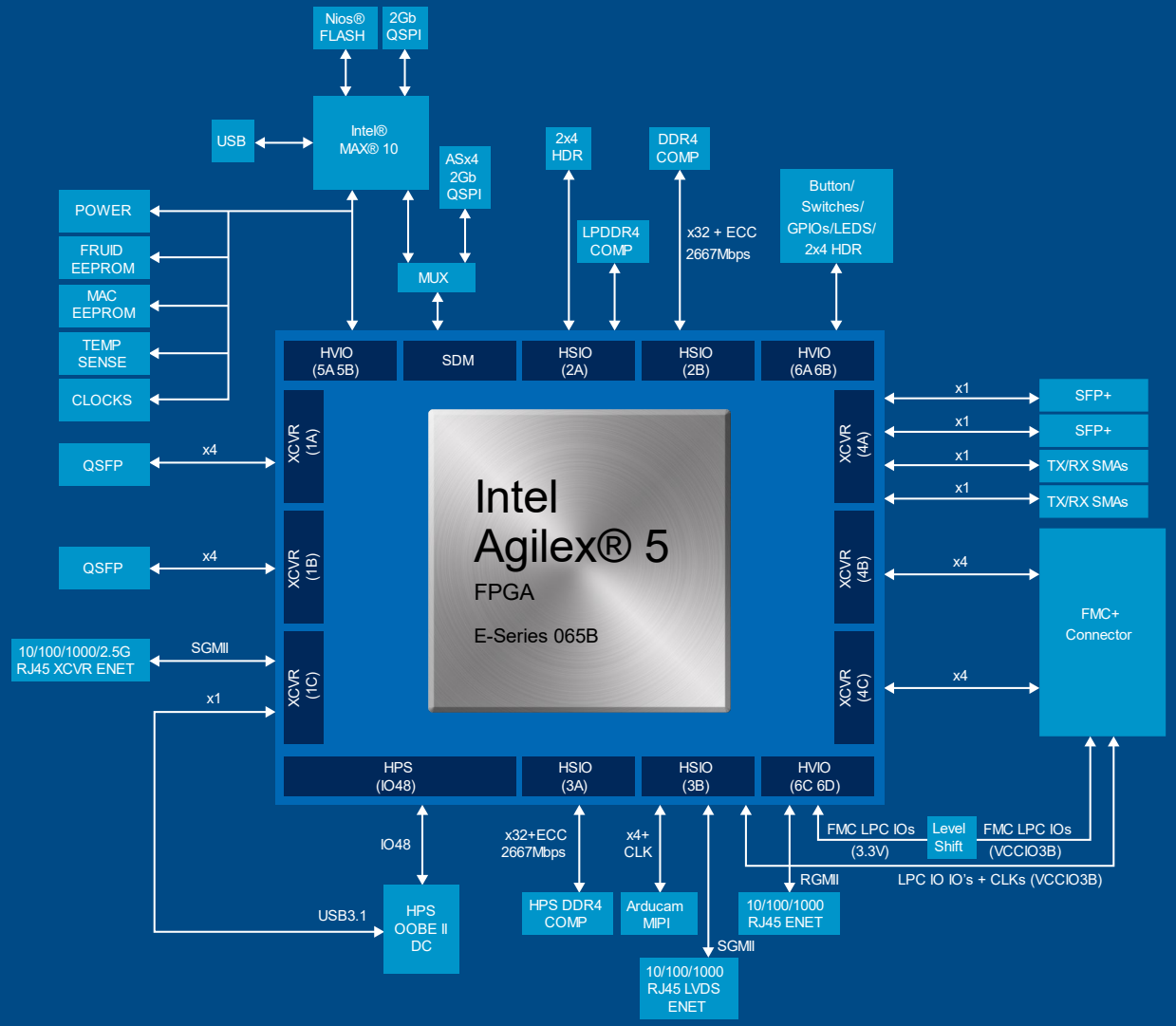
- Primary Use:
  - Performance and features evaluation and analysis

Modular Development Kit



- Primary Use:
  - Segment specific application development and proof of concept verification

Premium Development Kit Block Diagram



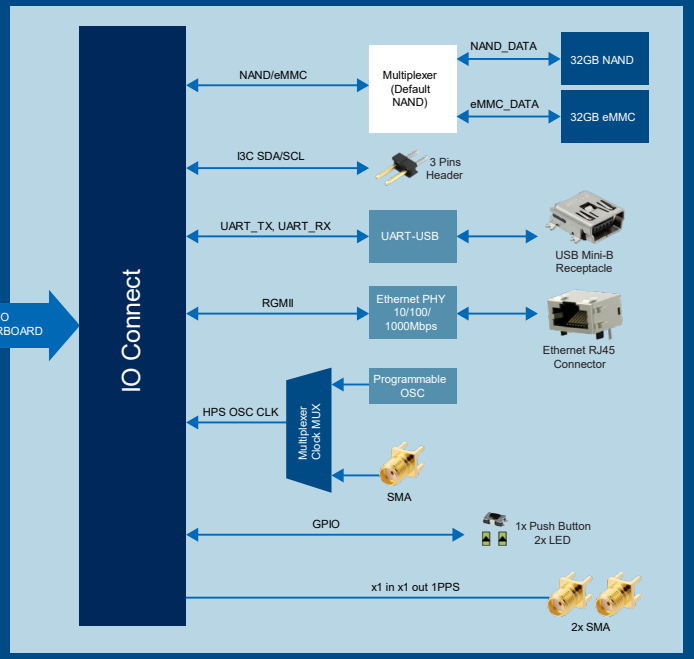
Not for production use

HPS Expansion Boards Features

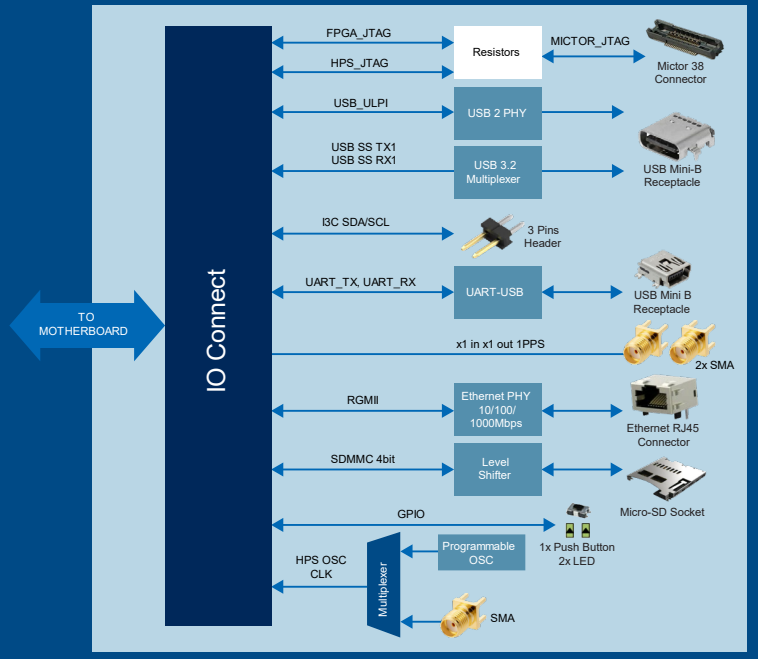
- Demonstrate new features of the Intel Agilex® 5 FPGA HPS
  - I3C
  - 1588 TSN
  - NV-DDR (NAND)
  - USB 3.1
- Provide platforms for different HPS peripheral configurations
  - HPS Enablement Expansion Board
  - HPS NAND Board
  - HPS Test Board
- Usability improvements
  - New Programmable Oscillator
  - Larger I/O Connector
  - UX changes like connector types and orientation
  - New remote debug features
    - Remote power cycle
    - Remote push buttons
- Scope of Expansion boards
  - Used with Intel Premium Development Kits
  - Not backwards compatible with previous generations of development kits

HPS Expansion Board Layouts

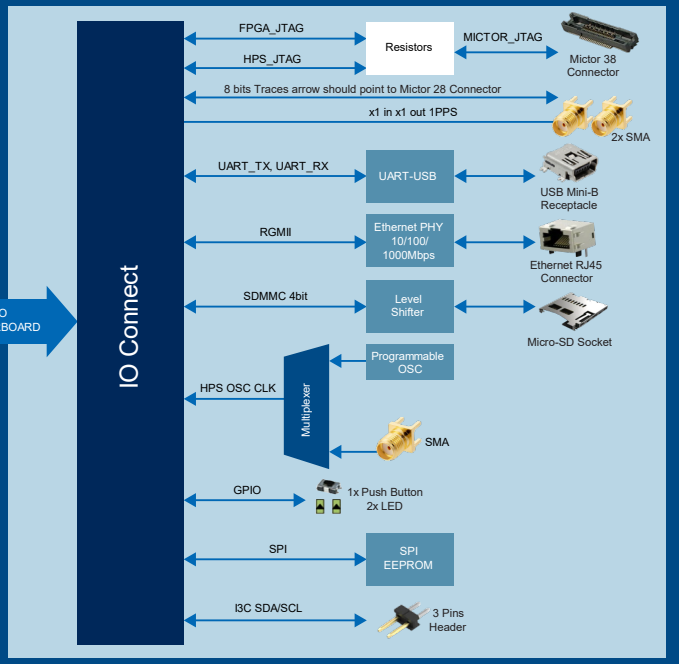
Nand Board



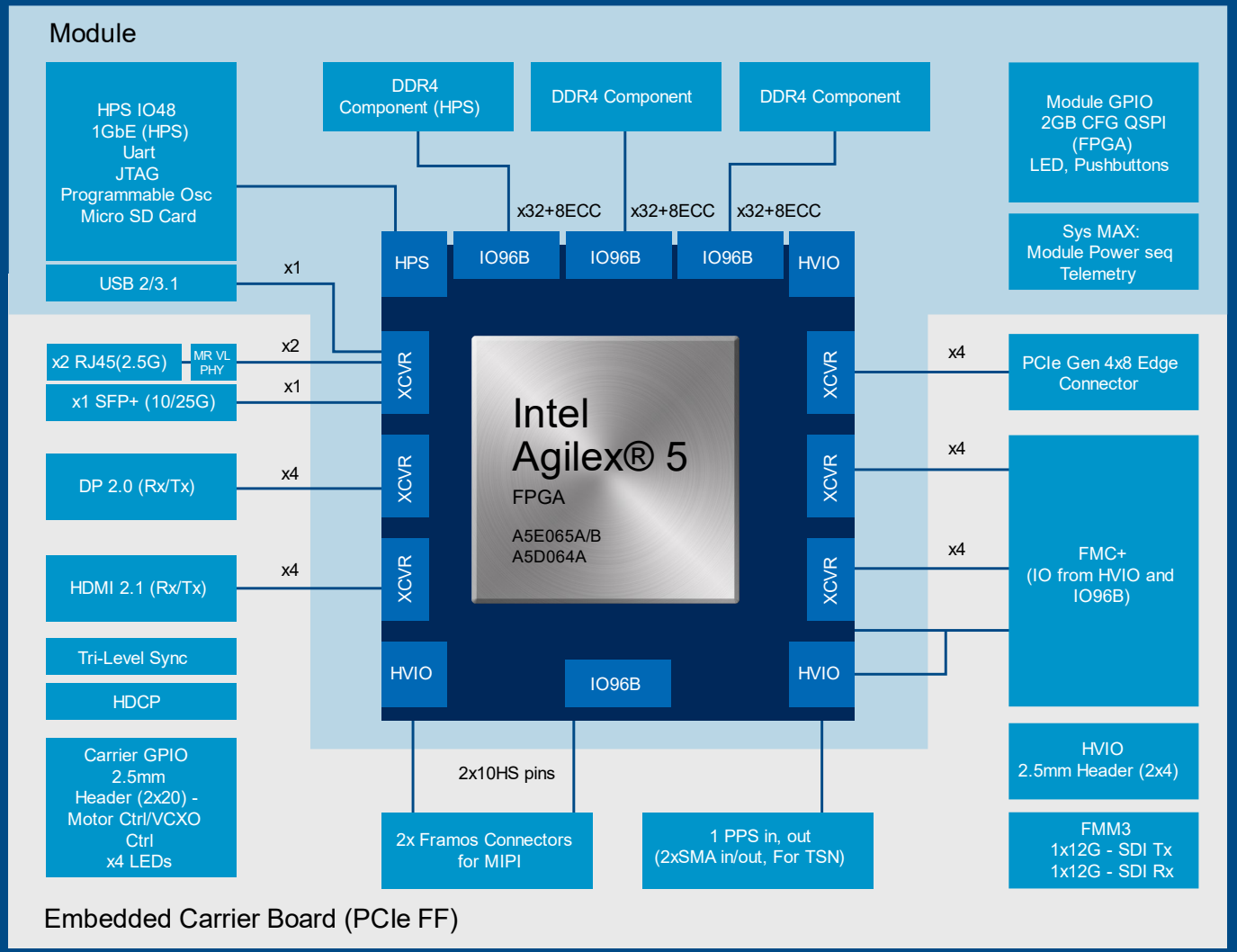
I/O Expansion Board



I/O Test Board



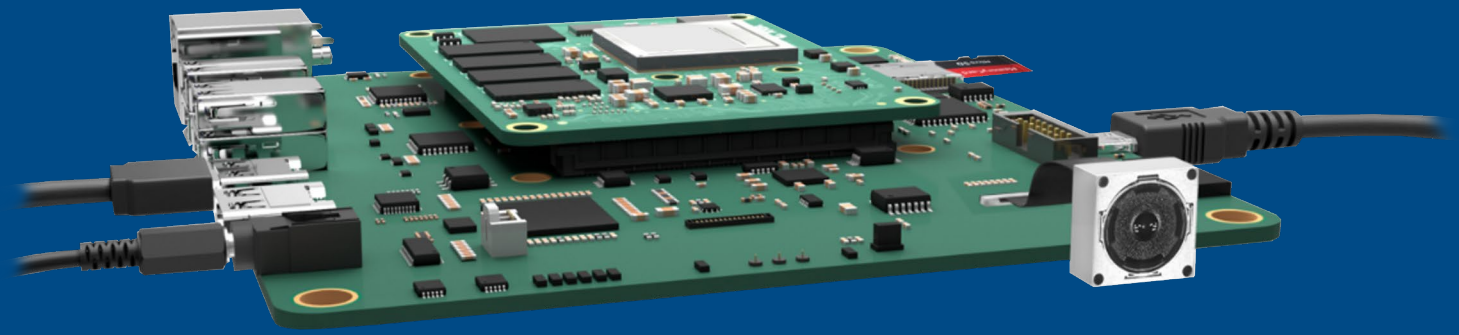
Modular Development Kit Block Diagram



Not for production use

Modular Development Kit Benefits

- Enables Reuse
- Flexible
- Lower TCO
- Supply chain / Ecosystem
- Targeted reference designs
- Module functions without the Carrier



Intel Agilex® 5 FPGA System On Module

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Intel Agilex® 5 System On Modules (SoM) Offerings

Intel will leverage its partners for SoM solutions

- Nine key partners are part of our Early Access program for ES Silicon
- Intel has Identified a list of critical market segment solutions and we are making sure each of them are covered by our partners

Q3-23

- List of Intel Agilex 5 FPGA SoM partners
- High-level overview of each providers SoMs
- List of target application solutions

Q4-23

- Detailed information on each SoM (FPGA size, interfaces supported etc.)
- Detailed overview of application solutions

2024

- Availability of Intel Agilex 5 FPGA-based production SoMs

Intel® Quartus® Prime Pro Edition Software

intel®

Best-in-Class Developer Experience

Focus on what matters with an enhanced platform and IP automation

Lower TCO

- One speed grade advantage
- Fit into a lower-cost device

Faster TTM

- Intel® Quartus® Prime Software v23.1
- oneAPI Toolkit for IP centric flows
- Intel ® FPGA AI Suite and OpenVINO™ Toolkit

Fits Your Design Flow

- Nios® V/g processor and RISC-V ecosystem
- Open source support

Intel® Quartus® Prime Software

Power and Performance

- Delivering performance for Intel Agilex® devices
- Compile innovations in each release
- Less than 32 GB of memory consumption (Agilex 5®)
- ECO compiles Simulation Aware Signal Tap for faster debug turnaround time
- Back-Annotation and Fast Preservation Compile to reduce compile time

Ease of Use

- Design Assistant for design rule checking
- Snapshot viewer allows cross-probing during analysis
- Platform Designer for IP-based design
- Remote debug over Ethernet and PCI Express

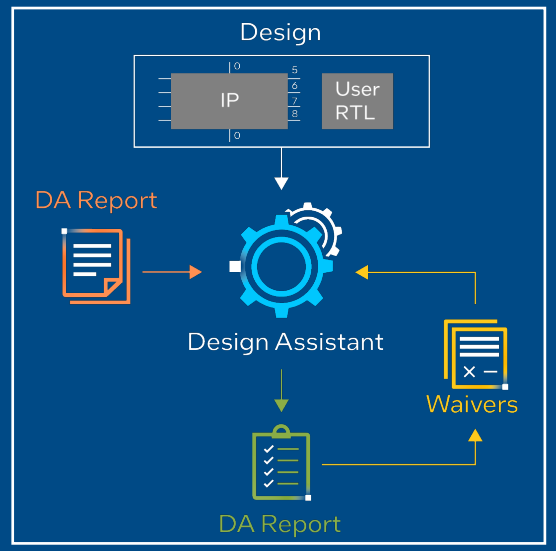
Partners

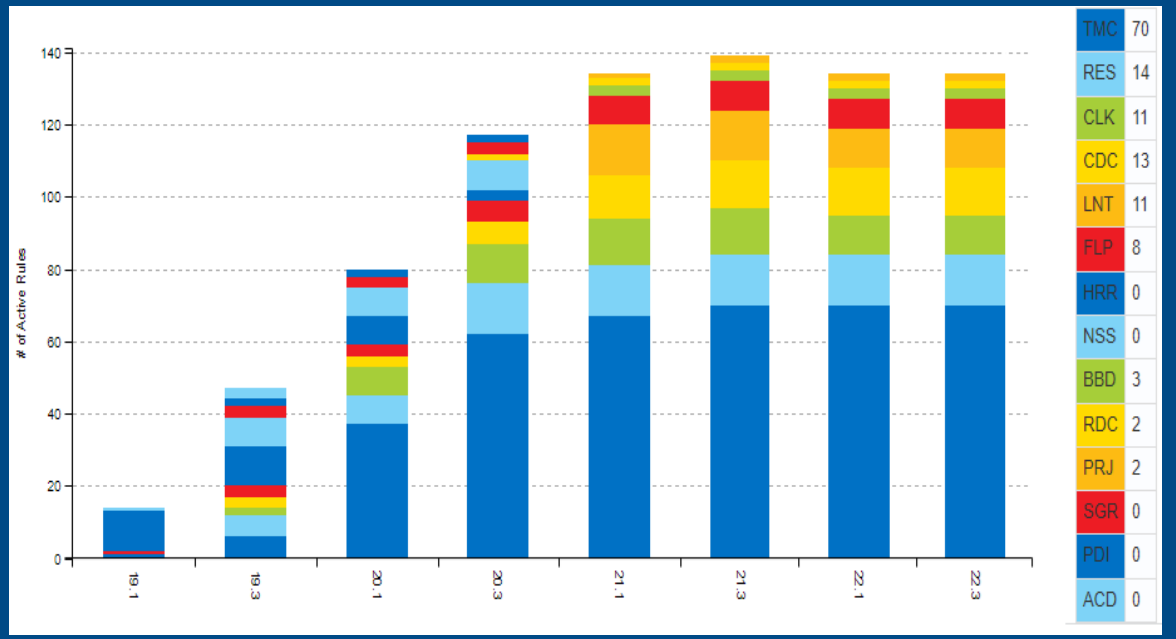
- Plug-in and built-in with industry EDA and embedded leaders
- Simulation, CDC and RDC, interfaces, and formal verification

Maximize Silicon Performance and Deliver an Intuitive UX for FPGA developers

Design Assistant

- DRCs to Flag Common Issues
  - Timing Closure DRCs
  - SDC/CDC Rules
  - Block-Based or Partial Reconfiguration Design Rules
  - RTL Linting, Project Rules
- Tag Rules and Filter by Rules
- Violation Waivers
  - Express Waivers as Boolean Expressions





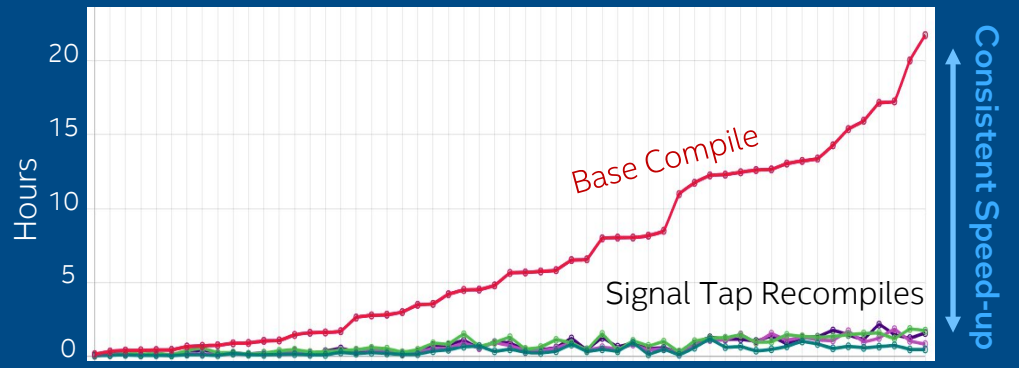
Fine Tuning

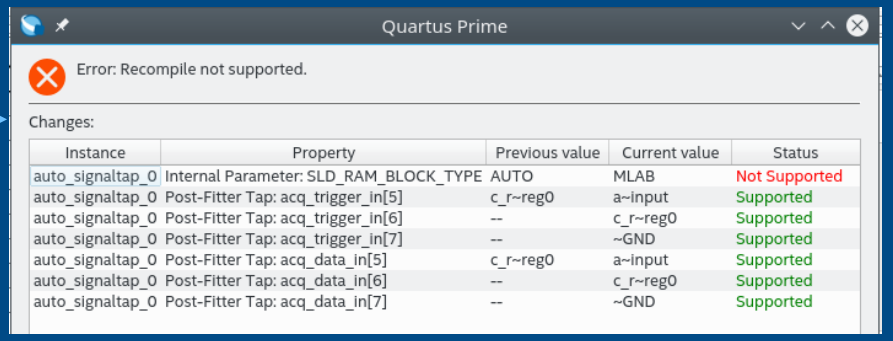
- False positive reduction
- Message clarity
- Cross-probing enhancements
- Runtime improvements

System Level Debug: Incremental / ECO Signal Tap

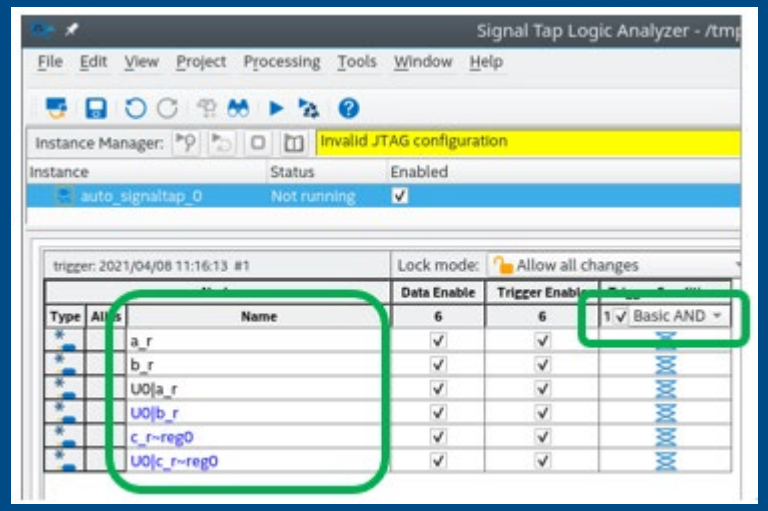
Change Description	21.1	22.3
Change postfit tap targets	✓	✓
Change postfit tap inputs to Basic AND trigger	✓	✓
Change postfit tap inputs to Basic OR trigger		✓
Change Advanced trigger (postfit inputs and/or logic)		✓
Increase number of post-fit tap targets		✓
Convert pre-synthesis tap to post-fit tap		✓
GUI Recompile Button Preview STP differences		✓

22.3 supports more types of changes





Changes are directly analyzed after clicking "Start Recompile" → Faster feedback



- Add/Change Post-Fit Targets regardless of Trigger mode
- Change Trigger mode
- Change Nodes allocated
- Pre-synthesis targets can be changed to Post-fit Targets
- Post-Fit Targets are shown in blue in the list

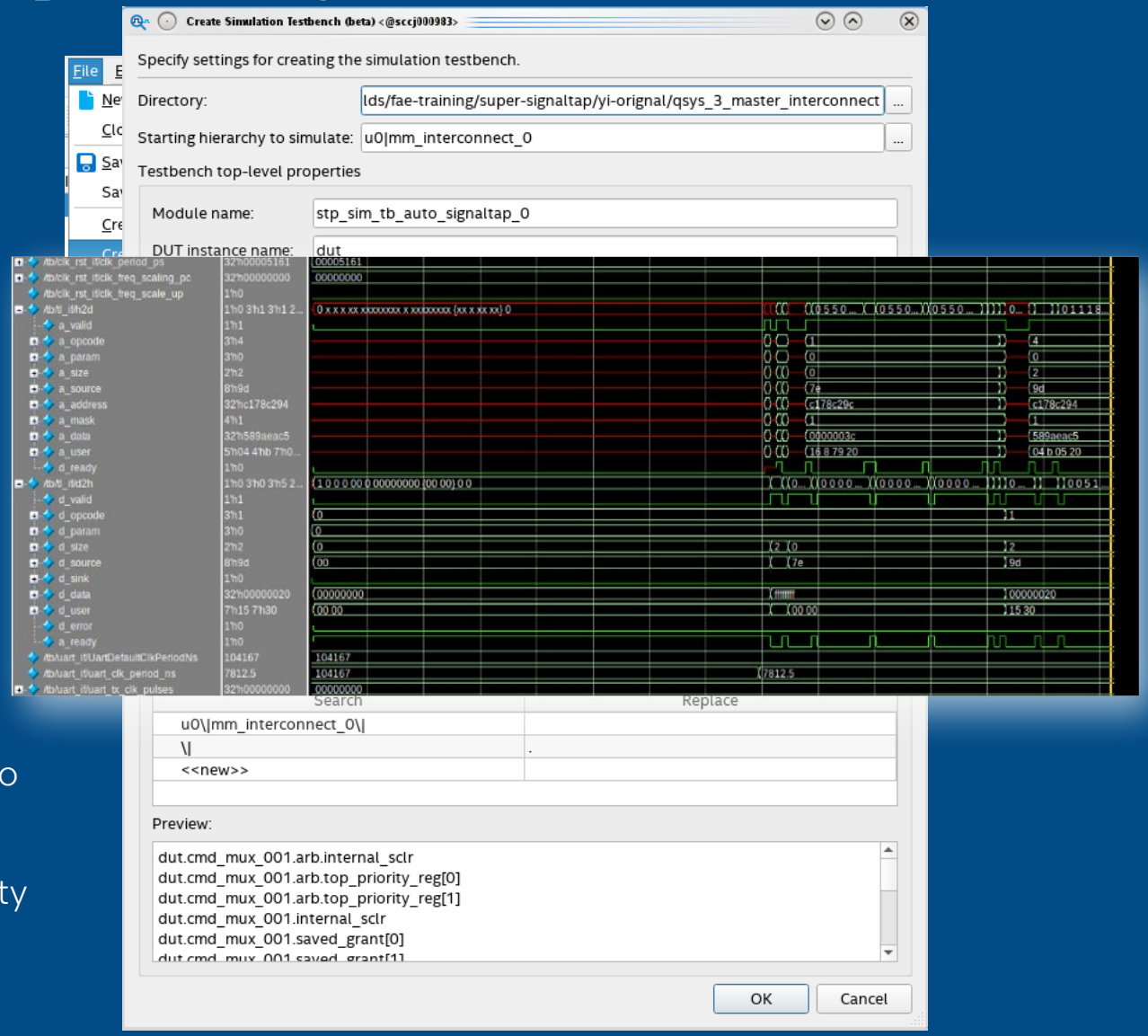
SLD: Simulator-Aware Signal Tap

Maximum Visibility with Minimal Resources

- Tap the minimum number of nodes in hardware
- Export Signal Tap data to Simulator
- Gain visibility of 10X or more node visibility
- Limits the number of iterations and compiles required

Flow for Simulator-Aware Signal Tap

- Add “Simulator-Aware Nodes” with Intelligent Node-Finder
- The Intel® Quartus® Prime Software will generate simulation scripts and export captured hardware data to be loaded in RTL simulator
- RTL simulator provides full visibility into the functionality of the instance based on the initial hardware data



Power and Thermal Calculator (PTC)

New tool for

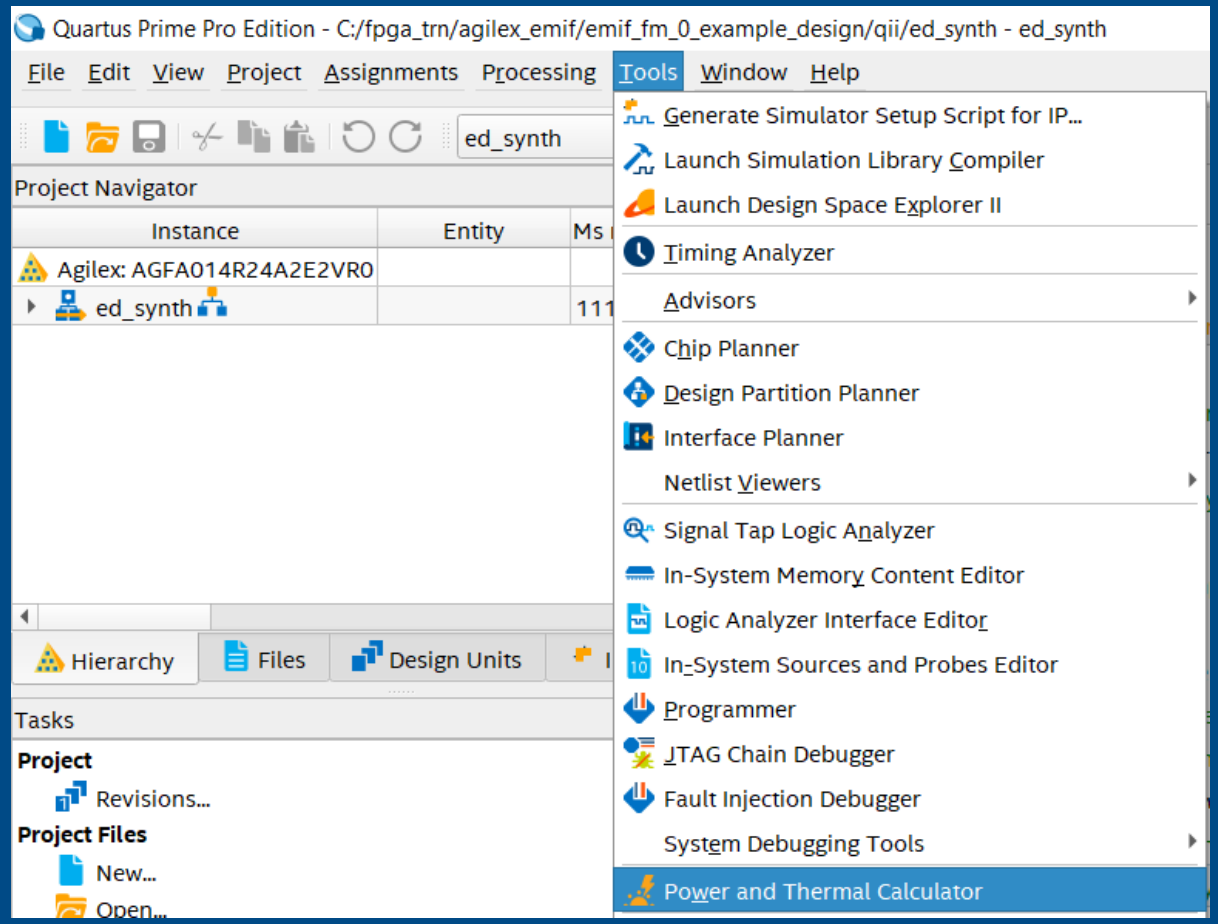
- Power estimation
- Regulator sizing
- Thermal Tab for system thermal design and CFD optimizations

Intel Agilex® FPGA and Intel® Stratix® 10 FPGA Support

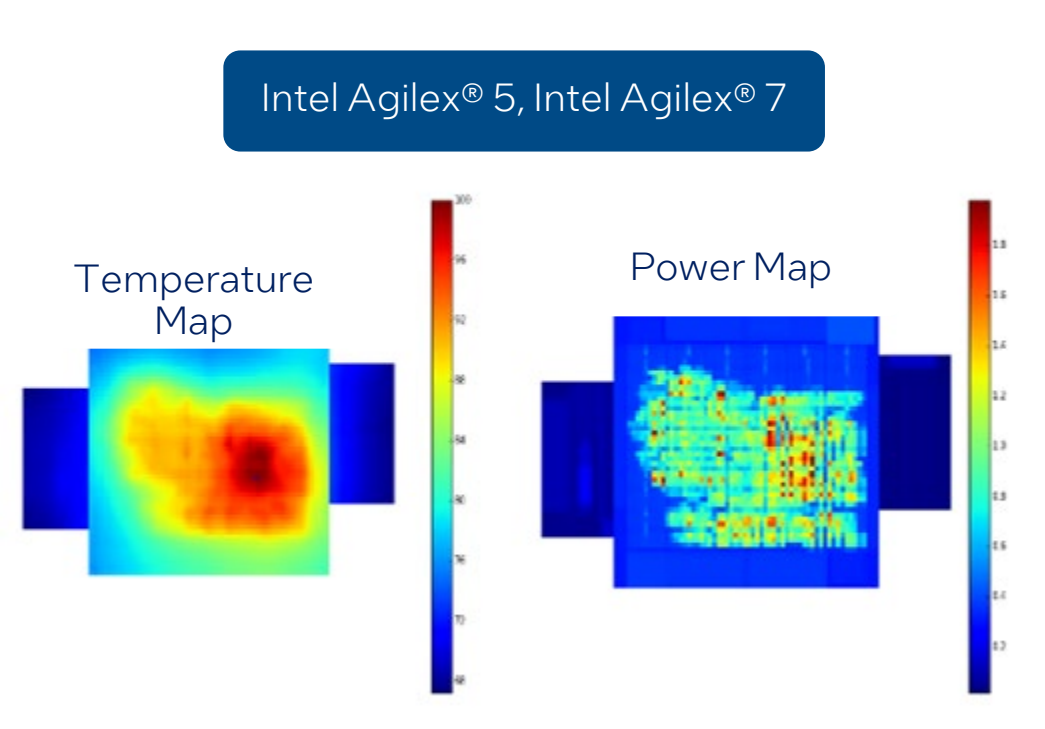
- Same accuracy as the Early Power Estimator (EPE)
- Within 15% from Silicon with final device models

Advantages

- Not based on Microsoft* Excel*
- Faster operation and response time
- Available in the Intel® Quartus® Prime Software (Integrated and Stand-alone)
  - Windows* and Linux*



Power and Thermal Analysis for Intel Agilex® FPGAs



Granular Power models
- Higher granularity of modelling
- Consistent pre-silicon modelling across blocks
- Automated coverage and checks deployed for accuracy

Efficient thermal simulations
- A hybrid technique developed for solving heat conduction problems

Hardware mapping
- Enable logical to spatial mapping on the die

Efficient system-level simulations

Increased accuracy of Thermal and Power models helps add to the Perf/Watt advantage for Intel Agilex® FPGAs

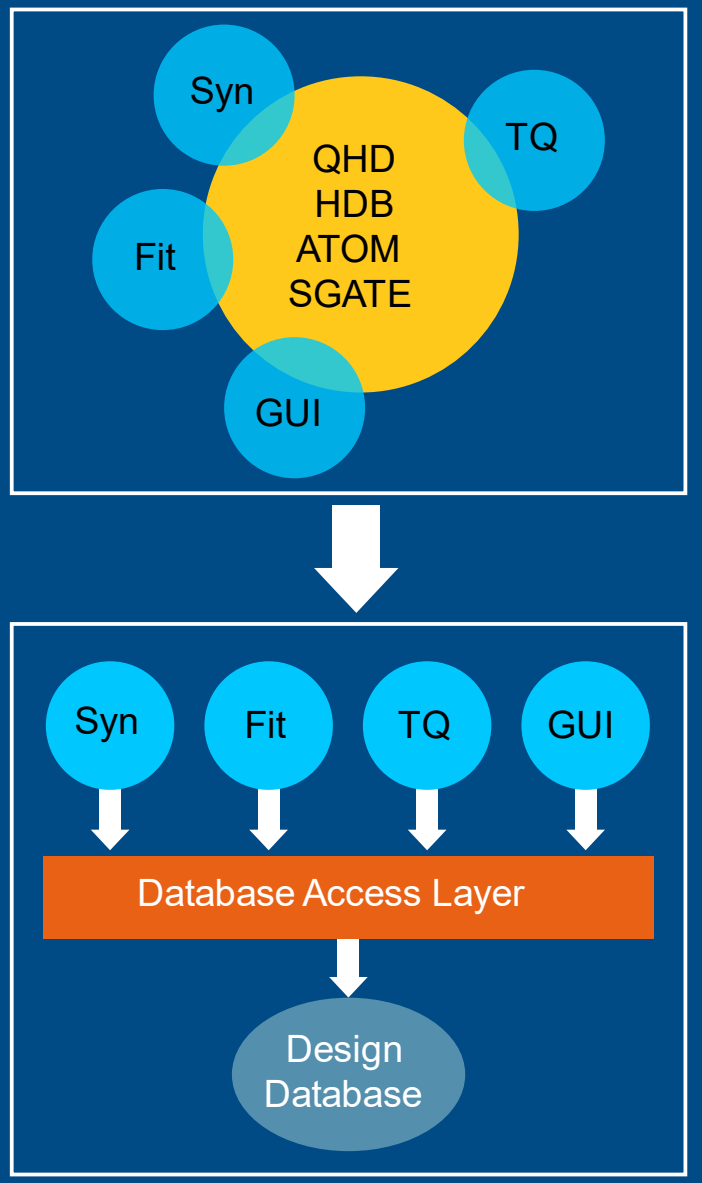
Design Netlist Infrastructure(DNI)

Major infrastructure update to the Intel® Quartus® Prime Software

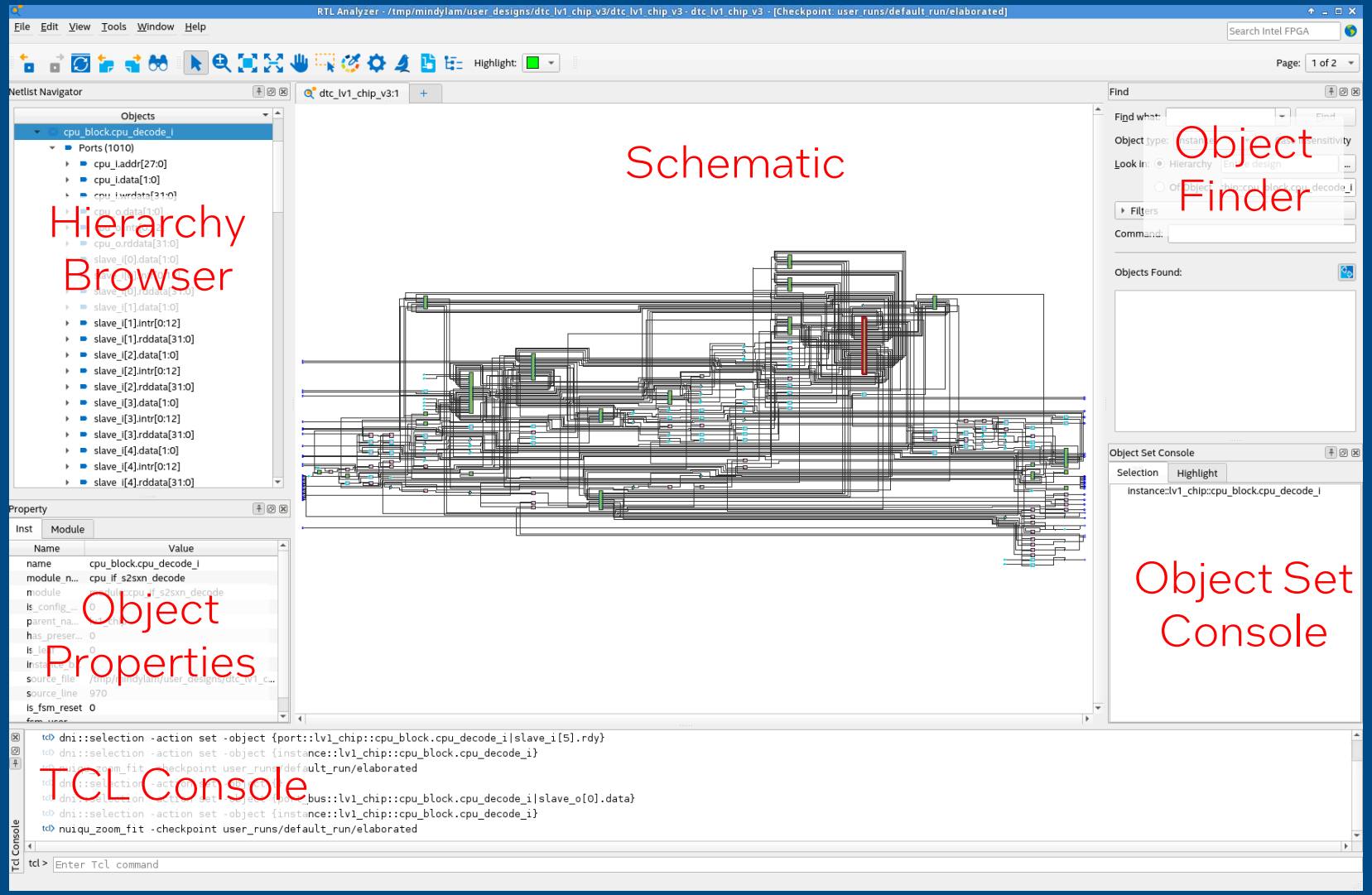
- Unified database
- Unified scripting layer to decouple backend from UI
- Unified UI IDE

Customer productivity

- WYSIWYG viewer on design (RTL Analyzer)
- Common infrastructure facilitate communication between tools
- Hierarchical design enabling block level design
- Incremental flow making iteration faster
- SDC on RTL
- Early timing analysis
- And more …



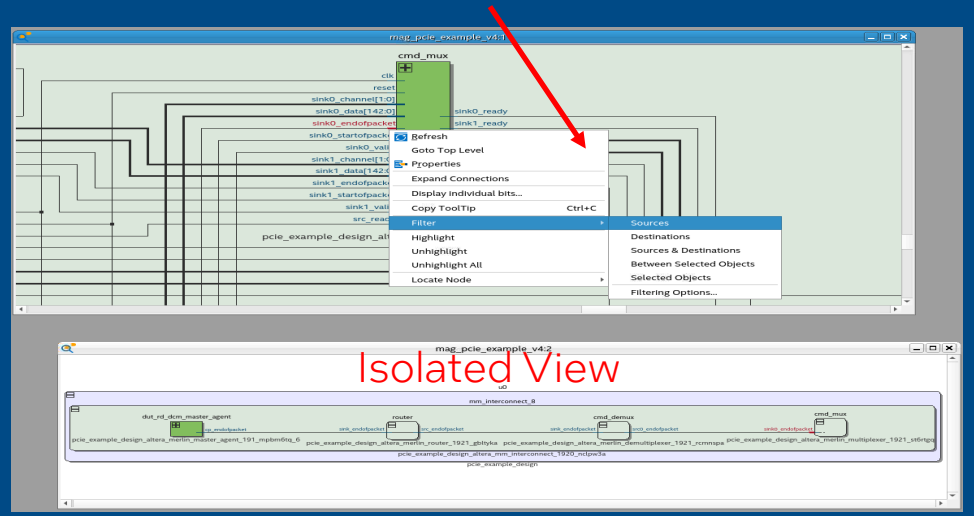
DNI: RTL Analyzer

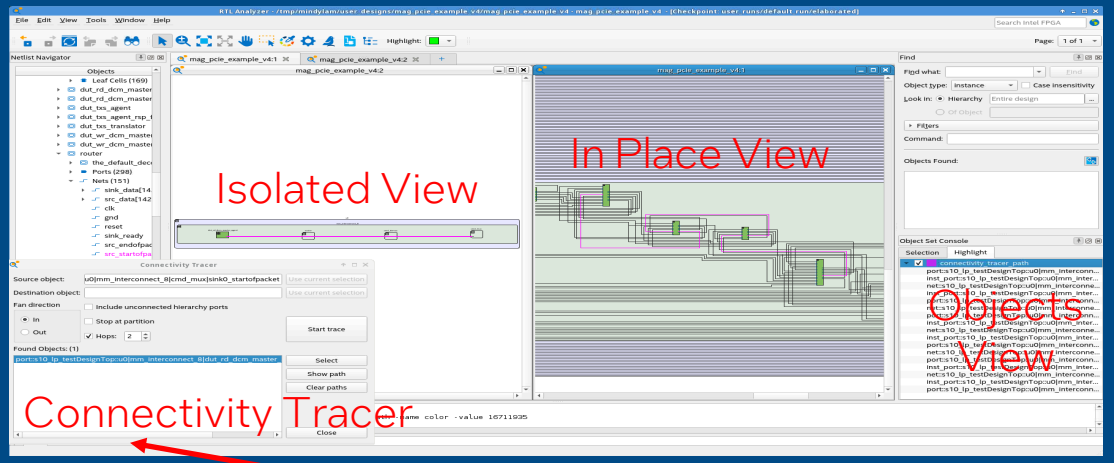


- You can see multiple debug points at the same time
- Cross-probing across multiple views and source RTL
- Graphical hints to show objects that will disappear after logic clean up

DNI: Connectivity Tracing

Quick access to trace connectivity

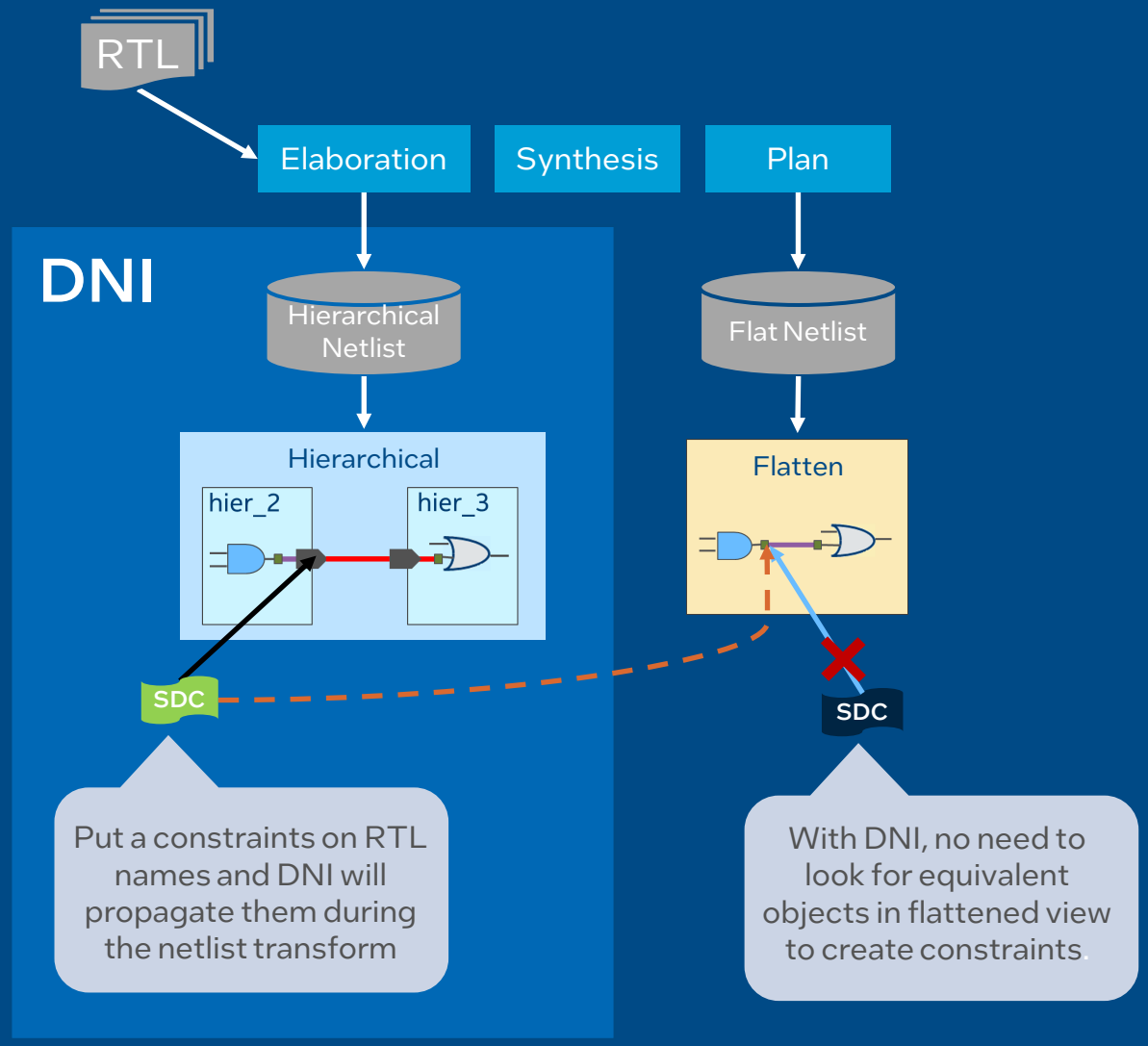




Through Connectivity Tracer Tool

- Helps you to trace logical connectivity in your design
- Options to trace direction, level of hierarchy, stop at register, etc.
- Highlight the path in the context of the whole design or isolated view with only connecting objects
- Group connecting objects as an object set for you to explore

DNI: SDC on RTL



- Create SDCs based on RTL names that you are familiar with
- Iteration interval is shortened when SDCs are applied early in the design setup and maintained throughout the compilation
- Seamless transfer of SDC from Synthesis to Fitter
- Enables timing analysis after Synthesis to give early timing feedback

Will the Intel® Quartus® Prime Software be available for free for Intel Agilex® 5 FPGAs E-Series ?

YES

- Intel Agilex® 5 FPGAs E-Series will be supported using:
  - Intel Quartus Prime Pro Software at no cost
  - All you need is a zero-dollar license

Platform Designer with Board Aware Flow

intel®

Platform Designer – Board Awareness

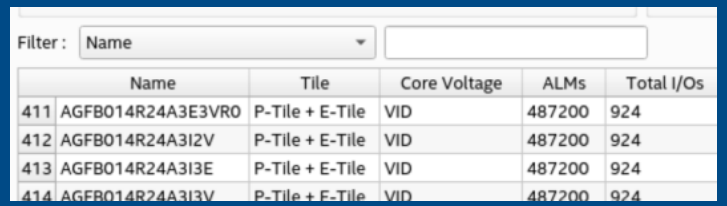
- **Why?** - Accelerates design creation for Intel boards and 3rd party boards
- **How?**
  - Board File and IP Preset File **Creation**:
    - IP Parameters, External Port Connections, and I/O Constraints extracted from a working design
    - Information extracted saved as Board File and IP presets
  - Board File Usage:
    - Board Files and IP preset files are read from the repo when the Intel® Prime® Software starts
    - **Intel Quartus Prime Software:** Lists of Boards in addition to Devices
    - **Platform Designer:** List of IP presets for the target board in a Board Tab
    - When instantiated IP presets applied with pin locations and I/O standards external ports are exported
    - QIP will contain I/O constraints that will be used in the compilation flow

Current Design Entry Overview

Device parts aimed – Device

Parametrization of IPs – IP Parameter Editor

Pin location assignments – Pin Planner



	Name	Tile	Core Voltage	ALMs	Total I/Os
411	AGFB014R24A3E3VR0	P-Tile + E-Tile	VID	487200	924
412	AGFB014R24A3I2V	P-Tile + E-Tile	VID	487200	924
413	AGFB014R24A3I3E	P-Tile + E-Tile	VID	487200	924
414	AGFB014R24A3I3V	P-Tile + E-Tile	VID	487200	924

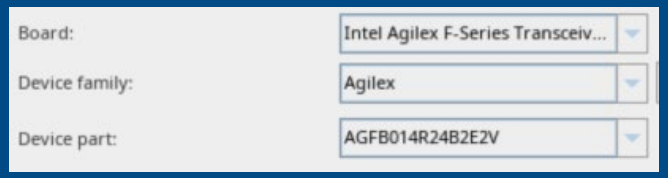
Node Name	Direction	Fitter Location	I/O Standard
reset_reset	Input	PIN_P45	1.2 V
clk_clk	Input	PIN_C40	1.2 V
pio_0_ex...xport[0]	Output	PIN_B31	1.2 V
pio_0_ex...xport[1]	Output	PIN_D31	1.2 V
pio_0_ex...xport[2]	Output	PIN_A30	1.2 V
pio_0_ex...xport[3]	Output	PIN_C30	1.2 V

Cannot Reuse Configuration ✕

Time-consuming and error-prone!

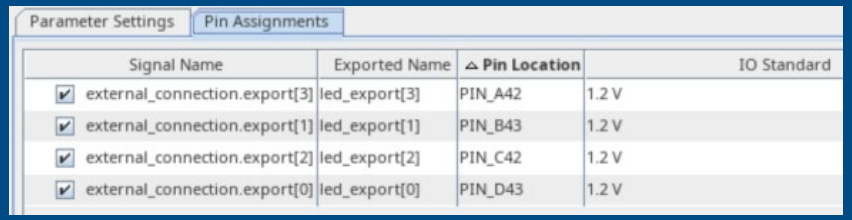
Board Awareness- IP Author and End User Flow

Device parts aimed – Platform Designer



Parameterization of IPs – IP Parameter Editor (in Platform Designer)

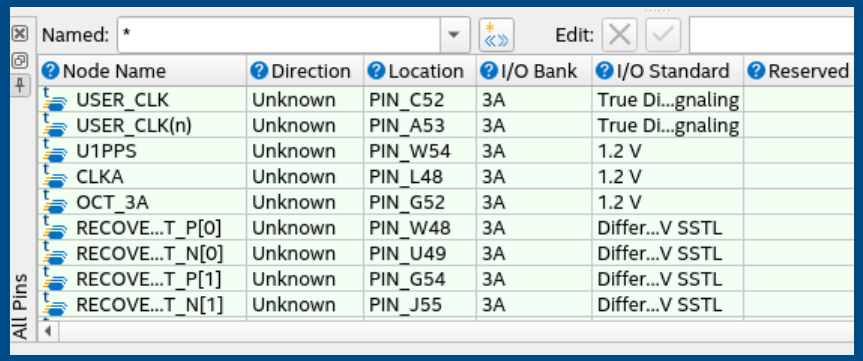
Pin location assignments – Platform Designer



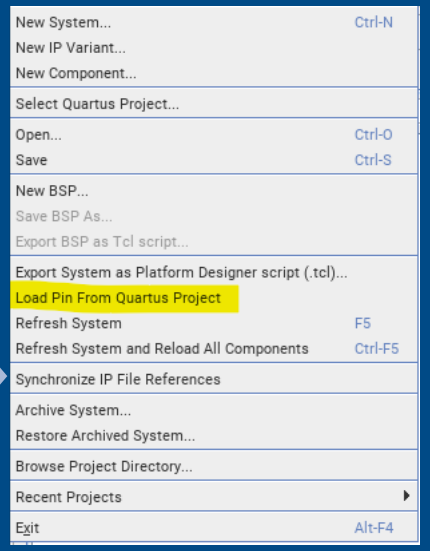
Can Reuse Configuration ✓

Time-saving and error-free!

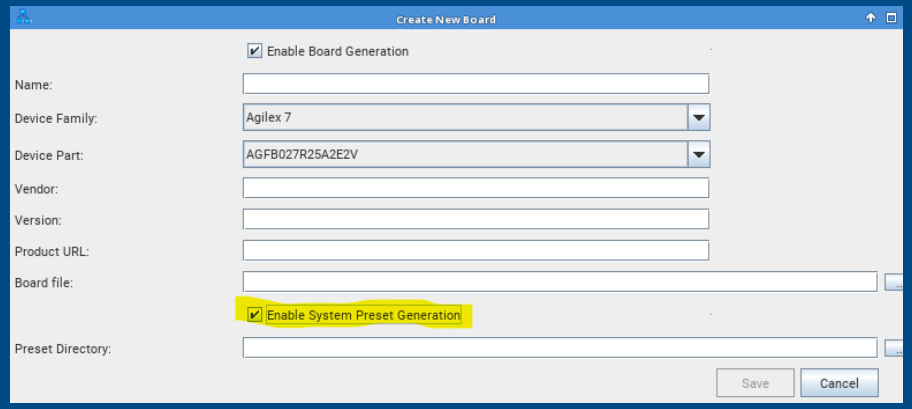
Preset Extraction Flow (from an Existing Design)



Existing compiled design with I/O standards and pin assignments



Load the pin information from the Intel® Quartus® Prime Software project into the Platform Designer



Capture information by enabling system preset generation

Nios® V Processor

RISC-V processors for Intel® FPGAs

intel®

Enabling the RISC-V Ecosystem

Fits your design flow with access to the RISC-V ecosystem of IDEs, compilers, debuggers, and real-time operating systems

Ashling* RiscFree IDE for Intel® FPGAs enables a single environment to debug hard (Arm) and soft (RISC-V) processors

Nios® V processor and Ashling RiscFree IDE for Intel FPGAs are included in the Intel® Quartus® Prime Software at **no cost**

Nios® V/m Microcontroller

New: Nios ®V/g General Purpose Processor

Future RISC-V Area Optimized Processor

Future RISC-V Application-Class 64-bit Processor

Nios® V Processor Cores Available Today

/m core

- Microcontroller configuration
- RV32IA RISC-V instruction set
- Enables the open-source ecosystem with uC/OS-II, FreeRTOS and Zephyr

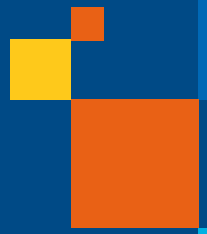
/g core

- General-purpose configuration
- RV32IMA RISC-V instruction set
- More functionality and performance with caches and integer multiply divide hardware
- Enables the open-source ecosystem with uC/OS-II, FreeRTOS and Zephyr

Both cores use the same software development flow and tools

Intellectual Property

For Intel Agilex® 5 FPGAs



intel®

Overview: Intel Agilex® 5 FPGA IP Blocks

Transceiver and GPIO	Network Interconnect	Communications
DirectPHY – PMA and FEC Direct XCVR IBIS AMI Models Direct PHY Fast Simulation Models PMA Direct FEC Direct PHYLite IP LVDS/SLVS Serdes IP GPIO IP I/O PLL IP HPS GPIO IP GPIO IBIS and IBIS AMI models - auto generated in Quartus HPS GPIO IBIS models – auto generated in the Intel® Quartus® Prime Software	Interlaken / Look-Aside (ILA) SIP 50G-100G SerialLite IV 1-4x Up to 25G Ethernet TSN HIP : 10M/100M/1G/2.5G System ED + Linux SW 10G/25GE HIP: CR/KR (AN, LT) 1588 (1.5ns) System ED 10G/25GE + 1588 + DR + Linux SIP: 1588 PTP-PTM Sync bridge, System ED, Linux SW 10M/100M/1G/2.5G/ 5G/10GE MAC + PHY Example design - SGMII+ PHY: 10M-2.5G - USXGMII PHY: 10M-10G 40GE MAC, PHY TSE / 10GE HIP + 1588 + CR/KR + DR	10G / 25G CPRI 10G / 25G eCPRI 10G / 25G O-RAN 10G / 25G Fronthaul Compression JESD 204B JESD 204C 4G Turbo / Turbo vRAN FEC 5G LDPC / LDPC vRAN FEC 5G Polar FEC

Overview: Intel Agilex® 5 FPGA IP Blocks (Cont'd)

Memory and Storage	Video	DSP
DDR4 LPDDR4 DDR5 LPDDR5 PHYLite HPS and DIMM support NAND Flash PCIe 3.0 x4 PCIe 4.0 x8	HDMI 2.0 HDCP 1.4 / 2.3 SDI 12G DP 1.4 / 2.0 MIPI D-PHY MIPI CSI-2 MIPI DSI-2 USB 3.2 Gen2 Video and Vision Processing Suite	DSP Builder for Intel® FPGAs (Advanced Blockset) All DSP IP optimized for Intel Agilex® 5 FPGAs

Intel® Video Processing IP Portfolio and Roadmap

VVP

Video and Vision Processing IP (VVP) Suite 32+ cores

Scaler, Clipper, Mixer, Color Converter, De-Interlacer

Consistent Performance:
Fmax >600 MHz
Agilex 7 and 5 D

AXI-4

Optimized for >8K60

Agilex 7 - Now
Agilex 5 E – 2H2023
Agilex 5 D – 1H2024

ISP

11 new cores

300 MHz (A10, Agilex 5 E)
600 MHz (Agilex 7, 5D)

Up to 64 Mpixels
8-16 BPS, 1-8 PIP
1-3 Colour Planes

Noise Reduction, Lens and Color Correction, AWB, Statistics...

AXI-4 (VVP compatible)

Agilex 7 - Now
Agilex 5 E – 2H2023
Agilex 5 D – 1H2024

Genlock

+7 new cores

Video input and output clock and/or start of frame (SOF) synchronization

Frame buffer-less uses
Ultra low latency
Clean switching
Mixing, blending, keying
Rate Conversion

External and VCXO-less operation

Agilex 7 – Now
Agilex 5 E – 2H2023
Agilex 5 D – 1H2024

WT3

VVP Premium cores
Optimized for >8K60

3D LUT – convert between different colour spaces and dynamic ranges

Warp – geometric transformations & camera lens correction

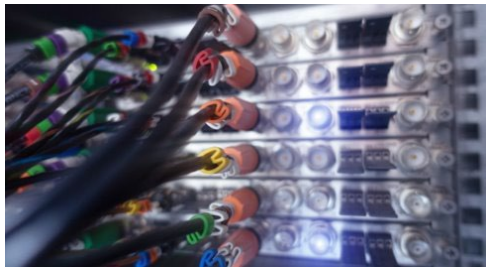
TMO – provides image contrast enhancement

Agilex 7 – Now
Agilex 5 E – 2H2023
Agilex 5 D – 1H2024

New Video & Vision Processing IP Suite (VVP)

- Retuned Video and Vision Processing IP (VVP) Suite – 32+ cores
- New cores and features
- Consistent Performance: Fmax >600 MHz
- AXI-4
- Optimized for 8K60 and above
- Expanding portfolio (ISP, Genlock, Audio, …)



[Video and Vision Processing Suite Intel® FPGA IP User Guide ›]

[Intel® FPGA Streaming Video Protocol Specification ›]

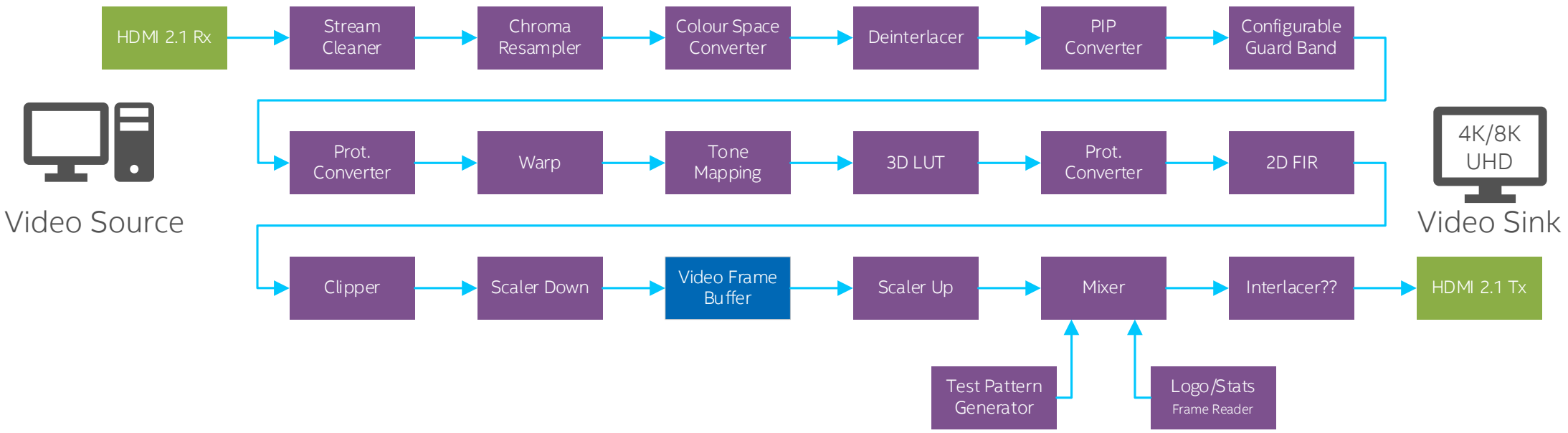
Video, Image and Vision Processing IPs …

Timing IPs
Protocol IPs
General Processing IPs
ISP IPs

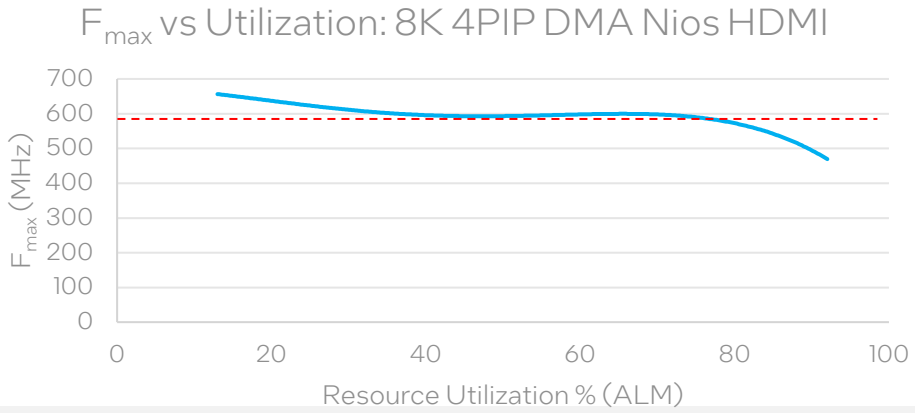
Clocked Video Input	Clocked Video Output	CV to FR Converter	Genlock Controller	Stream Cleaner	Warp	Scaler
FR to CV Converter	FR to AXI4-S Converter	Video Broadcaster	PIP Converter	Frame Cleaner	3D LUT	Tone Mapping
Video Crosspoint	Genlock Router Profiler	VTiming	Prot. Converter	Deinterlacer	Video FIFO	Video Frame Buffer
Test Pattern Generator	Clipper	Gamma	Interlacer	Mixer	2D FIR	Switch
Configurable Guard Band	Colour Space Converter	Chroma Resampler	Chroma Key	Video Frame Reader*	Video Frame Writer*	ISP IPs (11)*

> 600 MHz | AXI | 8K60 | Backward Compatible

8K Video Processing



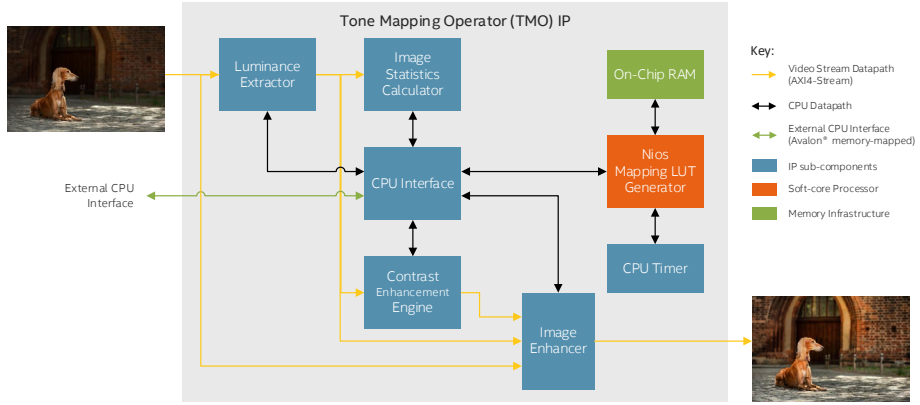
- Linux IP Discovery
- Nios V Adoption
- Complete 8K60 @ 600Mhz Designs
- Consistent +600MHz Fmax up to 80% device utilization



Tone Mapping Operator (TMO) Intel® FPGA IP

Improves local contrast and visibility

- Supports RGB 8-bit, 10-bit, or 12-bit per color component
- 1, 2, and 4 parallel pixels per clock
- 16 tile local image statistics collection
- Supports resolutions up to 8K @ 60 fps
- Subframe latency (~ 100 clock cycles)
- Low FPGA resource usage
- CPU bare metal drivers



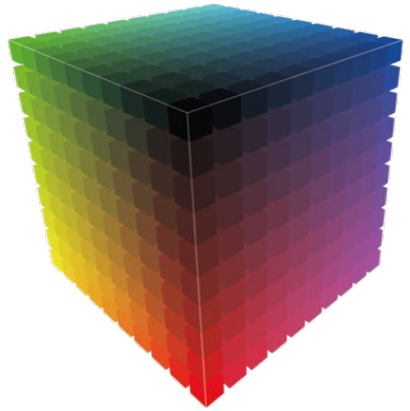
Applications

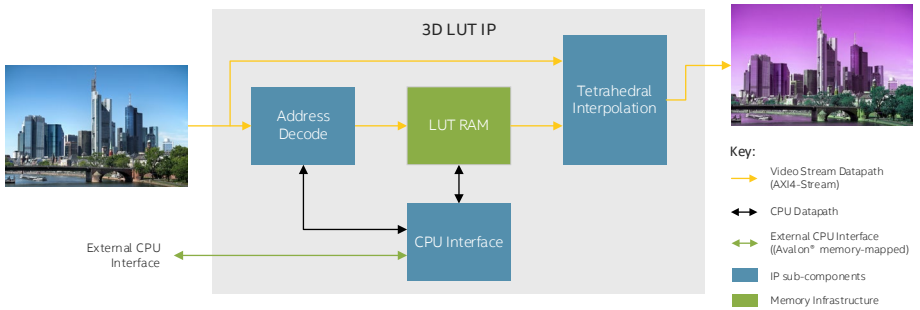
- Automotive
- Medical
- Video Projection
- Security
- Video Conferencing
- Machine Vision

3D LUT Intel® FPGA IP

Color-space and non-linear gamuts conversion

- High quality
- Supports RGB 8, 10, 12 or 16 bit per color component
- 1, 2, and 4 parallel pixels per clock
- 9^3, 17^3, 33^3, and 65^3 LUTs
- Supports resolutions up to 8K @ 60 fps
- 3 or 4 output channels (alpha channel)
- Low latency and highly configurable





Applications

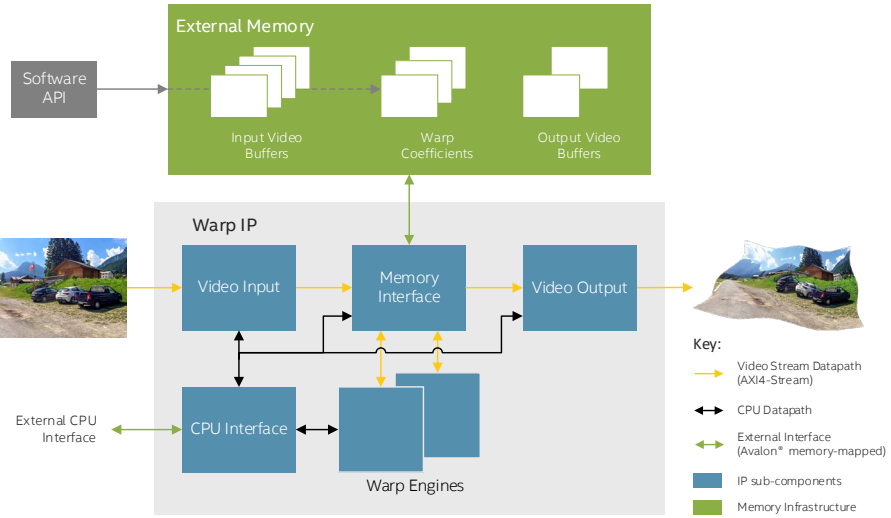
- Video projectors
- Medical
- Virtual reality
- Multi-camera stitching
- Digital signage
- Interactive graphical/web content

Warp Intel® FPGA IP

Adobe Stock
Image 156322912
Panoramic scenario of
Italian Alps, Dolomites
By jovannig

Geometric corrections and arbitrary non-linear distortions

- Per-pixel filtering
- Efficient external memory interface
- QPDS Support 4K @ 60 fps
- 8K60 on Agilex
- Color convergence, Edge blending
- Low FPGA resource usage
- Drivers and Application



Applications

- Video projectors
- Medical
- Virtual reality
- Multi-camera stitching
- Digital signage
- Interactive graphical/web content

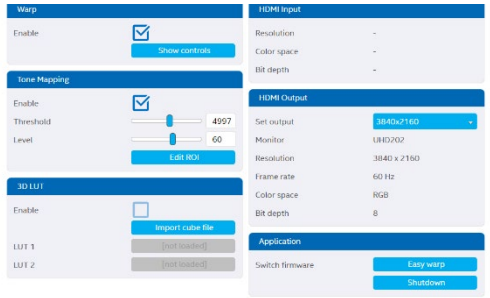
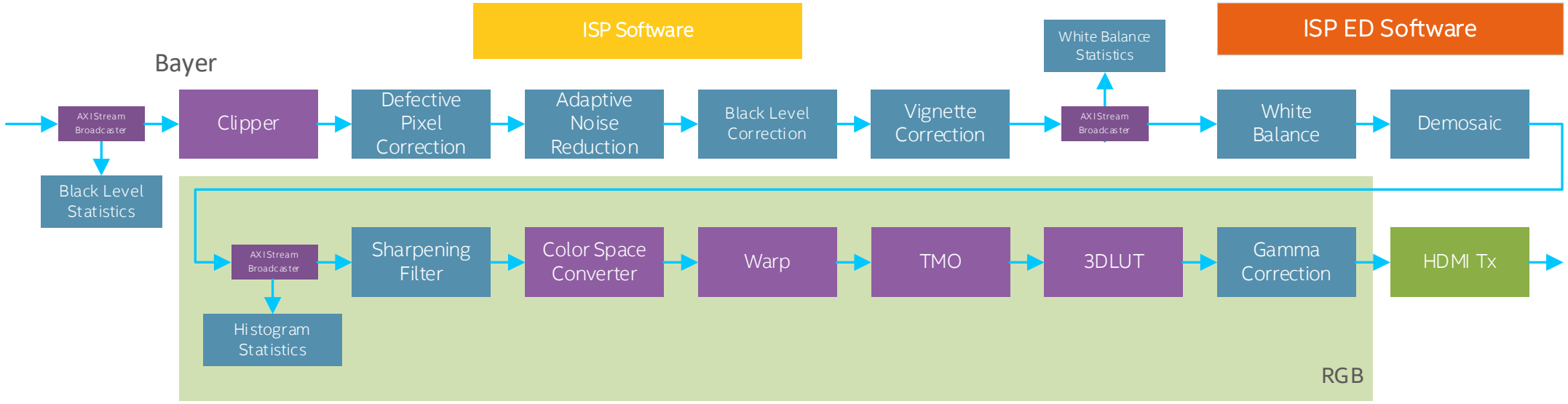
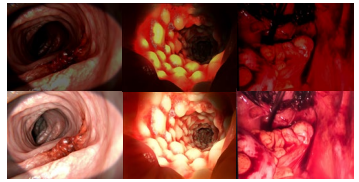
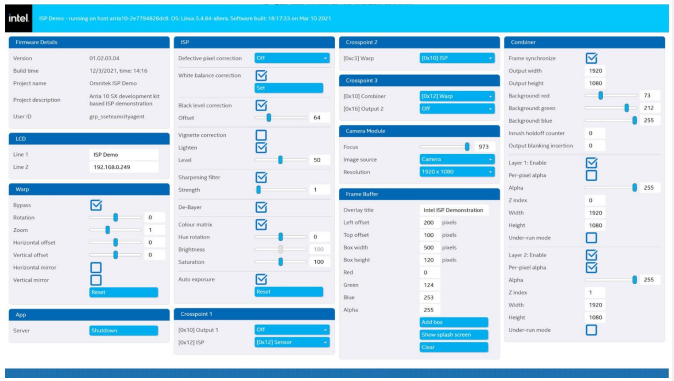


Image Signal Processing (ISP)



- QPDS - 11 New ISP IPs
- Example Design: Turn-key System Design on SoC, SW, Web GUI, etc
- ISP SW Model: Individual IP Functions, C++ Library





Intel® Video Connectivity IP Portfolio and Roadmap

DisplayPort

Compliant with v1.4 and v2.0
Up to UHBR20

Up to 4-channel MST
Up to 8-ch audio
Deep color mode, 48bpp

Includes Link-Training
Adaptive Sync
HDR metadata transport
HDCP 1.4 and 2.3

Agilex 7 - Now
Agilex 5 E – 1H2024
Agilex 5 D – 2H2024

HDMI

Compliant with v1.4, v2.0 and v2.1
TMDS and FRL modes
Up to 48Gbps

Up to 32-ch audio
HDR infoframe
HDCP 1.4 and 2.3

Variable Refresh Rate (VRR)
Auto Low Latency Mode (ALLM)

Agilex 7 - Now
Agilex 5 E – 1H2024
Agilex 5 D – 2H2024

SDI

Multi-standard up to 12G-SDI

SMPTE425M level A & B

Payload ID ST352
CRC encode/decode
Line Number LN insert/extract

Audio Embed/Extract
Up to 4 groups (16-ch)
Sine wave generator

Agilex 7 – Now
Agilex 5 E – 1H2024
Agilex 5 D – 2H2024

MIPI

Hardened D-PHY v2.5
CSI-2 v3.0 (RX & TX)
DSI-2 v2.0 (TX)
Up to 8 lanes

Virtual Channel (VC)
Latency Reduction and Transport Efficiency (LRTE)
Smart Region Interest (ROI)

Up to 3.5Gbps

Agilex 5 E – 2H2023 (prelim)
Agilex 5 E - 1H2024
Agilex 5 D – 2H2024

Intel® Partner IP Portfolio and Roadmap

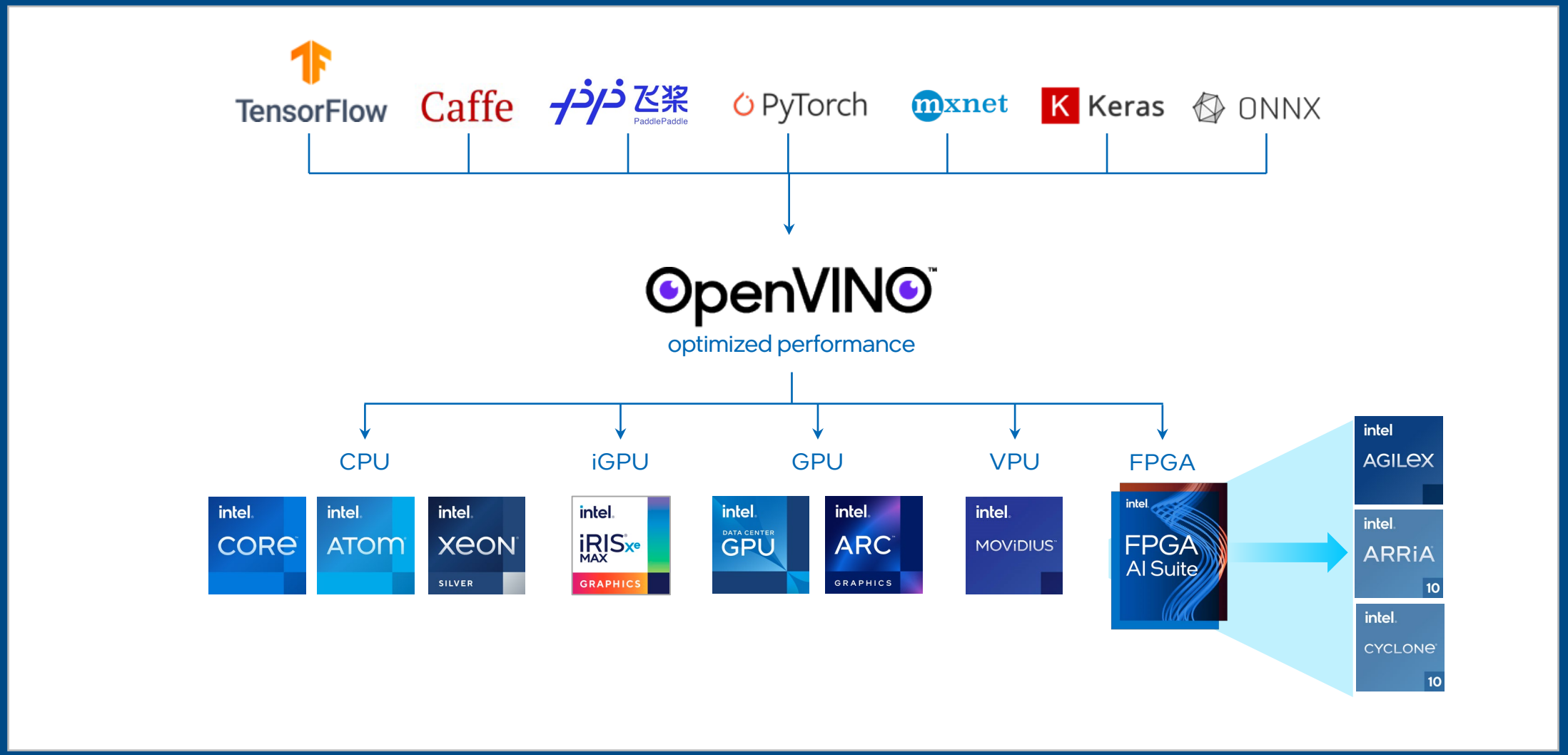
Macnica	Adeas / Nextera	NDI	B-Com	Rambus	Foresys Rambus Shiki no BitSimNow	intoPIX IBEX SOC Tech Visengi CAST	Grovf
ST2110 **SmartNIC** **SLVS-EC** **V-by-One** **CoaXPress**	**ST2110**	**NDI** **SpeedHQ**	SDR-HDR, HDR-SDR, HDR-HDR	**HDMI 2.1** **Rx DSC** **decoder**	MIPI various	CODECs various	**RoCEv2**
intel. CYCLONE, intel. ARRiA, intel. AGILEX, intel. STRATiX	intel. AGILEX	intel. ARRiA, intel. AGILEX	intel. CYCLONE, intel. ARRiA, intel. AGILEX	intel. AGILEX	intel. CYCLONE, intel. ARRiA, intel. AGILEX, intel. STRATiX	intel. CYCLONE, intel. ARRiA, intel. AGILEX, intel. STRATiX	intel. AGILEX, intel. STRATiX

intel.

Intel® FPGA AI Suite

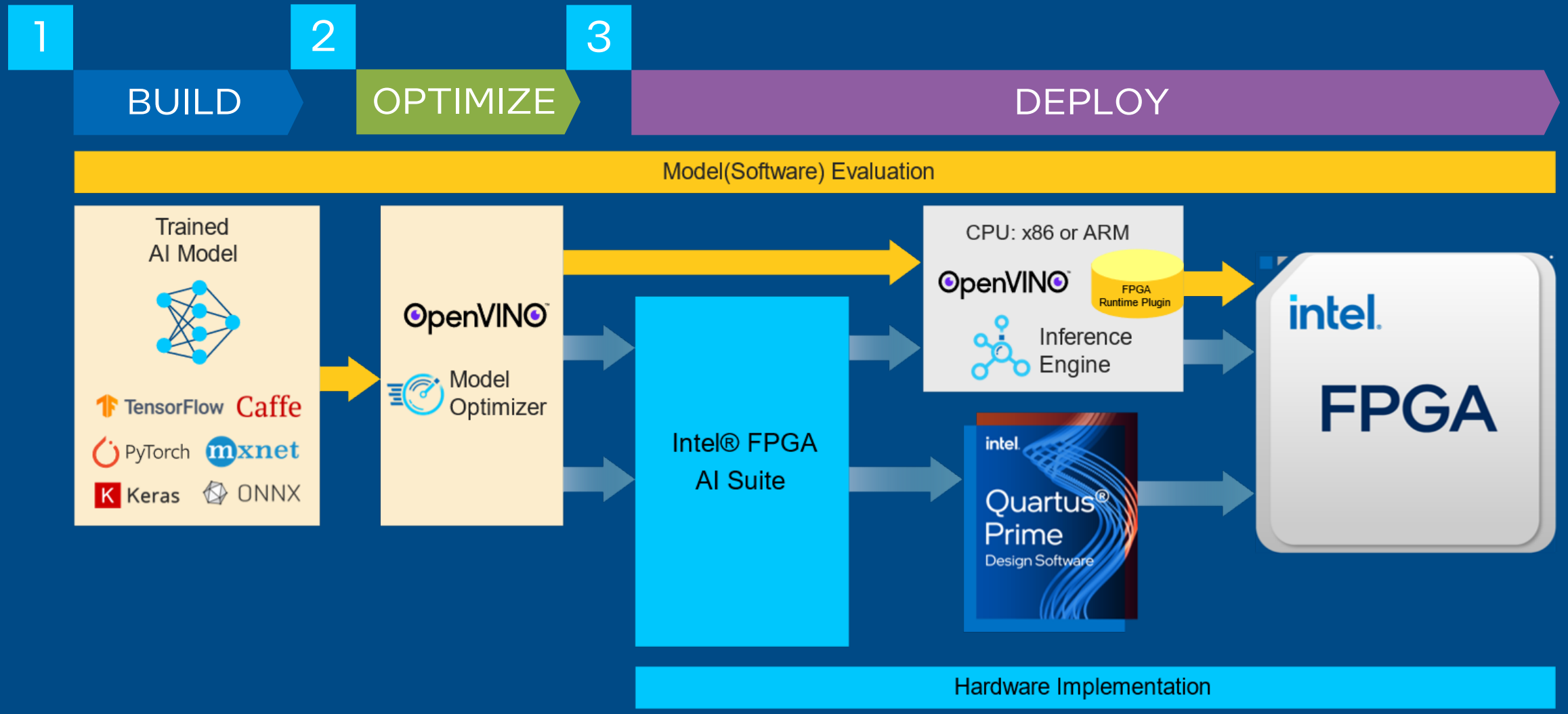
intel®

OpenVINO™ Toolkit: Deploy on Diverse Hardware

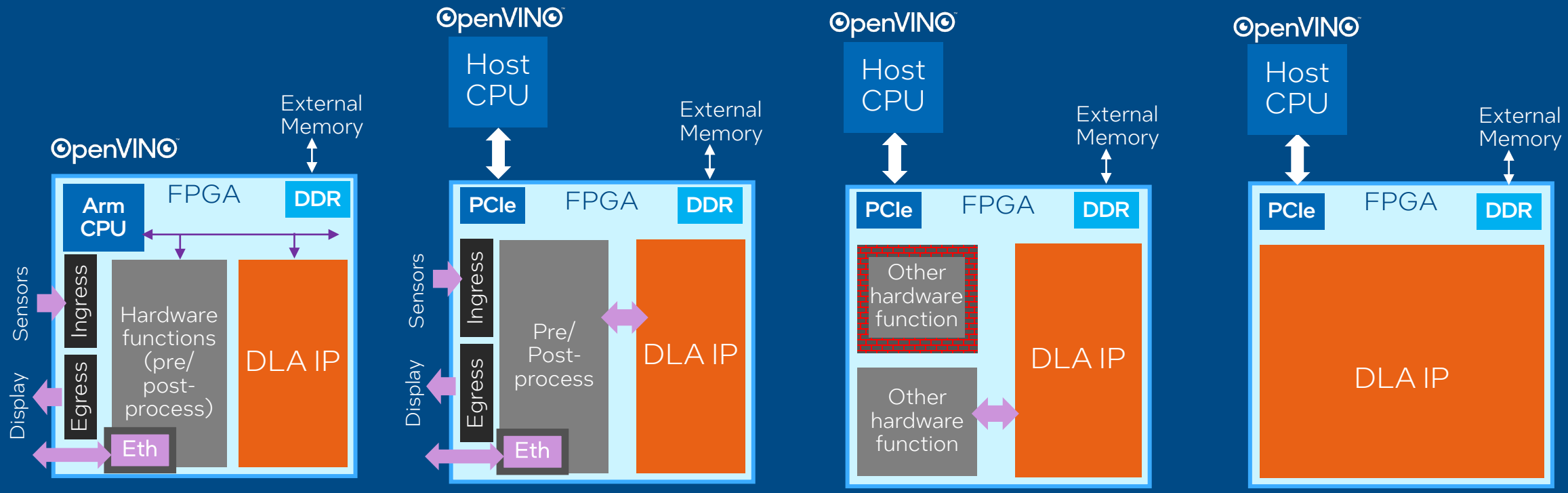


Custom Solutions with Intel® FPGA AI Suite

Deploy FPGA AI Suite optimized AI IP on custom platforms



Intel® FPGA AI Suite Enables +AI Use Cases



1- Embedded SoC FPGA + AI solution

2- Ingest / Inline Processing + AI

3- Multi-function CPU offload

4- CPU offload

- *DLA = Deep Learning Acceleration*
- *Above examples are generic and meant to illustrate the flexibility of FPGA AI Suite. Applications may utilize a soft host CPU (such as RISC-V based Nios® V processor in the FPGA fabric) and/or other in-line, streaming sources such as HDMI.*

Intel Agilex® 5 FPGAs Further Expands FPGA AI Suite Capabilities

Order of Magnitude Improvement in AI and DSP compute density

- Intel Agilex® 5 FPGA and SoC FPGA
- Offers 2 TOPS to 56 TOPS for INT8 across E-Series and D-Series device families with Enhanced DSP with AI Tensor Blocks
  - Multi-core Arm processors of Dual-core A55 @ 1.5 GHz and Dual-core A76 @ 1.8 GHz
  - Small package sizes: 15 mm x 15 mm and 23 mm x 23 mm

Applications	Multiplier	Capabilities per DSP Block		Improvement*
		Earlier Intel Agilex 7 ® Devices	Enhanced DSP with AI Tensor Block*	
AI, Signal Processing	INT8	4 OPS	20 OPS	5X
	INT9	4 Multipliers	6 Multipliers	50%
Signal Processing	16-bit Complex Multiplier	Needs 2 DSP Blocks	1 DSP Block	2X

OneAPI

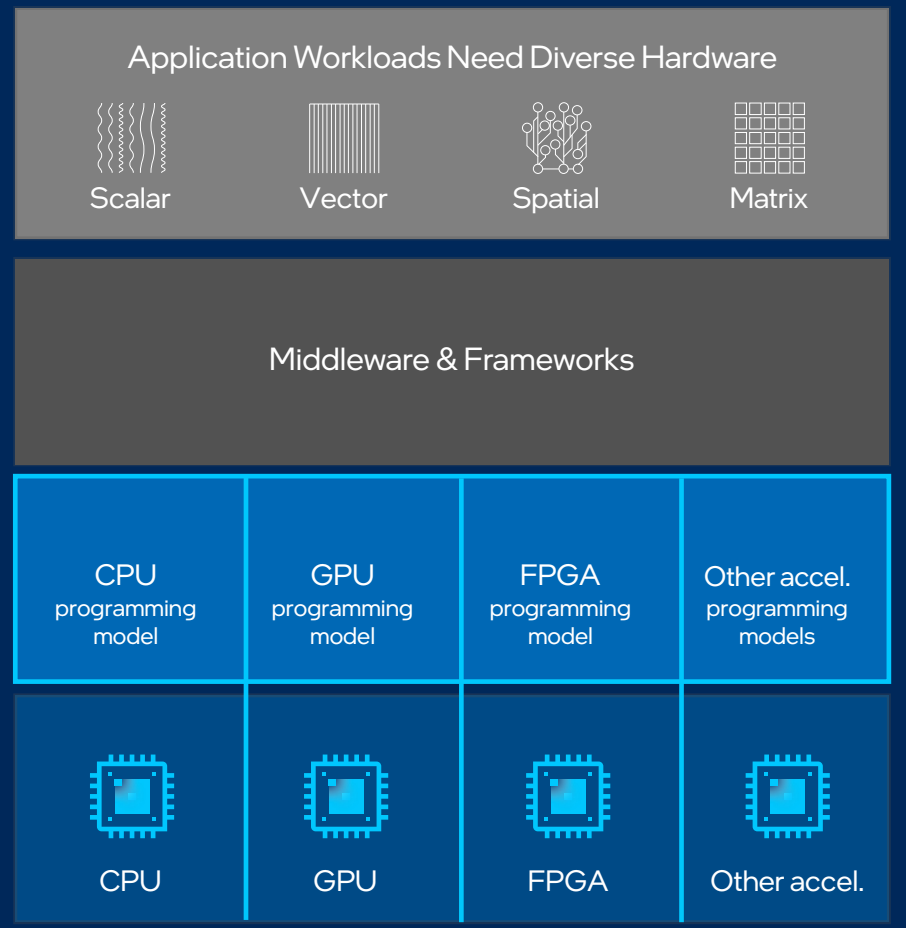
intel®

Programming Challenges for Multiple Architectures

40% of developers target heterogeneous systems that use more than 1 type of processor, processor core, or coprocessor.

Source: Evans Data Global Development Survey 2020, Volume 2

- Growth in specialized workloads
- Variety of data-centric hardware required
- Separate programming models and toolchains for each architecture are required today
- Software development complexity limits freedom of architectural choice

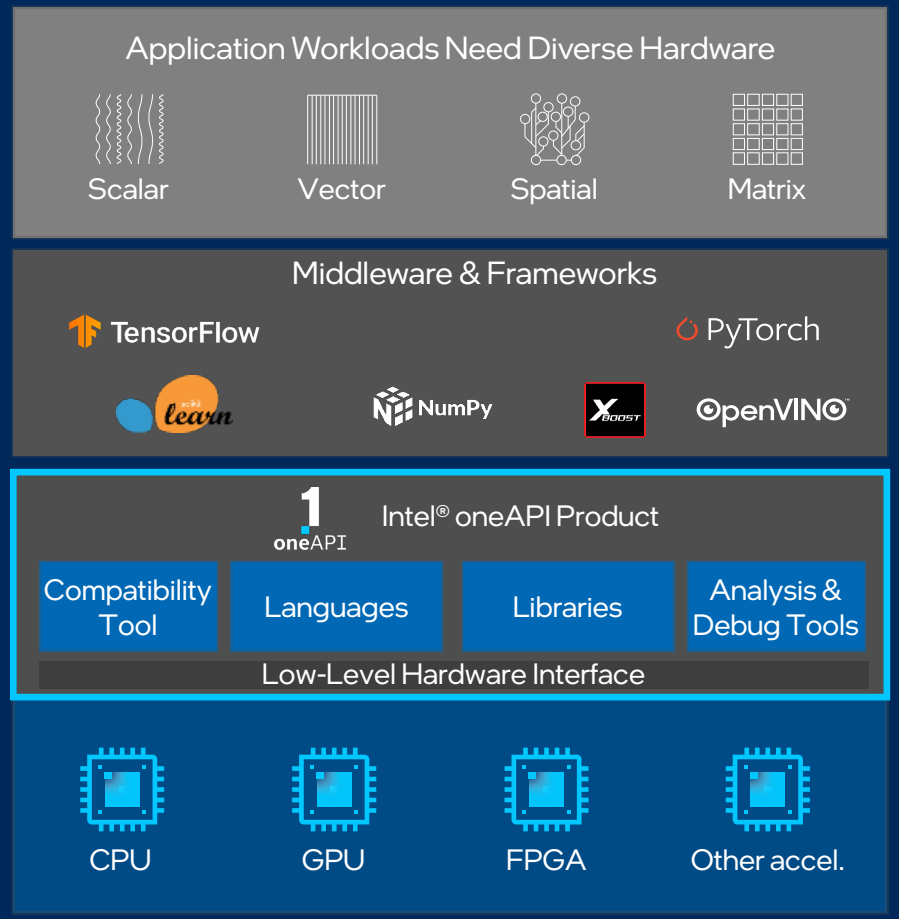


Intel oneAPI

- Software validation through Emulation
- FPGA Optimization Reports
- Debug and runtime analysis
- Industry leading Intel® VTune™ Profiler

- Native support for hardware parallelism
- Code Re-use across architectures
- Community led language

- Fast ramp-up/training for oneAPI Developers:
  - Intel® Developer Cloud to get started
  - Common sequential language
- Industry leading IDE Integration on VS, VS Code & Eclipse



Intel oneAPI for FPGAs

One Tool, Two Flows

- Full-Stack Flow
  - For **Software** developers to accelerate a part of their **full-stack** on an FPGA platform
  - FPGA bitstream automatically generated and execute on supported FPGA Platforms

- IP Authoring
  - For **Hardware** developers who wish to develop hardware **IP** for use inside the Intel® Quartus® Prime Software or Platform Designer
  - The FPGA IP is an industry-standard RTL

BittWare a molex company

HITEK SYSTEMS

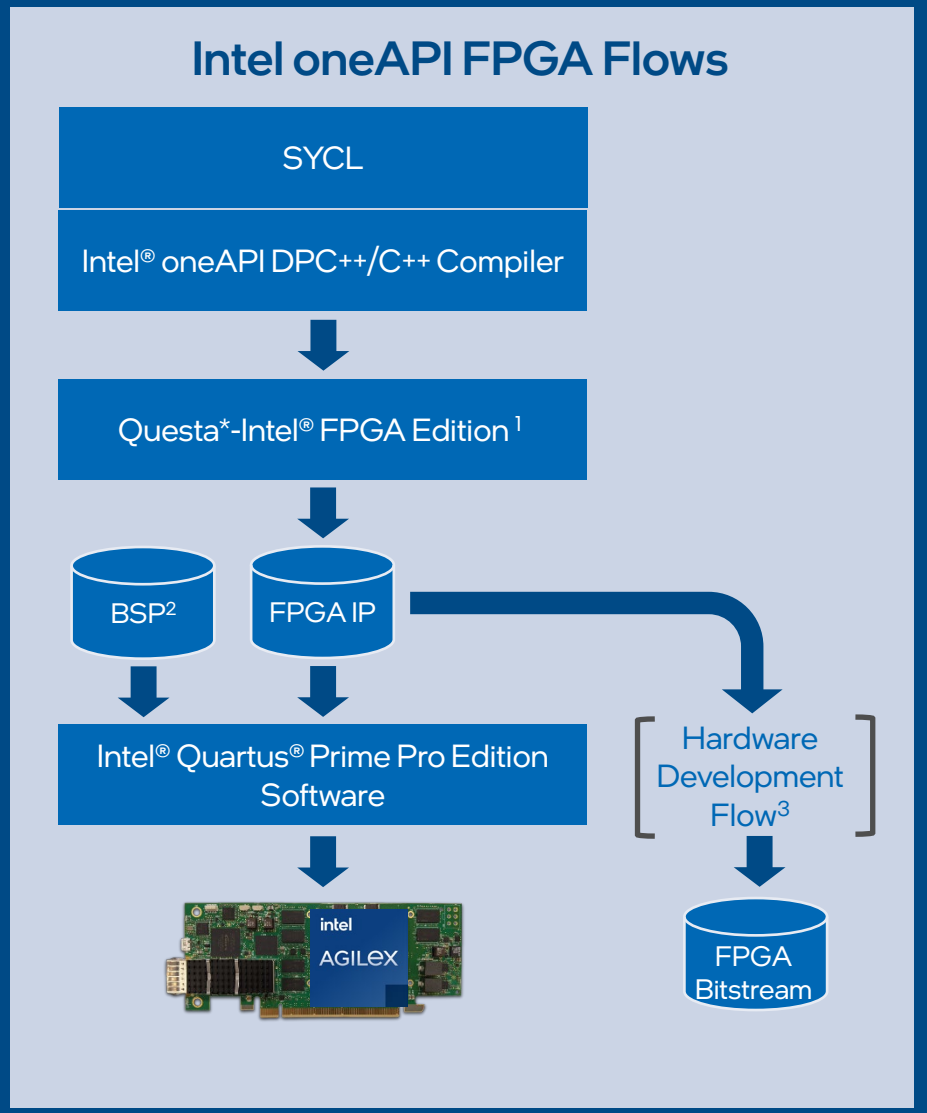
intel AGILEX 7

intel STRATIX 10

intel ARRIA 10

intel CYCLONE 10

intel CYCLONE V



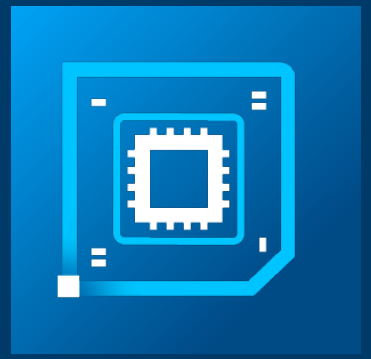
(1) Provided as part of Intel® Quartus® Prime Pro Edition Software (or use an RTL simulator of your choice)
(2) BSP : Board Support packages are available from 3rd party vendors, choose a platform here.
(3) The hardware IP is used hardware developers to build a new/unique FPGA design

Getting Started with Intel oneAPI

- oneAPI is License Free
  - No Intel® Quartus® Prime Software license is required to generate RTL
  - Licensed version of the Intel Quartus Prime Software required to synthesize the RTL
    - No Intel Quartus Prime Software license is required in Full-Stack Flow

- Get Started
  - By visiting the Intel FPGA Add-On site
    - Download information and documentation
    - Existing Intel Quartus Prime Software users review the IP Authoring Install Guide
  - On Intel DevCloud
    - 120 days of free Access to CPU, GPU, and FPGA platforms

Committed to Delivering Programmable Innovation



Leadership FPGA & Custom Logic

Best-in-Class Developer Experience

Industry-Leading Supply Chain

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