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How are we doing?

Although we pride ourselves in the service and support we provide to you, we also acknowledge that there is always room for improvement.

Therefore, as a valued customer we would deeply appreciate if you take a couple of minutes to fill in our customer perception questionnaire.

The answers you supply are completely anonymous, and the results will be used to further enhance the service we provide.

You can access the online survey from the following internet link:

[http://support.sundance.com/questions/questions\\_2007.html](http://support.sundance.com/questions/questions_2007.html)

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A splitter to put them all together...

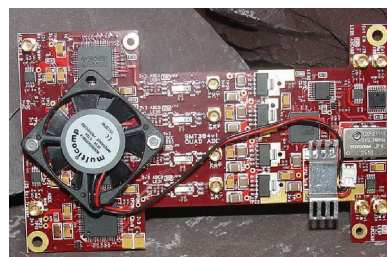
The [SMT594](#) is not a simple "Gadget" from Sundance to plug into the SMT384. It is an engineering adapter circuitry that turns your four ADC channels into one single analogue-to-digital input channel. The sampling frequency can reach up to 500MSPS using the interleaving methodology inside the FPGA-base module over the four input channels.

The analogue [performances](#) of [SMT384](#) can be improved by an efficient digital correction inside the FPGA. This task is done by the new [FC201](#) IP core from Sundance. It is designed to optimized some key parameters for any ADC modules. The designer can tweak the general offset, gain and delay correction in order to enhance the effective number of bits (ENOB) of the analogue-to-digital converter. This core is an hardware task that is fully compliant with the [3L Diamond FPGA](#) concept.

The main advantage of the SMT384 is its accurate and programmable clock circuitry based on the [AD9510](#) device that allows synchronization of several modules. System designers can cascade as many SMT384 as they wish to push the boundary of the most demanding applications.

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January 2007

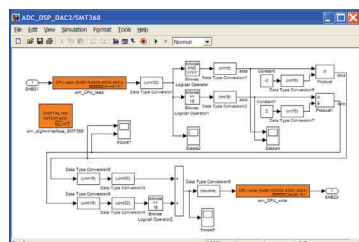


[SMT384](#), designed for interleaving and cascade architectures

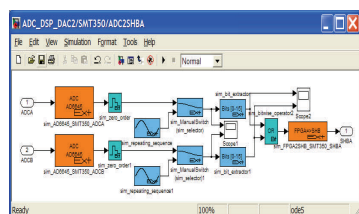
Newsletter Spotlight

- [Your opinion counts!](#)
- [Quad 14-bit ADC module](#)
- [ADC/DAC calibration core](#)
- [Simulink add-on for Video Kit](#)
- [Simulink add-on for Radio Kit](#)
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Zoom in on Modeling Framework for Hybrid Architectures



[SMT368](#), FPGA Blocksets



Model of the [SMT350](#)  
Dual 14-bit ADC/ 16-bit DAC

Hardware and software co-design methods, and simulation-in-the-loop are innovative approaches to design high-performance solutions with a very high level of abstraction.

It consists in the modeling of algorithms with general subsystems from toolboxes integrated in a MATLAB/Simulink framework without worrying about any implementation aspects. Once the algorithms are verified and validated within the simulation environment, the compilation starts after a manual HW/SW partitioning. Automatic optimized DSP and FPGA codes towards C-programming and VHDL are respectively generated to let place to the real co-simulation onto the Sundance's hybrid DSP+FPGA platforms.

The modules communicate with the MATLAB graph viewers via the carrier boards that implements a link to the Host PC while the real external stimuli (video capture, analogue or digital signals) are directly applied to the platform. The algorithms implemented can be finely tuned with accuracy as the result is immediately observed and interpreted from the hardware itself.

Sundance offers support for the [SMT8096](#) Software Defined Radio and the [SMT8039](#) Advanced Video Imaging systems. The [SMT6096](#) (also integrated in the SDR-DS) and [SMT6039](#) add-on for the Simulink environment give a Hardware/Software co-design toolboxes for rapid prototyping.

Ideally suitable for system level engineers, the Sundance's toolboxes targets both designers from the hardware and software worlds to build some efficient solutions onto proven platforms quickly.

[More Details](#)

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