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GENERIC SDR PLATFORM USED FOR MULTI-CARRIER AIDED LOCALIZATION

Igor Arambasic, Javier Casajus and Ivana Raos
Universidad Politecnica de Madrid (UPM)
Ciudad Univeristaria s/n, 28040 Madrid, Spain
{igor, javier, ivana}@gaps.ssr.upm.es

Abstract — This paper describes the Software Defined Radio (SDR) platform that is being developed and implemented in the scope of the EU 7th Framework WHERE Project. The platform is based on one full-length PCI carrier board populated with one DSP module, one dual high-speed ADC/DAC module and one module corresponding to IF/RF front-end. It is equipped with two omni-directional antennas working at 2.4GHz with 100MHz bandwidth. The platform is not restrained only to the PC tower box since its mobility is guaranteed with small portable PCI bus extension chassis supporting PCMCIA laptop connections. It is intended for exploring the localization possibilities of different multi-carrier interfaces.

1. INTRODUCTION

The presented SDR platform is developed using hardware produced by Sundance [1]. It is based on one full-length PCI carrier board (SMT310Q) which provides access to four, industry standards, Texas Instruments Modules (TIMs) format. The benefits of system based on this PCI carrier board approach include low-cost, scalable system configuration, flexible task allocation and above all expandable system which allows future expansions. In fact, the SDR platform used in WHERE project [2] is an expansion of SMT8036 SDR development kit which has been used for communication research and system demonstration purposes at the Universidad Politecnica de Madrid.

The SMT8036 kit includes C64xx-based module (SMT365) combined with a dual high-speed ADC/DAC module (SMT370), both plugged on a SMT310Q carrier board. The SDR platform implemented in WHERE includes an additional module which is the IF/RF front-end (SMT349). This module is delivered together with two omni-directional antennas working at 2.4GHz with 100MHz bandwidth.

Since WHERE SDR platform is imagined as dynamic and mobile system which is later to be used for measurements campaigns, the carrier board should not be restrained to large PC tower boxes. For this reason a PCI extension bus chassis is acquired. This chassis includes its own cooling fans

and power supply. It can be connected to the PCMCIA slot of the laptop (as seen in Figure 1) and as such offers flexibility and mobility to the system.

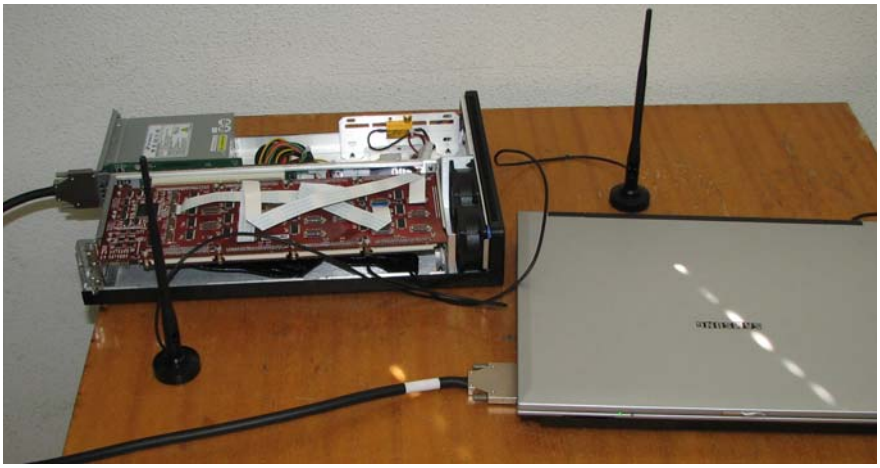

Figure 1.The carrier board is connected to laptop

2. PLATFORM OVERVIEW

The block diagram of WHERE SDR platform is depicted in Figure 2. The SMT310Q carrier board is connected to the host over PCI bus. The communication with the host computer is done only via SMT365 located in the root TIM slot. In fact the entire platform is controlled through this DSP as ADC/DAC and RF module are both programmed by DSP using comport connections on the carrier board. The connection between the SMT370, SMT349 and corresponding antennas is done via coaxial cables and MMBX connectors while data transmission between the DSP and ADC/DAC converters is achieved with Sundance High Speed Bus (SHB) protocol. The SHB connectors give 32-bit communication interfaces which operate at a fixed clock rate of 100MHz and can thus support traffic between the modules of up to 400MB/s.

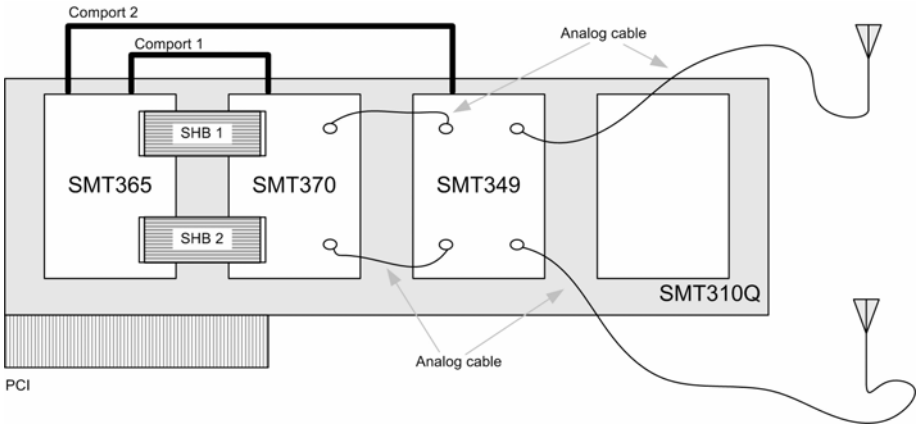

Figure 2. Block diagram of WHERE platform

2.1 SMT310Q - PCI Carrier Board

SMT310Q has an 'on-board' XDS-510 compatible JTAG controller which allows Code Composer Studio and 3L Diamond applications to be used for debugging or uploading the software to the modules. The interconnection of modules is done using comports which support communications at 20MB/s. The external comports cables are not necessary since the board supports software-configurable routing matrix between the TIM modules. The board also includes on-board V3 PCI bridge chip which provides DMA access, mailbox events, and interrupts control. The SMT310Q is connected to the host PC through standard PCI bus which runs at 33MHz. Hence, the communication between the host and root TIM site is implemented at burst speed in the range of 60-130MB/s. This fact labels PCI access as a possible bottle neck for real time presentations of measurements on the host screen.

2.2 SMT365 – DSP Module

The presented SDR platform is based on Sundance SMT365 module at the root TIM space. The main components of this single width TIM module are one Texas Instruments DSP and one Xilinx FPGA Virtex-II device with the following characteristics:

- TMS320C6416 fixed-point processor running at 600MHz
- Xilinx Virtex-II device XCV2000
- Six 20MB/s Comports
- 8MB of ZBTRAM (133MHz)

- 8MByte Flash ROM for boot code and FPGA programming
- High bandwidth data input/output via 2 SHBs

2.3 SMT370 – ADC/DAC Module

The second TIM slot is filled with SMT370 which is a single width TIM module that offers dual high-speed ADC/DAC processing characterized with the following features:

- Two 14-bit ADCs (AD6645-105) sampling at up to 105MHz, DC coupled
- Dual 16-bit TxDAC (AD9777) sampling at up to 160MHz without interpolation and up to 400MHz with interpolation
- Xilinx Virtex-II FPGA (XC2V1000-6).
- Two SHB connectors.
- Two 20 MBytes/s communication ports.
- User defined pins for external connections
- 50-Ohm analogue inputs and outputs, external triggers and clocks via MMBX connectors.

The 14-bit ADC converter is able to sample from 30MHz up to 105MHz which makes it suitable for multi-carrier 3G applications. It also includes the option to reduce sampling rate by performing decimation on the data flow. The 16-bit dual interpolating DAC consists of two data channels that can be operated independently or coupled to form a complex. The chip features include a selectable 2x/4x/8x interpolation filter, an Fs/2, Fs/4 or Fs/8 digital quadrature modulation with image rejection, a direct IF mode and a programmable channel gain and offset control.

This module is also populated with 32MBytes NtSRAM memory which allows a ‘pattern generator’ function where a pattern (or periodic frame) is stored into the memory, read back continuously and send to the DAC. This configuration allows to board to work as a periodic generator in stand-alone mode. In this way, SMT370 works as a loadable Arbitrary Waveform Generator (AWG) and this mode is used for demonstration purposes. The board offers the possibility to output data in either two’s complement or binary format. It is also possible to output a 16-bit counter on each SHB half for system testing purpose as it then becomes easier to detect any missing data.

The communication between SMT370 and SMT365 is done at two levels. The first level corresponds to the programming and control of SMT370 done via comports while second level refers to transmission of data between the modules which is done at higher speed via SHB interface.

2.4 SMT49 – IF/RF Front-end Module

SDR platform of WHERE is completed with the introduction of SMT349, corresponding to IF/RF front-end module located in third TIM slot. This single width TIM completes the transmission and reception paths of digital radio system and its main features include:

- Xilinx Virtex-II FPGA (XC2V1000-4)
- Two SHB connectors
- Two comports,
- 50-Ohm analogue RF/IF inputs and outputs and external clock via MMBX connectors,

The analogue section of SMT349 includes two RF transceiver modules, operating in the 2.4 GHz ISM band. The up conversion from the 70MHz IF to the 2.4 GHz is done in two stages. The first stage converts the 1st IF to 374 MHz, while the second converts it to the RF frequency. Down-conversion approach follows the opposite procedure converting RF frequency to 374MHz and than in the second stage to 70MHz. The RF centre frequency of both transceivers is controlled by one synthesizer which is set by the FPGA. The FPGA also controls the AGC, TX power and TX/RX switch for each of the two IF/RF sections.

Technical specifications for the IF/RF part are:

- Input signal filtered by 1st IF tuned to 70MHz ± 8MHz,
- 70Mhz BPF characteristics
  - -1dB → +/-8 MHz
  - -20dB → +/-12 MHz
  - -50dB → +/-15 MHz
- 70MHz IF is converted to a 2nd IF of 374 MHz
- RF output signal is in the 2.4–2.5 GHz ISM band,
- Transmitter gain control done using 31dB at 1dB steps
- RF input signal is in the 2.4–2.5 GHz ISM band,
- Receiver gain control done using 2x31dB at 1dB steps
- IF output signal is at 70MHz ± 8MHz

3. SOFTWARE FEATURES

Due to complex nature of software controlling the described SDR platform, the logical way would be to classify it into various sections depending on the interface and required debugging information. For example, the GUI is done in Labview since it offers flexible interface and rapid memory access favorable for data graphic presentation. More on, four wireless interfaces, whose localization skills are to be explored, are

developed and tested in Matlab before passing them on to C and finally the last step is to implement the interfaces inside SMT365 module which is achieved by means of 3L Diamond IDE and Code Composer Studio.

The execution of entire software package begins with program loader developed in Visual C, that establishes a contact with the carrier board, and loads the application into the root DSP. The application is previously developed in C and debugged under 3L Diamond environment directly on SMT365 root module. The purpose of this application is to start and control the entire hardware initialization process and consequently prepare the platform for corresponding signal processing. The platform initialization includes DSP boot-up, configuration of ADC/DAC of the SMT370, and of the IF/RF parameters of SMT349. The configuration is done from the root DSP through the corresponding comport connections available on the SMT310Q board. After the initial parameters are set, a signal pattern is generated at DSP and transmitted to SMT370 via SHB connection. It is than stored in the local memory of SMT370 module. Since the module is configured as a periodic generator, this pattern is read back continuously and sent to the DAC.

At this point the loader execution on the host side is terminated, and the GUI in Labview takes over the control. The communication between Labview and DSP on the carrier board is done by means of dll library, also developed in Visual C. This library is in fact a two-way interface as DSP receives the expected number of samples, sampling frequency etc. from the Labview, while it transmits the received AD samples, calculated location parameters, control status etc. in the opposite direction.

This analog output of DAC converter is connected via MMBX-MMBX coaxial cable with the SMT349 module where FPGA than routes the data through the transmission RF chain. On the receiver side (which can be implemented on the same carrier board) the RF signal received by the antenna is guided through RF chain via on-board FPGA. The base-band signal is than passed with via another MMBX-MMBX coaxial cable to ADC of SMT370 and is afterwards routed to DSP via second SHB connection.

4. PARAMETER MEASUREMENT PROCEDURE

The main objective of the measurement scenario is to provide real data which is to be used in WHERE project for different signal exploration, namely hybrid data fusion, tracking, cooperative positioning and estimation of location dependent channel information. The data will be available under

the form of empirical likelihood functions for location dependent magnitudes, namely:

- Received signal power
- Time of arrival
- Angle of arrival

Thus, the empirical likelihoods $p(\theta \mid x,y)$ will be measured, where θ is any of the above magnitudes and *(x,y)* is the position on a rectangular grid within the measurement space. Once the experimental setup is defined the likelihoods associated to several specific air interfaces will be estimated. In this case the kind of modulation and the bandwidth impose restriction on the accuracy of the measurement that combine with the environment and variability to yield the final likelihoods. Two multicarrier interfaces that are implemented are: 802.11 (OFDM in general), 802.11g (WiFi). In addition two more wireless interfaces, namely: 802.15.4 (ZigBee) and 802.15.4a (CSS – Chirp Spread Spectrum) are also supported.

Because the resulting data are to be used for the development and analysis of cooperative positioning techniques, the likelihoods are measured pairwise. That is to say, given a grid position *(x,y)* there is a different empirical likelihood for every possible position of the transmitter on the same grid. In fact the measured likelihoods are $p(\theta \mid \mathbf{r},\mathbf{r}_i)$, where $\mathbf{r}$ and $\mathbf{r}_i$ are the position vector of a generic grid point and the position vector of the transmitter respectively.

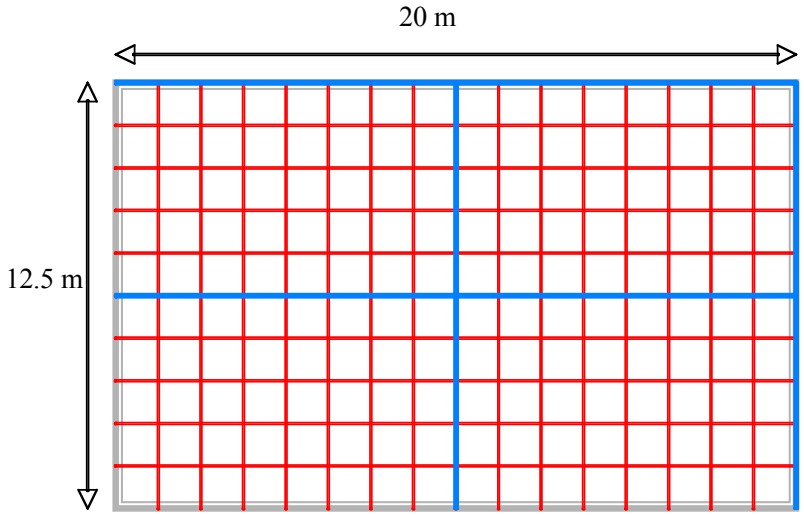

Figure 3. Measurment grid where transmitter positions are shown in blue and receiver positions are in red.

Assuming that the measurement space is a rectangular area, as shown in Figure 3, with sides of 12.5m and 20m respectively, and assuming a grid of step 1m, the number of grid points in the space is very large (more than 31000). For this reason the number of measured pairs is reduced. However, in order to be able to use the obtained measurements for the cooperative positioning we will restrict the position of the transmitters to be on grid point situated on two sides of the perimeter (major and minor sides) and along the two middle lines of the area. This way, for the example shown on Figure 3, the resulting number of pairs is reduced to 5625.

At the time the measurements are taken, the plan is to use the optimal measurement procedures and ad-hoc methods specifically developed for signals supported by the analyzed wireless interface standard. For optimal procedures the synchronization is assumed to be perfect. In this case the two platforms are used, one as a transmitter and another as receiver, and the synchronization between the platforms is achieved via cable.

5. CONLUSIONS

The described SDR platform used in the scope of WHERE project is based on the commercial hardware developed by Sundance. As such it is not intended for ranging purposes and the expected precision of localization results is limited. However, the advantage is the software flexibility the platform offers as well as the scalable hardware system configuration which can be easily expanded if necessary. The platform is implemented for exploring the localization possibilities of two multicarrier wireless interfaces, namely: 802.11 (OFDM in general), 802.11g (WiFi). Two additional wireless interfaces are alo explored: 802.15.4 (ZigBee) and 802.15.4a (CSS – Chirp Spread Spectrum). The measurements will take place in short range LOS situation in the typical indoor office of around 250 square meters.

Acknowledgment

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REFERENCES

[1] Sundance Multiprocessor Technology, www.sundace.com
[2] WHERE project, http://www.ict-where.eu/