MIMO PROTOTYPING TEST-BED WITH OFF-THE-SHELF PLUG-IN RF HARDWARE

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ABSTRACT

In this contribution we describe the current state of our Multiple-Input Multiple-Output (MIMO) test-bed, which employs a 2-antenna transmitter and a 4-antenna receiver in the so-called "offline" mode, where pre-processed data is transmitted over-air and logged for later processing. The receiver admits 512 MBytes of memory per receive antenna and a sampling frequency of a maximum of 100 MHz, which results in a logging time of 2.68 s with 14-bit resolution. The test-bed is based on Sundance's modular digital signal processing platform [1] and plug-in Radio Frequency (RF) components manufactured by Mini-Circuits [2]. With help of the plug-in approach a basic, modular and low-cost transmitter and receiver MIMO RF Front-end for the 2.4 GHz ISM-Band can be built up.

1. INTRODUCTION

For more than a decade multiple antenna systems have been an important field of communications research. MIMO is seen as a key technology to fulfill the high data-rate demands of current and future wireless communications systems, without occupying additional signal bandwidth. For this reason MIMO techniques are under discussion for current and for emerging communication standards like IEEE 802.11n, IEEE 802.16 and 3GPP HSDPA.

The advances in theoretical MIMO algorithm research are often based on simplified models of reality, which can be validated by employing dedicated test-beds, demonstrators and prototypes for assumption-free testing. Thereby more insight into the practical challenges of an algorithm or approach can be achieved [3].

Our first MIMO test-bed (STARS[1]) for the 2.4 GHz ISM-band was developed starting in 2003 and exhibited at EUSIPCO 2004 in Vienna. A description also including our educational project (a 2×2 MIMO test-bed employing acoustical transmission) can be found in [4].

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In this contribution we describe the current state of our new MIMO test-bed (Fig. 1) - called STARS[2] - for the 2.4 GHz ISM-band [5], which aims to assist the research by admitting flexibility in signaling. The test-bed is not dedicated to a special communication standard so that different signaling schemes (OFDM, CDMA, SC-FDE) and a 3-dB signal bandwidth up to 30 MHz can be studied. In order to allow a common and easy use of the test-bed a Graphical User Interface (GUI) and MATLAB integration are embedded. This permits the researcher to replace his or her modeled channel by the realistic one offered by the test-bed. This will of course require realistic assumptions concerning synchronization and channel knowledge.

Fig. 1. 4-Antenna Receiver of the STARS2 Test-bed Mounted on a Trolley.

Due to the fact that there is no MIMO RF front-end available on the market yet, it is a common challenge for all test-bed developers to built one. In this contribution we present our solution for when costs and efforts are limited.

In section 2 the architecture of the digital part of the test-bed and the general DSP software flow is described. The implementation of the RF front-ends is depicted in section 3. Here also the implementation and characteristic of self-designed Band Pass Filters (BPF) are reported, which are used to reject image bands. First system tests are described in section 4. These tests cover a validation of the signal bandwidth and a frequency offset analysis. A conclusion with a foreshadowing of the next project phases finishes this contribution in section 5.

2. DIGITAL PART OF THE STARS^2 SYSTEM

2.1. Setup of the Digital Hardware

The digital platform consists of processing modules for signal conversion (analog-to-digital and vice versa) and digital signal processing by Texas Instruments Digital Signal Processors (DSP) and/or Xilinx Field Programmable Gate Arrays (FPGA), so that the user can step-wise improve the test-bed in terms of real-time processing and processing power. In this contribution we review our so-called "offline" MIMO system or hardware-in-a-loop MIMO system, where pre-processed data is transmitted over-air and logged by the receiver for later analysis with help of MATLAB. Because of the modular nature of the platform, it is possible to introduce real-time processing blocks step-by-step.

Such real-time processing can be added with the help of Sundance's signal processing modules which are based on XILINX Virtex II or Virtex II-pro FPGAs and/or Texas Instruments' TMS320C6416 DSPs.

In addition, it is possible to build up additional systems (e.g. users, interferers, measurement stations in other rooms). Note, that in the case of an offline system it is not possible to have a cooperation/feedback between transmitters and receivers, or between the users. This will require real-time processing, which will be in focus for the next project phases.

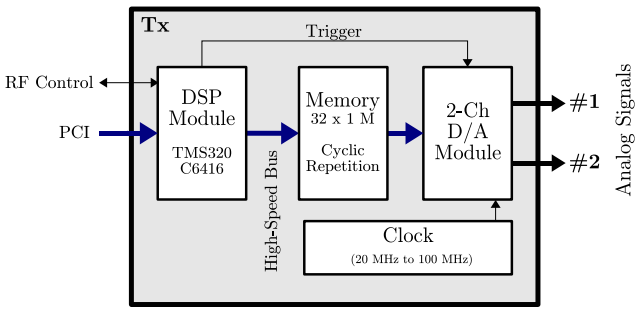


Fig. 2. Digital Part: Transmitter with Two Antennas.

In Fig. 2 the setup of the digital part of the 2-antenna transmitter is presented. A TMS320C6416 DSP is used for setup, host communication and system control. The DSP loads pre-processed data to a 1 M $\times$ 32-bit memory. The 2-channel Digital-to-Analog Converter (DAC) forms the analog Intermediate Frequency (IF) signals (#1, #2) by repeatedly reading data from the data sequence inside the memory. The maximum conversion rate is 160 Mega Samples Per Second (MSPS) with 16-bit resolution. A trigger signal controlled by the DSP is used to start or stop the DAC.

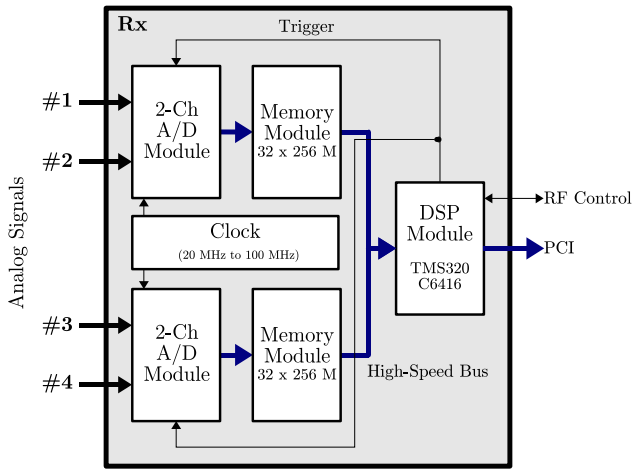


Fig. 3. Digital Part: Receiver with Four Antennas.

The digital part of the 4-antenna receiver is sketched in Fig. 3. Here two modules with two Analog-to-Digital Converters (ADC) are used. The ADCs can sample at up to 100 MHz and offer a resolution of 14-bits. A common sampling clock and a trigger controlled by the DSP is deployed to ensure synchronous sampling. The digital output signals of the four ADCs are stored in two large memory modules each of size 1 GByte (256 M $\times$ 32 bit). The dedicated Sundance High-speed Bus (SHB) employed between a single 2-channel A/D module and one memory module is able to transfer 32-bit data by a 100 MHz clock (400 MBytes/s), so that the received data can be stored in real-time. After data logging the DSP can read out the memory module's contents and transfer it to the host-PC, without being forced to meet the real-time requirement of the previously performed over-air communication. The logged data is stored in binary files, which can be analyzed with the help of MATLAB.

Due to the 'offline' processing approach, it does not matter to the digital part of STARS^2 which kind of signaling scheme is used. The bandwidth of the processible signals is limited only by the chosen conversion rates of the ADC/DAC (Nyquist criterion) and by the specification of the external RF hardware.

The digital part provides the following interfaces to external hardware: An external Trigger Output (LVTTL) is directly controlled by the DSP. This trigger is used to ensure a

synchronous start-up of the multiple A/D modules of the receiver. It is also used to control the D/A module. It is possible to share one trigger signal between transmitter and receiver, which will yield time synchronous operation of transmitter and receiver. A common sampling clock can be fed in as well. The trigger outputs, trigger inputs and sampling clock inputs are accessible via SMA connectors mounted on a PCI-slot plate. A digital 3- or 4-wire bus and additionally LVTTL I/O can be provided, if they are required by external hardware.

2.2. Software

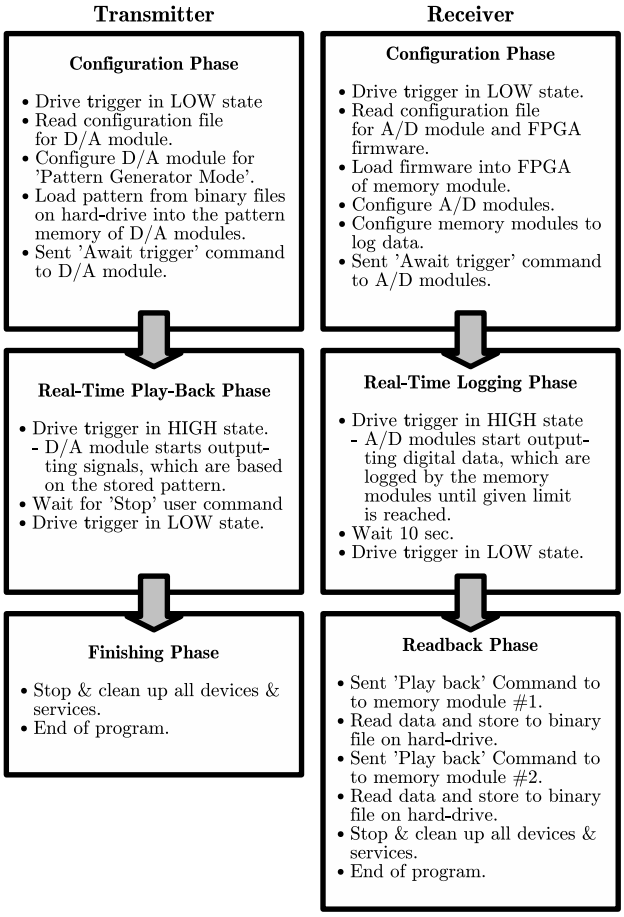


Fig. 4. Software Flow of STARS^2 Transmitter and Receiver.

In Fig. 4 the software flow of the transmitter and receiver program running on a TI TMS320C6416 DSP is given. As can be seen the DSP only used for system initialization, control tasks and host communication. Additional (real-time) signal processing can be deployed, if required. The software is based on the Real-time Operating System 3L Diamond 3.0 and programmed in the C programming language.

The software flow of the transmitter can be separated into three phases: The first one is the *Configuration Phase*. The trigger output signal is driven in 'Low' state and the D/A module is configured in 'Pattern Generator Mode' corresponding to a configuration file stored on the host-PC. Afterwards the pattern is loaded from a binary file, which has the filename as given by the configuration file. In this mode the D/A module will repeatedly read out its memory and convert the stored pattern into an analog signal. At the end the D/A module is started and will wait for the trigger 'High' event. The second phase is the *Real-Time Play-Back Phase*. The trigger output signal is driven to a 'High' state, so that the D/A module will start playing back the pattern. The DSP software will wait for a user command to stop the play back by driving the trigger output to 'Low'. The third phase is the *Finishing Phase*, where all devices and services of the STARS^2 are stopped and the system is cleaned up.

The software flow of the receiver can be separated into three phases: In the first phase, the *Configuration Phase*, the trigger output signal is driven to a 'Low' state. Afterwards the DSP reads the configuration file for the A/D module and the FPGA firmware for the memory module. Then the firmware is loaded into the memory module's Virtex II-pro and the A/D modules are configured. The memory modules are configured to log data until a given limit of samples is reached. The second phase is the *Real-Time Logging Phase*. The trigger output signal is driven to 'High' state, so that the A/D modules will start outputting digital samples to the SHB. The memory modules will log these samples until the given limit is reached. The DSP software will wait for 10 sec and will then stop the A/D modules by driving the trigger output signal to 'Low'. The third phase is the *Readback Phase*, where the DSP reads out one memory module after another and store the data into binary files on the hard-drive of the host-PC. At the end of this phase all devices and services of the STARS^2 are stopped and the system is cleaned up.

The used binary file formats can be accessed by functions developed for MATLAB, which allow reading back parts of the large binary files and an economical usage of the PC memory. The toolset also includes the implementation of DUC and DDC, so that the user can deal with (over-sampled) base-band signals as well. The configuration of the STARS^2 system is done with the help of a Graphical User Interface (GUI) developed in Visual C++, which allows for ease of use.

3. PLUG-IN MIMO RF HARDWARE SOLUTION

3.1. Transmitter & Receiver Front-end Setup

The setups of the RF front-ends at the transmitter and at the receiver are given in Fig. 5 and Fig. 6, respectively. The analog output/input signals of the digital part are assumed to be at a low IF of 10 MHz - 30 MHz, so that according to the used filters a 3-dB signal bandwidth of up to 30 MHz is possible.

The choice of the IF is a trade-off between required sam-

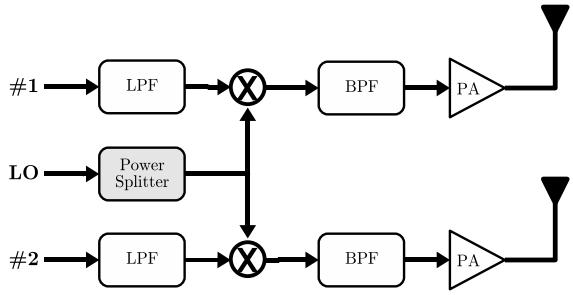


Fig. 5. Analog Part: Transmitter Front-End with Two Antennas (Low Pass Filter (LPF): SLP-30, Frequency Mixer: ZX05-C42LH, Power Amplifier (PA): ZVE-8G, Power Splitter: ZX10-2-42).

pling frequency, base-band signal bandwidth, implemented analog filters and required image rejection.

The transmitter front-end performs the up-conversion to the 2.4 GHz ISM-Band and the receiver front-end performs the down-conversion to the used IF. The conversion from or to the base-band is performed in the digital domain by pre- and post-processing respectively. Both front-ends are based on plug-in RF components manufactured by Mini-Circuits [2], which allows for a basic, modular and low-cost transmitter and receiver MIMO RF front-end. A MIMO Automatic Gain Control (AGC) unit is under development, but is faced with interfacing challenges due to the required examinations of the multiple Received Signal Strength Indicators (RSSI) by the digital part.

A common Local Oscillator (LO) for the antenna branches is obtained with the help of power splitters. The LO is generated with the help of an adjustable signal generator. For first carrier frequency offset free measurements, a common LO and a common sampling clock can be shared between transmitter and receiver. The common sampling clock is required due to the usage of Digital Up Conversion (DUC) to the IF and Digital Down Conversion (DDC) to base-band.

Without Band Pass Filters (BPF) the RF front-ends employ a Double Side Band (DSB) modulation, yielding an inherent frequency diversity gain at the cost of spectral efficiency. Note that the system is already band-limited because of its components, so that BPFs in a first step are not mandatory. Nevertheless, in order to obtain a Single Side Band (SSB) modulation sharp BPFs are required at the transmitter- and the receiver-side. At receiver-side the BPFs act as Image Reject (IR) filters. Unfortunately such filters are not easy to obtain on the market, so we decided to design a sharp BPF filter in micro-strip by ourselves. An alternative is of course the usage of an IR-Mixer, but they are typically designed for an IF of 70 MHz.

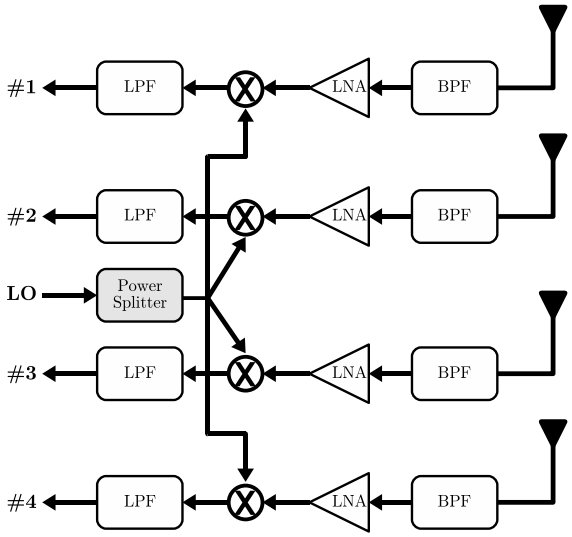


Fig. 6. Analog Part: Receiver Front-end with Four Antennas (LPF: SLP-30, Mixer: ZX05-C42LH, Low Noise Amplifier (LNA): ZX60-2534M, Power Splitter: ZX10-4-27).

3.2. Bandpass-Filter Development

Design aim for the BPF is to use the upper part of the 2.4-2.5 GHz ISM-Band and to filter out the lower image sideband as good as possible. To completely reject the lower image of the transmitted signal, a sharp edged band pass filter (BPF) is needed. Note, that we can freely adjust the LO frequency provided by a signal generator and can also adjust the used IF to some extent.

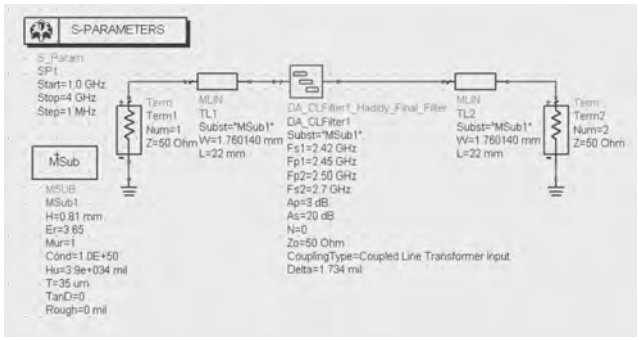


Fig. 7. Schematic View of the Layouted BPF.

We used Agilent Technologies' Advanced Design System (ADS 2005A) in the design and simulation of that BPF. ADS provides circuit (schematic) and electro-magnetic (Momentum) simulation technology that offer good performance in capacity, accuracy, speed and convergence.

The BPF is designed as Coupled Line Filter (CLF), which provide a high performance of the bandpass frequency response between the input and the output port. In Fig. 7 a screenshot of the layout of 4 coupled-line sections is shown,

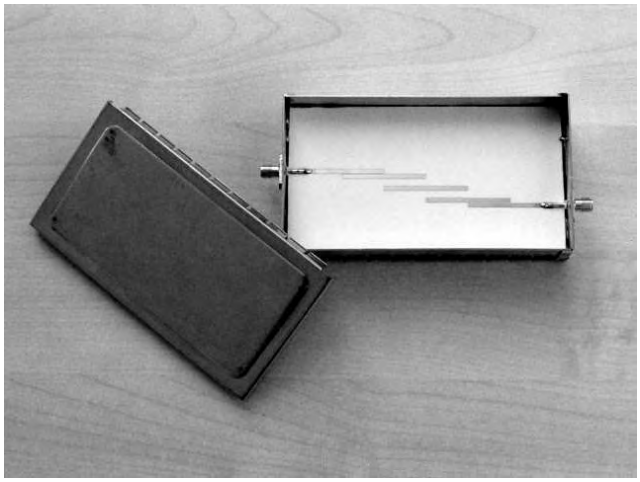


Fig. 8. Photo of BPF Designed in Micro-Strip Technology.

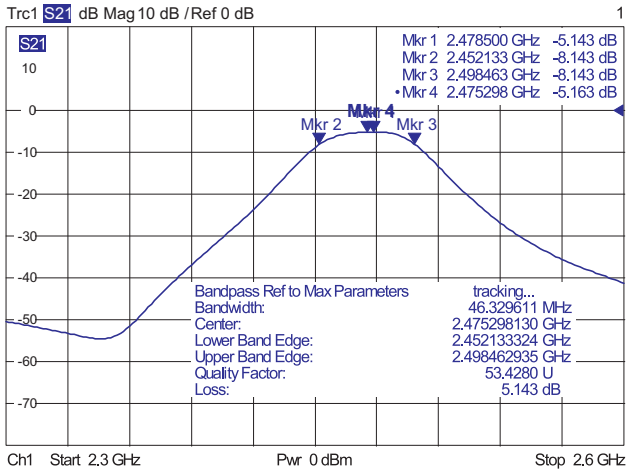


Fig. 9. Self-designed Band-Pass-Filter.

which produce a 3rd order filter response. An additional number of sections can be used to steepen the transition band roll off or to widen the pass bandwidth. Note, that the number of required filter sections is computed from the required frequency and attenuation informations.

The BPFs are realized using RO4003C substrate material manufactured by Rogers Cooperation with a dielectric constant $\epsilon_r = 3.65$ and a substrate height of 0.81 mm. The BPF is soldered into a metal box and SMA connectors are used to connect the two ports of the filter (Fig. 8).

In Fig. 9 the measured power spectrum of one of the self-designed BPF is given. The BPF has a 3-dB bandwidth of 46.3 MHz, the lower 3-dB corner frequency is approx. 2.4521 GHz and the upper one is approx. 2.4984 GHz. The insertion loss is around 5.15 dB.

In order to sharpen the characteristic we cascaded two of the BPFs. The resulting power spectrum is presented in Fig. 10. The two cascaded BPFs have a 3-dB bandwidth of approx.

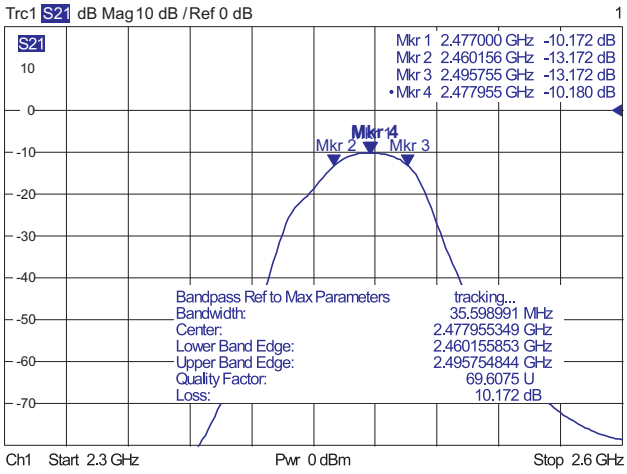


Fig. 10. Two Cascaded Self-designed Band-Pass-Filter.

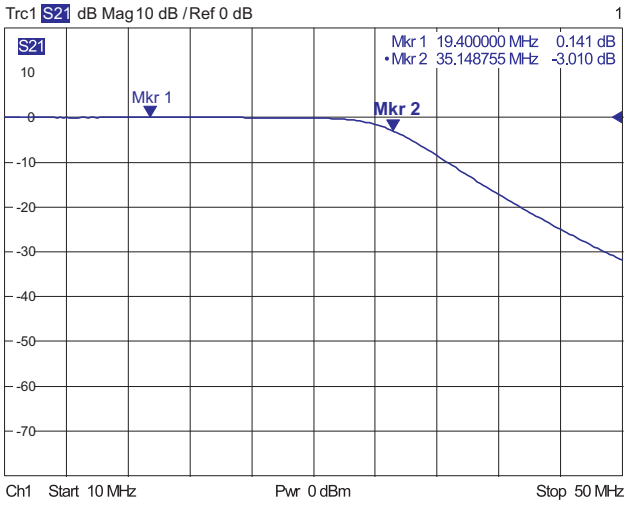
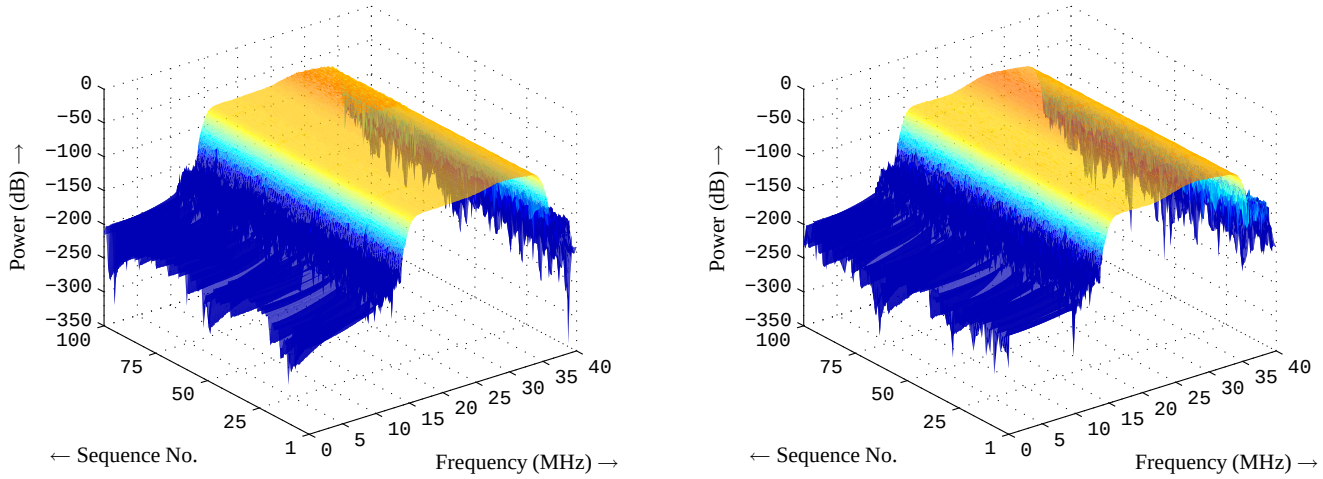


Fig. 11. Low-Pass Filter of Type MiniCircuits SLP-30.

35.6 MHz, the lower 3-dB corner frequency is approx. 2.4601 GHz and the upper one is approx. 2.4957 GHz.

We use two cascaded BPFs per antenna at transmitter-side to ensure a minimal distortion of other services in the ISM-Band and in the bands above. At the receiver-side we only use one BPF per antenna in order to reject the image band.

In Fig. 11 the measurement of the power spectrum of MiniCircuits' SLP-30 LPF is shown. This filter is used as an anti-aliasing filter at the ADC inputs. The SLP-30 filters are also placed at the DAC outputs to suppress any spurious signals. The 3-dB corner frequency is approx. 35.1 MHz and the insertion loss is 0.141 dB.



(a) Antenna 1

(b) Antenna 2

(c) Antenna 3

(d) Antenna 4

Fig. 12. Power Spectra of the Sampled Received IF Signals.

4. FIRST SYSTEM TESTS

4.1. System Bandwidth Test

The aim of this test is to verify the system bandwidth and the linearity of the hardware. Therefore a signal with a constant envelope in the time domain and a constant magnitude in the frequency domain is preferable, because effects become directly visible by looking at the power spectrum of the signal. The on-air transmitted signal can be verified with the help of a spectrum analyzer directly connected to an antenna. The samples of the received signal can be evaluated with the help of the logging functionality of the STARS[2] test-bed.

In the case of channel sounding these signals are often referred as *Chirp*, because they usually start with low frequencies and end up with high frequencies.

A basic sequence like that can be given by

$$c(n) = \mathrm{e}^{\mathrm{j}2\pi\theta(n)}, \tag{1}$$

with $n = 0, 1, ..., L-1$.

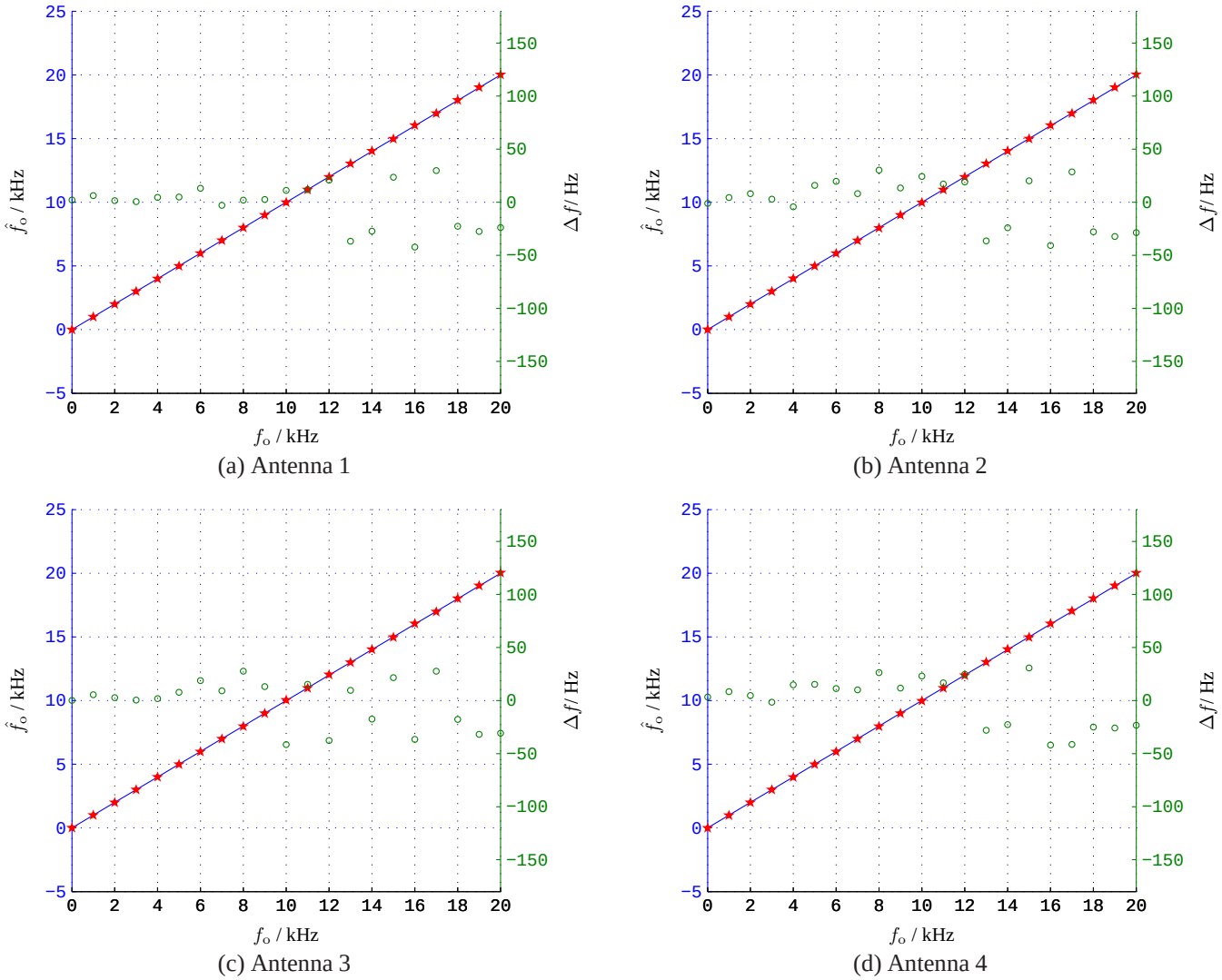
We will use so-called Chu-Sequences [6], where $\theta(n)$ is generated by

$$\theta(n) = \frac{n^2}{2L}. \tag{2}$$

For convenience we here restricted the sequence to be of even length L.

The Chu-Sequence shows good autocorrelation properties, so that one can also obtain insight into the time-domain behavior, with the help of a *Matched Filter*(MF) approach. The power of the MF output can be seen to some extent as a Power Delay Profile (PDP).

In Fig. 12 the power spectra of the sampled IF signals for the antennas 1 to 4 are given. The Chu-Sequence was



(a) Antenna 1 (b) Antenna 2

(c) Antenna 3 (d) Antenna 4

Fig. 13. Frequency Offset Estimation Results. Left-Hand Axis: Estimated Frequency Offset (Stars), Ideal Estimation (Solid Line); Right-Hand Axis: Estimation Error (Circles).

transmitted by one antenna, where the length of the base-band sequence is $L = 256$, the base-band rate is $f_{\mathrm{bb}} = 20$ MHz, the conversion rate for DAC /ADC is $f_{\mathrm{s}} = 80$ MHz, and the IF is $f_{\mathrm{IF}} = 25$ MHz. Note, that we already applied a digital BPF to suppress frequencies below 11 MHz and above 39 MHz. The digital BPF is chosen to be wider than required, to give insight into the received SNR. The obtained results for transmit antenna 1 and antenna 2 are very similar, such that we only present the results obtained with transmit antenna 1.

4.2. Frequency Offset

In a typical wireless communication system, imperfect up- and down-conversion caused by non-idealities in the transmitter and receiver local oscillators (LO) result in a frequency offset at the receiver. This offset causes a continuous rotation of the signal constellation, and must be corrected for reliable demodulation of the received signal. This frequency offset test aims to obtain the frequency offset between our transmitter and receiver, and it is also a good example to use for our platform to verify the performance of an algorithm in a real system. Furthermore, from this test we can investigate the frequency offset behavior of the four receiver branches.

In this test we apply the signal structure described in the Wideband Code Division Multiple Access (WCDMA) standards and use the system model and the algorithm as given in [7]. The transmit signal contains a Primary Synchronization Channel (PSCH) and the Primary Common Pilot Channel (pCPICH).

The signals are transmitted by one antenna and received

by four antennas. The chip rate is 3.84 MHz, the sampling rate for DAC/ADC is $f_{\mathrm{s}} = 76.8$ MHz and the intermediate frequency $f_{\mathrm{IF}} = 28$ MHz. We use a common LO and a common sampling clock for both transmitter and receiver to generate a fully frequency synchronized system for verifying the performance of the proposed algorithm. A frequency offset can be added in the digital down-conversion stage of the receiver post-processing. This allows for use of the same measured data set, so that the channel will be the same for all offset settings. For instance, because the intermediate frequency f_{IF} of the transmitter is 28 MHz, we can get a 1 kHz frequency offset by setting the IF used in the digital down-converter of the receiver to 27.999 MHz.

In Fig. 13 the estimated values versus the setting values for the four receive antennas are given and the estimation errors are shown at the same time. It shows that the algorithm is capable of covering the range of 20 kHz frequency offset and the estimation errors in this whole range are less than 50 Hz, as expected in [7]. From this test result it is also proved, that the frequency offset of the four receive antennas is, except for an estimation error, the same.

5. CONCLUSION

The current state of the STARS^2 test-bed allows us to study MIMO algorithms for different standards in an assumption-free manner, before going ahead with a real-time implementation. The pre- and post-processing approach allows for fast evaluation of approaches and the verification of theoretically derived algorithms. Real-time processing can be added step-by-step by placing FPGA/DSP modules into the system.

In addition, the modularity of STARS^2 allows for multiple users, which can act in an offline system as interferers or additional measurement stations. Cooperation between users or feedback between transmitters and receivers will require a full real-time processing implementation, which is indeed a challenging task.

The presented plug-in approach to build up RF Hardware, which is based mainly on off-the-shelf products, is especially useful, if costs and efforts are limited. The presented solution can be seen as a good starting point until 'true' MIMO transceiver Integrated Circuits (IC) are available off-the-shelf. Such ICs can be easily integrated to the STARS system by employing a 3- or 4-wire bus, as we have reported in [4].

In this contribution the first system tests and their results are reported. They verify the system-bandwidth and show up the required frequency synchronicity of all 4-antenna receiver branches.

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