Unit / Module Name:	Rocket Serial Link
Unit / Module Number:	RSL
Used On:	TIM Modules / Carriers
Document Issue:	1.3
Date:	08/09/2003

CONFIDENTIAL

Rocket Serial Link
Interconnection Standard

Outstanding Issues:

1) Sundance to provide additional information for Appendix A
2) Completion of Section 4 (MRV)
3) Completion of Section 5 (MRV)

Approvals		Date
Managing Director		
Software Manager		
Design Engineer		

Revision History

Date	Changes Made	Rev	Issue	Initials
02/05/03	**First release**	**01**	**01**	**MRV**
08/09/03	**General Updates to Document**	**01**	**02**	**MRV**
15/09/03	**Changed orientation of RSL Connectors**	**01**	**03**	**MRV**

List of Abbreviations

Abbreviation	Explanation
CDR	Clock and Data Recovery
FPGA	Field Programmable Gate Array
LVDS	Low Voltage Differential Signalling
MGT	Multi-Gigabit Transceiver
RSL	Rocket Serial Link
RSLCC	Rocket Serial Link Communications Channel
SHB	Sundance High-speed Bus
SI	Serial Interface
SMT	Sundance Multiprocessor Technology
TBD	To Be Determined

Table of Contents

Table of Figures

1 Introduction

1.1 Overview

The Rocket Serial Link (RSL) is a serial interconnection standard that is capable of data transfer speeds of up to 2.5GBit/s per serial link. Up to four of these links can be combined to form a Rocket Serial Link Communications Channel (RSLCC) that is capable of data transfer up to 10GBit/s.

Each RSL is made up of a differential Transmit and Receive pair. A single Rocket Serial Link is thus a full-duplex link and can transfer data at up to 2.5GBit/s in either direction at the same time. The transmission clock is recovered from the data stream, leaving the link as a fully independent communications link that requires no additional control or data signals.

The RSL standard is based on the RocketIO transceiver core found on Xilinx Virtex-II Pro FPGAs. These silicon integrated transceiver cores handle the serialization / de-serialization of the data stream as well as certain low level management functions.

This document describes various aspects of the Rocket Serial Link (RSL). It covers the mechanical specifications for the standard, including the connector types, position and pin-outs. It covers the electrical characteristics of the interconnection standard as well as certain standard VHDL building blocks.

The RSL specification defines all the aspects of how to interconnect Sundance modules in a standard way using the integrated RocketIO transceivers in the Xilinx Virtex-II Pro devices. The RocketIO transceivers are not limited for use with Sundance RSL compliant hardware only. These transceivers, with adequate physical layers, may be used form many different serial interconnection standards. These standards include RapidIO, Infiniband, Serial ATA and Gigabit Ethernet. For more information refer to the Xilinx documentation on RocketIO [1,2]

1.2 RSL Features

- Full Duplex Communication per RSL
- Data transfer at up to 2.5GBit/s *(To be confirmed by hardware characterization)* per RSL
- Grouping of up to four RSL to form a single 10GBit/s link
- Low Voltage Differential Signaling used
- Full clock recovery from data stream
- Compatibility with emerging serial interconnection standards

1.3 Related Documents

[1] Virtex-II Pro Datasheet, ds083.pdf – Xilinx

[2] RocketIO Transceiver User Guide, ug024.pdf - Xilinx

[3] SMT398-Pro Specification – Sundance.

2 Mechanical Specifications

2.1 Connector Type

The RSL connectors used on the TIM modules and Carriers are 0.8mm pitch differential Samtec connectors. Any single connector makes provision for a maximum of 14 differential pairs. The Samtec QSE-014-xx-DP and QTE-014-xx-DP type of connectors are used on both the TIM modules and the Carriers.

The following two diagrams show the Top View of the QSE and QTE type connectors.

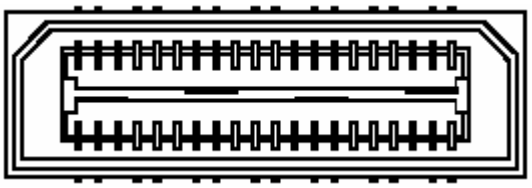

Figure 1 –RSL QSE-014-xx-DP Type Connector

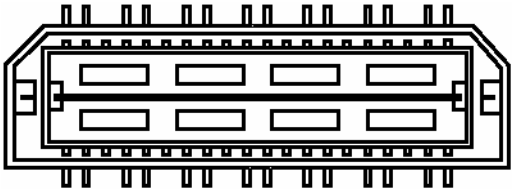

Figure 2 –RSL QTE-014-xx-DP Type Connector

Both connectors have a single pin omitted on either side of the connector after every second pin. This architecture creates 14 individual differential pairs in the connector with proper isolation between pairs. The connector also contains a solid integrated ground plain in the middle throughout the full length of the connector. This provides addition shielding to the differential pairs. The connector characteristics for a 5.03mm QSE/QTE connector stack is given in the following table:

Impedance Mismatch (Ohm)			Near End Cross Talk	
Period	**Impedance**		**Frequency**	**Percentage**
30 ps	111.6 to 88.0		6.40 GHz	~1.75%
50 ps	103.6 to 94.0		10.00 GHz	~2.0%
100 ps	98.8 to 98.2			
250 ps	100.0 to 99.6			

Figure 3 –QSE / QTE Connector Characteristics

The connectors are keyed to ensure correct insertion. The default QSE/QTE stacking height is 5.03 mm. The following stacking heights are also available: 8.03mm, 11.03mm, 16.00mm, 19.00mm, 22.00mm. The QSE connector always stays the same height. The QTE connector determines the stacking height.

The table underneath list the preferred TIM module and Carrier connector part numbers for a stacking height of 5.03mm. A description of which connectors are used where is provided in the following section.

No	Connector Description	Document Reference	Samtec Part Number
1	TIM and Carrier RSL Type A Connector	QSE-014-xx-DP	QSE-014-01-F-D-DP-A
2	TIM and Carrier RSL Type B Connector	QTE-014-xx-DP	QTE-014-01-F-D-DP-A

Figure 4 – Full RSL Connector Part Numbers

More information about the QSE-014-xx-DP or QTE-014-xx-DP connectors please visit the Samtec website.

2.2 RSL Connector Location

Unlike the SHB, the RSL signals are not bi-directional. To prevent inadvertent connection from Tx to Tx (and Rx to Rx), different connector genders with different signal assignments are used. There are two sets of signal assignments – RSL Type A assignments and RSL Type B assignments. When interconnecting RSL pairs RSL Type A must always interface to RSL Type B and visa versa. *The RSL Type A Connector is the Samtec QSE-014-01-F-D-DP-A and the RSL Type B Connector is the Samtec QTE-014-01-F-D-DP-A. It is however possible for similar connectors in the same group to have different pin-outs, depending on the connectors location.*

A single RSL is bi-directional. The RSL Type A signal group and the RSL Type B signal group thus contains a certain amount of bi-directional links each. RSL Type A links should not be confused as outputs only and RSL Type B links as inputs only.

2.2.1 RSL Compliant TIM Modules

On a TIM module the RSL connectors replace the optional second set of SHB connectors. Next to the SHB-A connector the RSL Type A connector is located. This connector is a QSE-014-xx-DP type connector. Next to the SHB-B connector the RSL Type B connector is located. This connector is a QTE-014-xx-DP type connector. These two connectors are located on the Top of the TIM Module and are ideal for module to module inter-connection. Identical connectors, but with a different pin-out, are located right underneath the RSL Type A and RSL Type B connectors. This set of connectors makes it possible to connect a RSL between a TIM module and a carrier without having to route the signals through a cable.

A Tim module thus contains two sets of two RSL connectors. Each set contains one connector on the Top of the module, and one on the Bottom of the module. The RSL Type A connector is a QSE type connector, and the RSL Type B connector is a QTE connector.

The following two diagrams shows the exact location of the RSL Type A and RSL Type B connectors on the Top and Bottom of a TIM module.

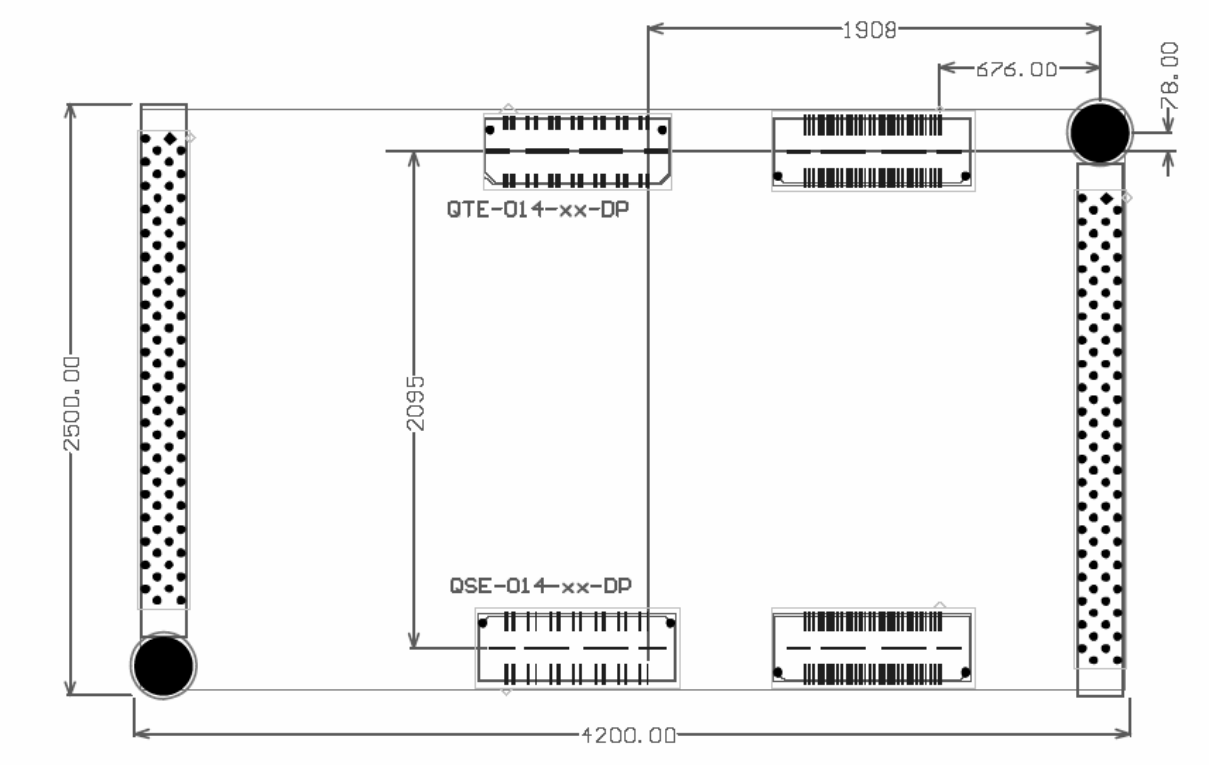

Figure 5 – Location of RSL Connectors on Top of TIM Module.

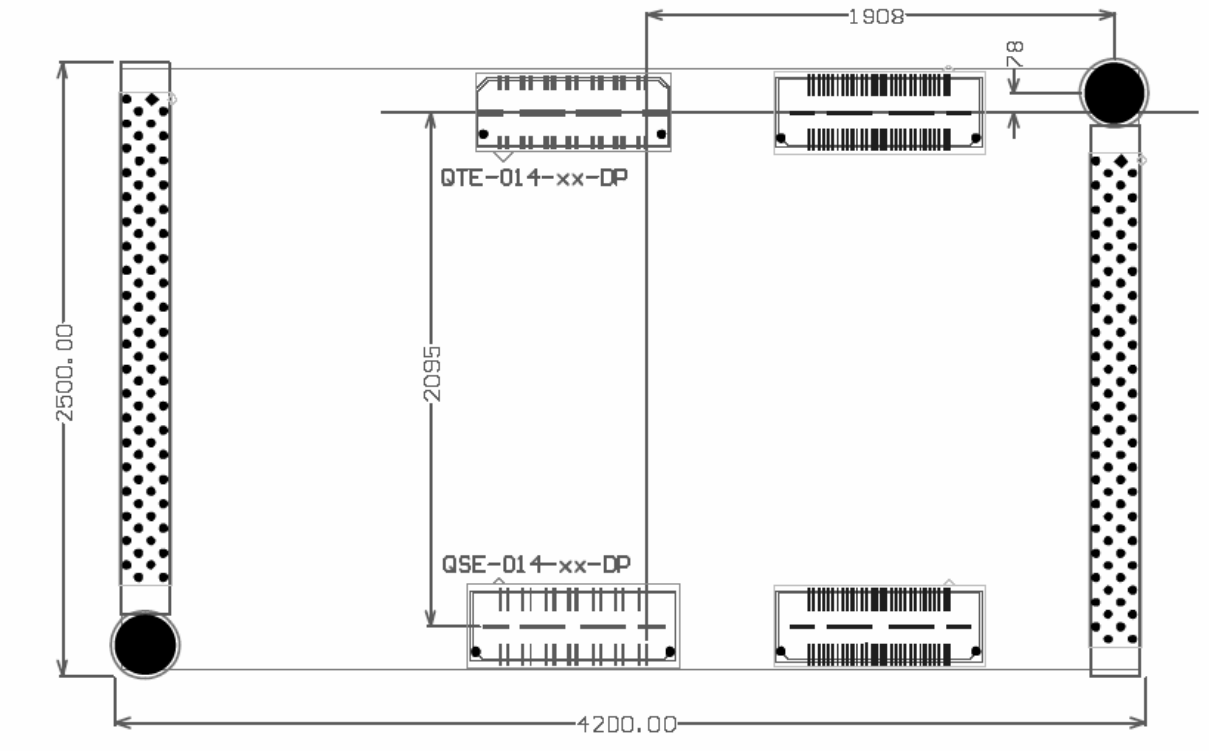

Figure 6 – Location of RSL Connectors on Bottom of TIM Module.

2.2.2 RSL Compliant TIM Carriers

All RSL compliant carriers contain only two RSL connectors per TIM site. One RSL Type B QTE connector to mate with the RSL Type A QSE connector on the TIM module, and one RSL Type A QSE connector to mate with the RSL Type B QTE connector.

The exact mechanics of the connector placement may vary from carrier to carrier. For this reason only a diagram depicting the location of the RSL Type A and B Connectors in relation to the TIM site is shown in the following diagram:

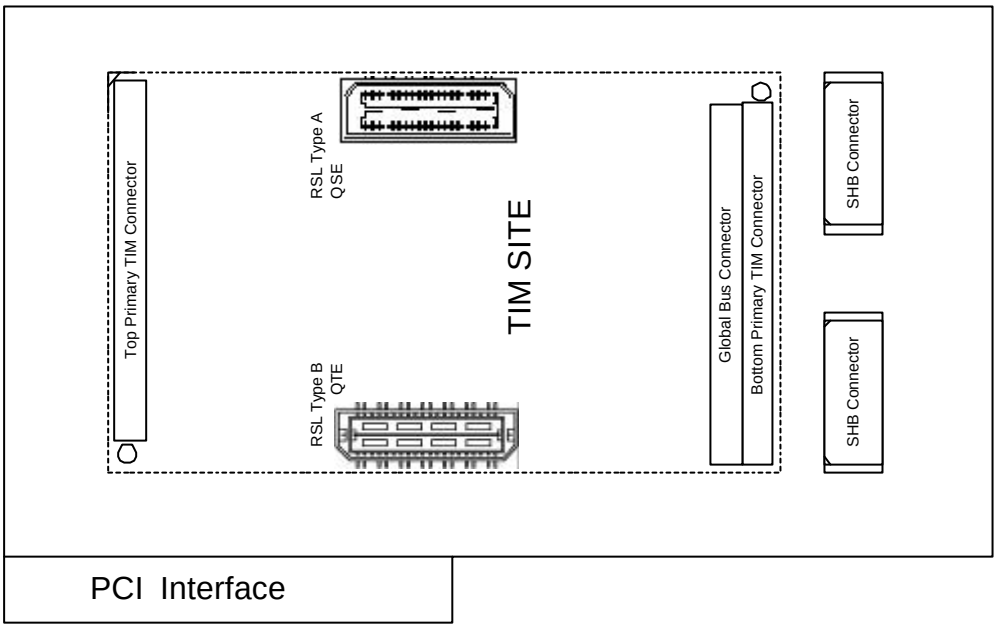

Figure 7 – Location of RSL Connectors on Carrier TIM Site.

Future RSL Compliant Carriers may expand the RSL standard to include industry standard connectors for interfaces such as RapidIO, SATA, Inifiband and Gigabit Ethernet. In general the design impact of conforming to one of the above mentioned standards is very small on the hardware side, but rather large on the firmware and software side. The Xilinx Virtex-II Pro RocketIO transceivers are compatible with the above mentioned standards.

2.2.3 Rigid Printed Circuit Boards

Rigid Printed Circuit Boards may be used to interconnect two adjacent TIM Modules. When two TIM modules are placed side by side the RSL Type A connector from the one module is adjacent to the RSL Type B connector form the other. The Rigid PCB thus provides a RSL Type A-to-Type B bridge between the two modules. The Rigid PCB contains a RSL Type B connector to connect to the Module RSL Type A connector and visa-versa. The routing on the PCB is a straight through 1 to 1 routing.

The two diagram on the following page illustrates this concept. The notation used to describe the location and type of connector is explained in the following section: *RSL Connector Type / Location.*

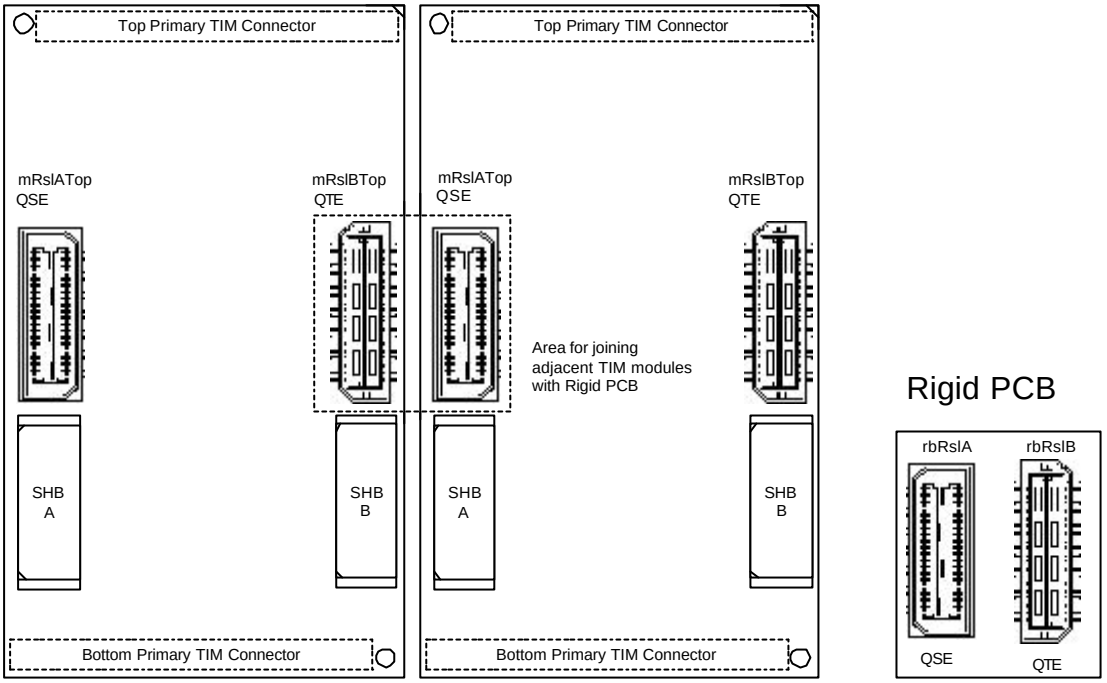

Figure 8 – Joining two adjacent TIM modules.

The above diagram illustrates the area for joining two adjacent TIM modules with a Rigid PCB. The diagram above illustrates the rigid PCB. Note that on the rigid PCB a RSL QSE Type B connector mates with the TIM module RSL QTE Type A connector.

2.2.4 Cable Assemblies

It is also possible to connect a RSL Type A connector to a RSL Type B connector using a high speed flexible cable with a QTE connector on the one side and a QSE connector on the other side. Like the rigid PCB the cable is a straight through 1-to-1 cable.

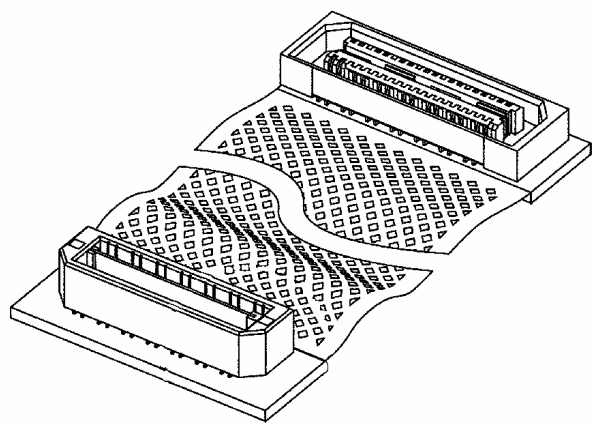

Figure 9 – RSL High Speed Data Link Cable.

The matching cable for the RSL Type A and Type B connectors is the Samtec High Speed Data Link Cable (HFEM Series). An illustration of this cable is shown the in figure above.

The cable comes in three lengths, measured from the outer edges of both connectors. These lengths are 76.2mm, 127.0mm and 242.32mm. The main characteristics of the cable are listed in the following table:

Insertion Loss			**Impedance (Ohm)**	
Frequency	**Loss**		**Frequency**	**Percentage**
500 MHz	-0.7 dB		Full Range	+/- 10%
1.0 GHz	-1.2 dB			
1.5 GHz	-1.3 dB			
2.0 GHz	-2.2 dB			
2.5 GHz	-2.2 dB			
3.0 GHz	-2.5 dB			
3.5 GHz	-3.4 dB			

Figure 10 – HFEM Cable Characteristics

2.3 RSL Connector Type / Location

The table underneath summarizes the connector type and connector location information. A unique identifier is assigned to each possible position. It is recommended that this identifier or similar identification appears in all RSL schematics to help with identifying the connector Type and Location.

No	Location	Description	Location	Identifier	Part Number
1	Carrier	RSL Type A Connector	TIM site on Carrier	cRslA	QSE-014-xx-DP
2	Carrier	RSL Type B Connector	TIM site on Carrier	cRslB	QTE-014-xx-DP
3	TIM Module	RSL Type A Connector	Top of TIM Module	mRslATop	QSE-014-xx-DP
4	TIM Module	RSL Type A Connector	Bottom of TIM Module	mRslABot	QSE-014-xx-DP
5	TIM Module	RSL Type B Connector	Top of TIM Module	mRslBTop	QTE-014-xx-DP
6	TIM Module	RSL Type B Connector	Bottom of TIM Module	mRslBBot	QTE-014-xx-DP
7	RSL Cable	RSL Type A Connector	Module-to-Module or Module-to-Carrier	icRslA	QSE-014-xx-DP
8	RSL Cable	RSL Type B Connector	Module-to-Module or Module-to-Carrier	icRslB	QTE-014-xx-DP
9	Module-to-Module Bridging PCB	RSL Type A Connector	Rigid Module-to-Module PCB	rbRslA	QSE-014-xx-DP
10	Module-to-Module Bridging PCB	RSL Type B Connector	Rigid Module-to-Module PCB	rbRslB	QTE-014-xx-DP

Figure 11 – RSL Connector Type and Position

The prefix in the Identifier column in the table above helps to identify and locate the specific RSL connector/location that is referred to. The following table summarizes the use of the prefix:

No	Prefix	Abbreviation For	Usage Example
1	‘c’	Carrier	cRslA = RSL Type A connector located on carrier
2	‘m’	Tim Module	mRslBTop = RSL Type B connector located on the Top of the module
3	‘ic’	Inter-connecting Cable	icRslA = RSLType A connector located on a module-to-module flexible cable
4	‘rb’	Rigid PCB	rbRslB = RSL Type B connector located on a rigid module-to-module interconnection PCB

Figure 12 – RSL Prefix Explanation

2.4 Connector Pin-outs

This section provides the pin-out definitions for the different RSL connectors. The pin-outs vary depending on the RSL Type and the connector location. Depending on the Carrier or TIM module configuration there will always the either four, eight or twelve links available. The amount of links are split over the RSL Type A and RSL Type B connector. So a module with four links will have two links on the RSL Type A connector and the other two on the RSL Type B connector. Remember that a link is made up out of four signals – a differential Tx pair and a differential Rx pair. The connector pin assignments for all connector locations and the amount of links per connector are provided in the tables in this section.

2.4.1 Naming Convention

Each table defines the signal direction as seen from the local perspective of that specific connector. So if the signal name on a RSL Type A connector on a TIM module reads as mRxLink0 it means that it is a signal that is received on the module and thus transmitted from a carrier. The following diagram clarifies this issue:

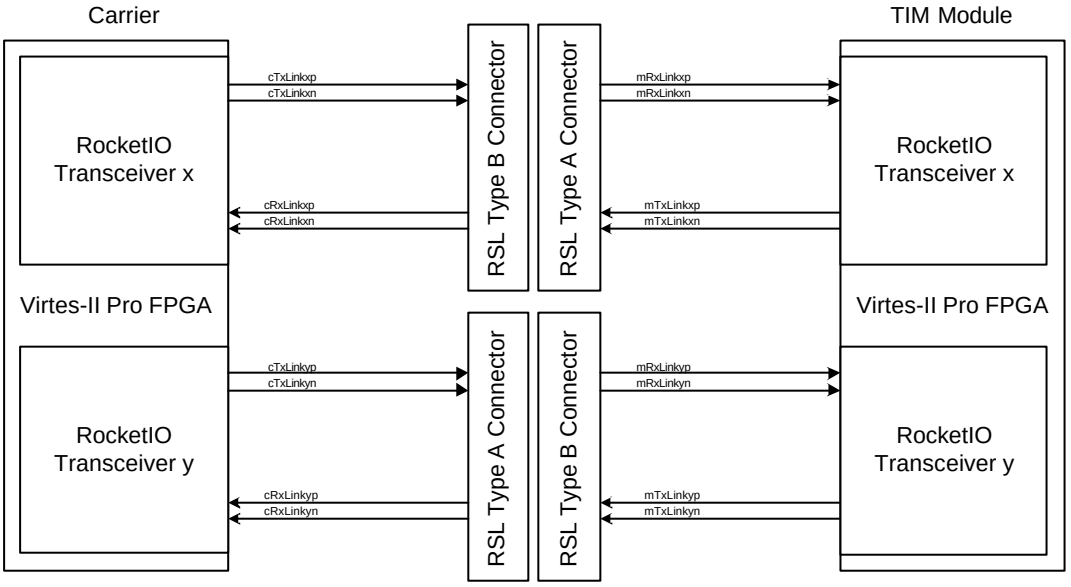

Figure 13 – RSL Naming Convention

The use of the prefix in the signal naming convention is explained in the section titled '*RSL Connector Type / Location*' earlier in this document.

2.4.2 Tim Module

The TIM module comes with the most possibilities. The RSL links are routed to an RSL Type A connector and an RSL Type B connector on the Top of the module. The same links are also routed to the same type of connectors underneath the module. This leaves the option open for connecting the links to a carrier, or to an adjacent TIM module. Please note that the links are not multi-drop links and that you can't be connected to a carrier and to another module at the same time. Depending on the size of the FPGA mounted on the module four, eight or twelve links are available. Even thought the same type of connector is used for the RSL Type A and RSL Type B groups on the Top and the Bottom of the module the pin assignments differ. The reasoning behind this is explained in the next section – Carrier Pin Assignments. The tables underneath list the pin-outs for all of these combinations.

2.4.2.1 RSL Type A, Top, 4 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mRxLink0p	Module Receive Link 0, positive	2	mTxLink0p	Module Transmit Link 0, positive
3	mRxLink0n	Module Receive Link 0, negative	4	mTxLink0n	Module Transmit Link 0, negative
5	mRxLink1p	Module Receive Link 1, positive	6	mTxLink1p	Module Transmit Link 1, positive
7	mRxLink1n	Module Receive Link 1, negative	8	mTxLink1n	Module Transmit Link 1, negative
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.2.2 RSL Type B, Top, 4 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mTxLink0p	Module Transmit Link 0, positive	2	mRxLink0p	Module Receive Link 0, positive
3	mTxLink0n	Module Transmit Link 0, negative	4	mRxLink0n	Module Receive Link 0, negative
5	mTxLink1p	Module Transmit Link 1, positive	6	mRxLink1p	Module Receive Link 1, positive
7	mTxLink1n	Module Transmit Link 1, negative	8	mRxLink1n	Module Receive Link 1, negative
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.2.3 RSL Type A, Top, 8 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mxLink0p	Module Receive Link 0, positive	2	mxLink0p	Module Transmit Link 0, positive
3	mxLink0n	Module Receive Link 0, negative	4	mxLink0n	Module Transmit Link 0, negative
5	mxLink1p	Module Receive Link 1, positive	6	mxLink1p	Module Transmit Link 1, positive
7	mxLink1n	Module Receive Link 1, negative	8	mxLink1n	Module Transmit Link 1, negative
9	mxLink2p	Module Receive Link 2, positive	10	mxLink2p	Module Transmit Link 2, positive
11	mxLink2n	Module Receive Link 2, negative	12	mxLink2n	Module Transmit Link 2, negative
13	mxLink3p	Module Receive Link 3, positive	14	mxLink3p	Module Transmit Link 3, positive
15	mxLink3n	Module Receive Link 3, negative	16	mxLink3n	Module Transmit Link 3, negative
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.2.4 RSL Type B, Top, 8 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mTxLink0p	Module Transmit Link 0, positive	2	mRxLink0p	Module Receive Link 0, positive
3	mTxLink0n	Module Transmit Link 0, negative	4	mRxLink0n	Module Receive Link 0, negative
5	mTxLink1p	Module Transmit Link 1, positive	6	mRxLink1p	Module Receive Link 1, positive
7	mTxLink1n	Module Transmit Link 1, negative	8	mRxLink1n	Module Receive Link 1, negative
9	mTxLink2p	Module Transmit Link 2, positive	10	mRxLink2p	Module Receive Link 2, positive
11	mTxLink2n	Module Transmit Link 2, negative	12	mRxLink2n	Module Receive Link 2, negative
13	mTxLink3p	Module Transmit Link 3, positive	14	mRxLink3p	Module Receive Link 3, positive
15	mTxLink3n	Module Transmit Link 3, negative	16	mRxLink3n	Module Receive Link 3, negative
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.2.5 RSL Type A, Top, 12 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mRxLink0p	Receive Link 0, positive	2	mTxLink0p	Transmit Link 0, positive
3	mRxLink0n	Receive Link 0, negative	4	mTxLink0n	Transmit Link 0, negative
5	mRxLink1p	Receive Link 1, positive	6	mTxLink1p	Transmit Link 1, positive
7	mRxLink1n	Receive Link 1, negative	8	mTxLink1n	Transmit Link 1, negative
9	mRxLink2p	Receive Link 2, positive	10	mTxLink2p	Transmit Link 2, positive
11	mRxLink2n	Receive Link 2, negative	12	mTxLink2n	Transmit Link 2, negative
13	mRxLink3p	Receive Link 3, positive	14	mTxLink3p	Transmit Link 3, positive
15	mRxLink3n	Receive Link 3, negative	16	mTxLink3n	Transmit Link 3, negative
17	mRxLink4p	Receive Link 4, positive	18	mTxLink4p	Transmit Link 4, positive
19	mRxLink4n	Receive Link 4, negative	20	mTxLink4n	Transmit Link 4, negative
21	mRxLink5p	Receive Link 5, positive	22	mTxLink5p	Transmit Link 5, positive
23	mRxLink5n	Receive Link 5, negative	24	mTxLink5n	Transmit Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.2.6 RSL Type B, Top, 12 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mTxLink0p	Module Transmit Link 0, positive	2	mRxLink0p	Module Receive Link 0, positive
3	mTxLink0n	Module Transmit Link 0, negative	4	mRxLink0n	Module Receive Link 0, negative
5	mTxLink1p	Module Transmit Link 1, positive	6	mRxLink1p	Module Receive Link 1, positive
7	mTxLink1n	Module Transmit Link 1, negative	8	mRxLink1n	Module Receive Link 1, negative
9	mTxLink2p	Module Transmit Link 2, positive	10	mRxLink2p	Module Receive Link 2, positive
11	mTxLink2n	Module Transmit Link 2, negative	12	mRxLink2n	Module Receive Link 2, negative
13	mTxLink3p	Module Transmit Link 3, positive	14	mRxLink3p	Module Receive Link 3, positive
15	mTxLink3n	Module Transmit Link 3, negative	16	mRxLink3n	Module Receive Link 3, negative
17	mTxLink4p	Module Transmit Link 4, positive	18	mRxLink4p	Module Receive Link 4, positive
19	mTxLink4n	Module Transmit Link 4, negative	20	mRxLink4n	Module Receive Link 4, negative
21	mTxLink5p	Module Transmit Link 5, positive	22	mRxLink5p	Module Receive Link 5, positive
23	mTxLink5n	Module Transmit Link 5, negative	24	mRxLink5n	Module Receive Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.2.7 RSL Type A, Bottom, 4 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mTxLink0p	Module Transmit Link 0, positive	2	mRxLink0p	Module Receive Link 0, positive
3	mTxLink0n	Module Transmit Link 0, negative	4	mRxLink0n	Module Receive Link 0, negative
5	mTxLink1p	Module Transmit Link 1, positive	6	mRxLink1p	Module Receive Link 1, positive
7	mTxLink1n	Module Transmit Link 1, negative	8	mRxLink1n	Module Receive Link 1, negative
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.2.8 RSL Type B, Bottom, 4 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mRxLink0p	Module Receive Link 0, positive	2	mTxLink0p	Module Transmit Link 0, positive
3	mRxLink0n	Module Receive Link 0, negative	4	mTxLink0n	Module Transmit Link 0, negative
5	mRxLink1p	Module Receive Link 1, positive	6	mTxLink1p	Module Transmit Link 1, positive
7	mRxLink1n	Module Receive Link 1, negative	8	mTxLink1n	Module Transmit Link 1, negative
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.2.9 RSL Type A, Bottom, 8 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mTxLink0p	Module Transmit Link 0, positive	2	mRxLink0p	Module Receive Link 0, positive
3	mTxLink0n	Module Transmit Link 0, negative	4	mRxLink0n	Module Receive Link 0, negative
5	mTxLink1p	Module Transmit Link 1, positive	6	mRxLink1p	Module Receive Link 1, positive
7	mTxLink1n	Module Transmit Link 1, negative	8	mRxLink1n	Module Receive Link 1, negative
9	mTxLink2p	Module Transmit Link 2, positive	10	mRxLink2p	Module Receive Link 2, positive
11	mTxLink2n	Module Transmit Link 2, negative	12	mRxLink2n	Module Receive Link 2, negative
13	mTxLink3p	Module Transmit Link 3, positive	14	mRxLink3p	Module Receive Link 3, positive
15	mTxLink3n	Module Transmit Link 3, negative	16	mRxLink3n	Module Receive Link 3, negative
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.2.10 RSL Type B, Bottom, 8 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mxLink0p	Module Receive Link 0, positive	2	mxLink0p	Module Transmit Link 0, positive
3	mxLink0n	Module Receive Link 0, negative	4	mxLink0n	Module Transmit Link 0, negative
5	mxLink1p	Module Receive Link 1, positive	6	mxLink1p	Module Transmit Link 1, positive
7	mxLink1n	Module Receive Link 1, negative	8	mxLink1n	Module Transmit Link 1, negative
9	mxLink2p	Module Receive Link 2, positive	10	mxLink2p	Module Transmit Link 2, positive
11	mxLink2n	Module Receive Link 2, negative	12	mxLink2n	Module Transmit Link 2, negative
13	mxLink3p	Module Receive Link 3, positive	14	mxLink3p	Module Transmit Link 3, positive
15	mxLink3n	Module Receive Link 3, negative	16	mxLink3n	Module Transmit Link 3, negative
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.2.11 RSL Type A, Bottom, 12 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mTxLink0p	Module Transmit Link 0, positive	2	mRxLink0p	Module Receive Link 0, positive
3	mTxLink0n	Module Transmit Link 0, negative	4	mRxLink0n	Module Receive Link 0, negative
5	mTxLink1p	Module Transmit Link 1, positive	6	mRxLink1p	Module Receive Link 1, positive
7	mTxLink1n	Module Transmit Link 1, negative	8	mRxLink1n	Module Receive Link 1, negative
9	mTxLink2p	Module Transmit Link 2, positive	10	mRxLink2p	Module Receive Link 2, positive
11	mTxLink2n	Module Transmit Link 2, negative	12	mRxLink2n	Module Receive Link 2, negative
13	mTxLink3p	Module Transmit Link 3, positive	14	mRxLink3p	Module Receive Link 3, positive
15	mTxLink3n	Module Transmit Link 3, negative	16	mRxLink3n	Module Receive Link 3, negative
17	mTxLink4p	Module Transmit Link 4, positive	18	mRxLink4p	Module Receive Link 4, positive
19	mTxLink4n	Module Transmit Link 4, negative	20	mRxLink4n	Module Receive Link 4, negative
21	mTxLink5p	Module Transmit Link 5, positive	22	mRxLink5p	Module Receive Link 5, positive
23	mTxLink5n	Module Transmit Link 5, negative	24	mRxLink5n	Module Receive Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.2.12 RSL Type B, Bottom, 12 Links, TIM

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	mRxLink0p	Receive Link 0, positive	2	mTxLink0p	Transmit Link 0, positive
3	mRxLink0n	Receive Link 0, negative	4	mTxLink0n	Transmit Link 0, negative
5	mRxLink1p	Receive Link 1, positive	6	mTxLink1p	Transmit Link 1, positive
7	mRxLink1n	Receive Link 1, negative	8	mTxLink1n	Transmit Link 1, negative
9	mRxLink2p	Receive Link 2, positive	10	mTxLink2p	Transmit Link 2, positive
11	mRxLink2n	Receive Link 2, negative	12	mTxLink2n	Transmit Link 2, negative
13	mRxLink3p	Receive Link 3, positive	14	mTxLink3p	Transmit Link 3, positive
15	mRxLink3n	Receive Link 3, negative	16	mTxLink3n	Transmit Link 3, negative
17	mRxLink4p	Receive Link 4, positive	18	mTxLink4p	Transmit Link 4, positive
19	mRxLink4n	Receive Link 4, negative	20	mTxLink4n	Transmit Link 4, negative
21	mRxLink5p	Receive Link 5, positive	22	mTxLink5p	Transmit Link 5, positive
23	mRxLink5n	Receive Link 5, negative	24	mTxLink5n	Transmit Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.3 Carrier

Care should be taken with the assignment of pin names on all carriers to ensure that the Tx and Rx pairs on the carrier match that of the TIM module. The signal assignments on the TIM module is confusing as the same type of connector is used for the RSL Type A signals on the Top and the Bottom of the module, but with different signal assignments give to pin one on both connectors. The reason for this strange pin assignment is to easy the routing of the differential pairs on the TIM modules. Extreme care should be taken when routing the RSL links as all stubs and vias should be minimized. This topic is further discussed in the '*Electrical Specifications*' section in this document. The reasoning behind the signal assignments on the TIM module is illustrated in the following diagram:

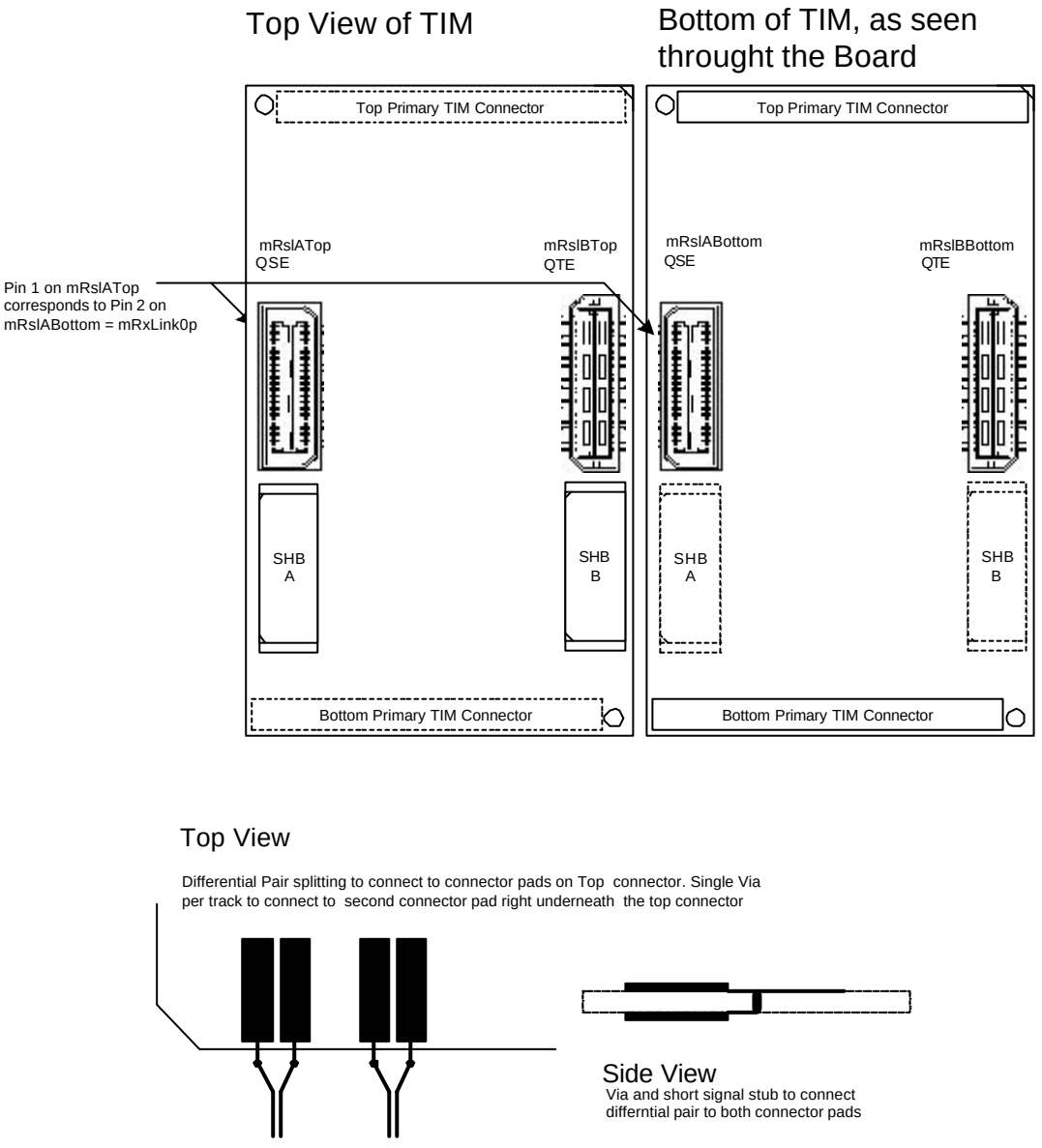

Figure 14 – Top and Bottom RSL Connector on TIM Module

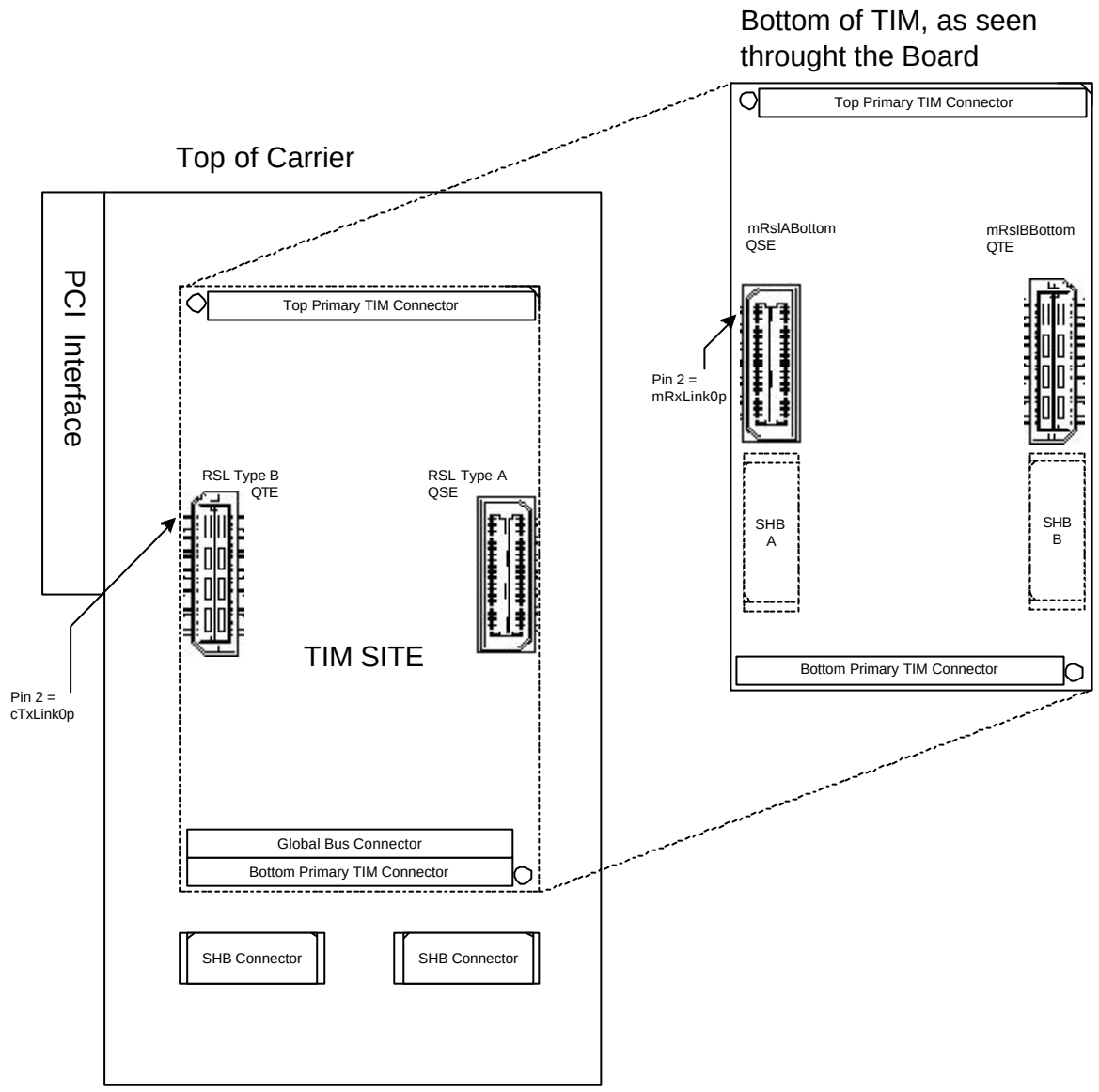

Figure 15 – RSL Connection between TIM Module and Carrier

The above figure illustrates how the Bottom RSL Type A and Type B connectors connect to the RSL connectors on the Carrier. Pin 1 on the RSL Type A connector on the Bottom of the TIM module is mTxLink0p. This connects to pin 1 on the RSL Type B connector on the carrier – cRxLink0p. Pin 2 on the module, mRxLink0p, connects to cTxLink0p on the carrier. The full lists of RSL Type A and RSL Type B connectors for carriers follow in the tables underneath.

2.4.3.1 RSL Type A, 4 Links, Carrier

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	cTxLink0p	Carrier Transmit Link 0, positive	2	cRxLink0p	Carrier Receive Link 0, positive
3	cTxLink0n	Carrier Transmit Link 0, negative	4	cxLink0n	Carrier Receive Link 0, negative
5	cTxLink1p	Carrier Transmit Link 1, positive	6	cxLink1p	Carrier Receive Link 1, positive
7	cTxLink1n	Carrier Transmit Link 1, negative	8	cxLink1n	Carrier Receive Link 1, negative
9	cTxLink2p	Carrier Transmit Link 2, positive	10	cxLink2p	Carrier Receive Link 2, positive
11	cTxLink2n	Carrier Transmit Link 2, negative	12	cxLink2n	Carrier Receive Link 2, negative
13	cTxLink3p	Carrier Transmit Link 3, positive	14	cxLink3p	Carrier Receive Link 3, positive
15	cTxLink3n	Carrier Transmit Link 3, negative	16	cxLink3n	Carrier Receive Link 3, negative
17	cTxLink4p	Carrier Transmit Link 4, positive	18	cxLink4p	Carrier Receive Link 4, positive
19	cTxLink4n	Carrier Transmit Link 4, negative	20	cxLink4n	Carrier Receive Link 4, negative
21	cTxLink5p	Carrier Transmit Link 5, positive	22	cxLink5p	Carrier Receive Link 5, positive
23	cTxLink5n	Carrier Transmit Link 5, negative	24	cxLink5n	Carrier Receive Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.3.2 RSL Type B, 4 Links, Carrier

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	cRxLink0p	Carrier Receive Link 0, positive	2	cTxLink0p	Carrier Transmit Link 0, positive
3	cRxLink0n	Carrier Receive Link 0, negative	4	cTxLink0n	Carrier Transmit Link 0, negative
5	cRxLink1p	Carrier Receive Link 1, positive	6	cTxLink1p	Carrier Transmit Link 1, positive
7	cRxLink1n	Carrier Receive Link 1, negative	8	cTxLink1n	Carrier Transmit Link 1, negative
9	Reserved	Reserved	10	Reserved	Reserved
11	Reserved	Reserved	12	Reserved	Reserved
13	Reserved	Reserved	14	Reserved	Reserved
15	Reserved	Reserved	16	Reserved	Reserved
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.3.3 RSL Type A, 8 Links, Carrier

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	cTxLink0p	Carrier Transmit Link 0, positive	2	cRxLink0p	Carrier Receive Link 0, positive
3	cTxLink0n	Carrier Transmit Link 0, negative	4	cxLink0n	Carrier Receive Link 0, negative
5	cTxLink1p	Carrier Transmit Link 1, positive	6	cxLink1p	Carrier Receive Link 1, positive
7	cTxLink1n	Carrier Transmit Link 1, negative	8	cxLink1n	Carrier Receive Link 1, negative
9	cTxLink2p	Carrier Transmit Link 2, positive	10	cxLink2p	Carrier Receive Link 2, positive
11	cTxLink2n	Carrier Transmit Link 2, negative	12	cxLink2n	Carrier Receive Link 2, negative
13	cTxLink3p	Carrier Transmit Link 3, positive	14	cxLink3p	Carrier Receive Link 3, positive
15	cTxLink3n	Carrier Transmit Link 3, negative	16	cxLink3n	Carrier Receive Link 3, negative
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.3.4 RSL Type B, 8 Links, Carrier

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	cRxLink0p	Carrier Receive Link 0, positive	2	cTxLink0p	Carrier Transmit Link 0, positive
3	cRxLink0n	Carrier Receive Link 0, negative	4	cTxLink0n	Carrier Transmit Link 0, negative
5	cRxLink1p	Carrier Receive Link 1, positive	6	cTxLink1p	Carrier Transmit Link 1, positive
7	cRxLink1n	Carrier Receive Link 1, negative	8	cTxLink1n	Carrier Transmit Link 1, negative
9	cRxLink2p	Carrier Receive Link 2, positive	10	cTxLink2p	Carrier Transmit Link 2, positive
11	cRxLink2n	Carrier Receive Link 2, negative	12	cTxLink2n	Carrier Transmit Link 2, negative
13	cRxLink3p	Carrier Receive Link 3, positive	14	cTxLink3p	Carrier Transmit Link 3, positive
15	cRxLink3n	Carrier Receive Link 3, negative	16	cTxLink3n	Carrier Transmit Link 3, negative
17	Reserved	Reserved	18	Reserved	Reserved
19	Reserved	Reserved	20	Reserved	Reserved
21	Reserved	Reserved	22	Reserved	Reserved
23	Reserved	Reserved	24	Reserved	Reserved
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.3.5 RSL Type A, 12 Links, Carrier

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	cTxLink0p	Carrier Transmit Link 0, positive	2	cRxLink0p	Carrier Receive Link 0, positive
3	cTxLink0n	Carrier Transmit Link 0, negative	4	cxLink0n	Carrier Receive Link 0, negative
5	cTxLink1p	Carrier Transmit Link 1, positive	6	cxLink1p	Carrier Receive Link 1, positive
7	cTxLink1n	Carrier Transmit Link 1, negative	8	cxLink1n	Carrier Receive Link 1, negative
9	cTxLink2p	Carrier Transmit Link 2, positive	10	cxLink2p	Carrier Receive Link 2, positive
11	cTxLink2n	Carrier Transmit Link 2, negative	12	cxLink2n	Carrier Receive Link 2, negative
13	cTxLink3p	Carrier Transmit Link 3, positive	14	cxLink3p	Carrier Receive Link 3, positive
15	cTxLink3n	Carrier Transmit Link 3, negative	16	cxLink3n	Carrier Receive Link 3, negative
17	cTxLink4p	Carrier Transmit Link 4, positive	18	cxLink4p	Carrier Receive Link 4, positive
19	cTxLink4n	Carrier Transmit Link 4, negative	20	cxLink4n	Carrier Receive Link 4, negative
21	cTxLink5p	Carrier Transmit Link 5, positive	22	cxLink5p	Carrier Receive Link 5, positive
23	cTxLink5n	Carrier Transmit Link 5, negative	24	cxLink5n	Carrier Receive Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.3.6 RSL Type B, 12 Links, Carrier

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	cRxLink0p	Carrier Receive Link 0, positive	2	cTxLink0p	Carrier Transmit Link 0, positive
3	cRxLink0n	Carrier Receive Link 0, negative	4	cTxLink0n	Carrier Transmit Link 0, negative
5	cRxLink1p	Carrier Receive Link 1, positive	6	cTxLink1p	Carrier Transmit Link 1, positive
7	cRxLink1n	Carrier Receive Link 1, negative	8	cTxLink1n	Carrier Transmit Link 1, negative
9	cRxLink2p	Carrier Receive Link 2, positive	10	cTxLink2p	Carrier Transmit Link 2, positive
11	cRxLink2n	Carrier Receive Link 2, negative	12	cTxLink2n	Carrier Transmit Link 2, negative
13	cRxLink3p	Carrier Receive Link 3, positive	14	cTxLink3p	Carrier Transmit Link 3, positive
15	cRxLink3n	Carrier Receive Link 3, negative	16	cTxLink3n	Carrier Transmit Link 3, negative
17	cRxLink4p	Carrier Receive Link 4, positive	18	cTxLink4p	Carrier Transmit Link 4, positive
19	cRxLink4n	Carrier Receive Link 4, negative	20	cTxLink4n	Carrier Transmit Link 4, negative
21	cRxLink5p	Carrier Receive Link 5, positive	22	cTxLink5p	Carrier Transmit Link 5, positive
23	cRxLink5n	Carrier Receive Link 5, negative	24	cTxLink5n	Carrier Transmit Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.4 Rigid PCB and RSL Cable

The purpose of the rigid PCB is to connect the RSL links of two adjacent TIM modules to each other. When two TIM modules are placed next to each other one Top RSL Type A and one Top RSL Type B connector is right next to each other. The reasoning behind the pin assignments is illustrated in the following diagram:

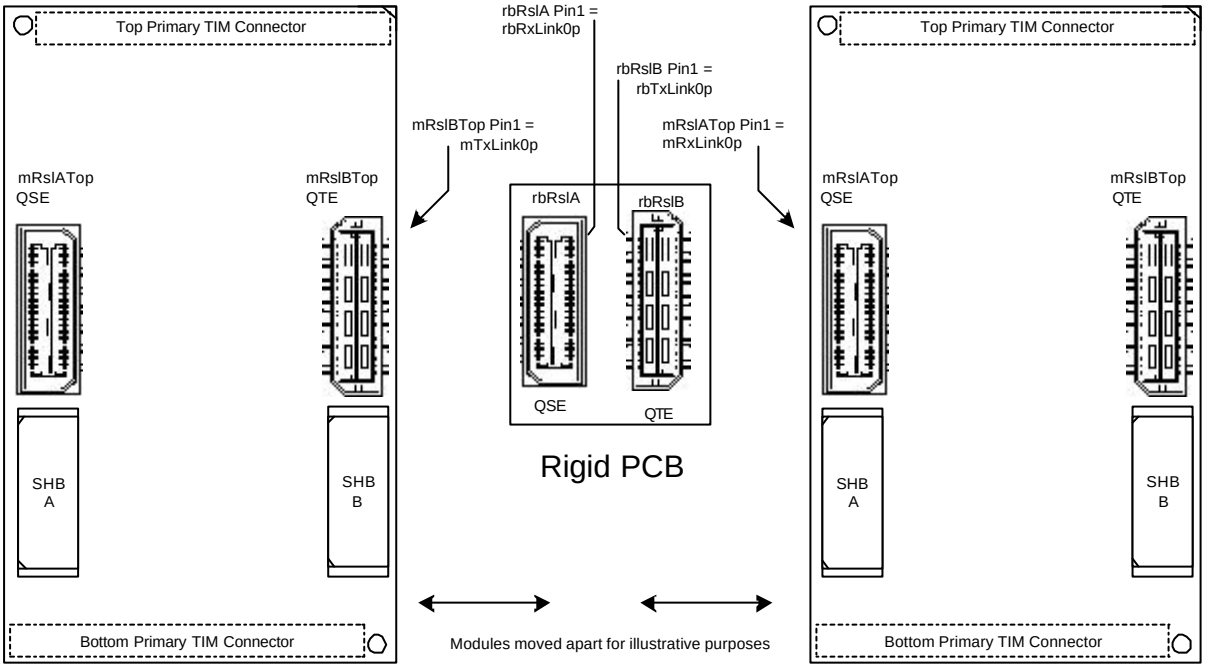

Figure 16 – Rigid PCB Pin Assignments

On the TIM Module RSL Type B connector pin 1, mRSLBTop, is mTxLink0p. This signal connects to a RSL Type A connector on the Rigid PCB, called rbRxLink0p. Similarly mRxLink0p on the TIM Module RSL Type A connector connects to rbTxLink0p on the rigid PCB. The signals on the rigid PCB map 1-to-1 to each other. Thus rbRxLink0p connects straight to rbTxLink0p.

The RSL interconnecting cable serves the same purpose of the rigid PCB, with the exception that it can interconnect modules that are not adjacent to each other. The signal allocations on the connector pins are the same and the cable also maps one to one. The only difference between the Rigid PCB and the Interconnecting Cable is the prefix assigned to the signal names. The Rigid PCB signals use 'rb' as a prefix and the Interconnecting Cable uses 'ic' as a prefix. No distinction is made between four, eight or twelve links as all the links are interconnected on both the PCB and the cable. Note that six (total of 12 over two connectors) of the possible seven links per connector are connected over the PCB. The seventh link is left as reserved like on all the other connectors. The seventh link is however connected on the inter-connecting cable. The signal assignments for the RSL connectors on the Rigid PCB and the Interconnecting Cable follows.

2.4.4.1 RSL Type A, Top, Rigid PCB

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	rbRxLink0p	RPCB Receive Link 0, positive	2	rbTxLink0p	RPCB Transmit Link 0, positive
3	RxLink0n	RPCB Receive Link 0, negative	4	rbTxLink0n	RPCB Transmit Link 0, negative
5	rbRxLink1p	RPCB Receive Link 1, positive	6	rbTxLink1p	RPCB Transmit Link 1, positive
7	rbRxLink1n	RPCB Receive Link 1, negative	8	rbTxLink1n	RPCB Transmit Link 1, negative
9	rbRxLink2p	RPCB Receive Link 2, positive	10	rbTxLink2p	RPCB Transmit Link 2, positive
11	rbRxLink2n	RPCB Receive Link 2, negative	12	rbTxLink2n	RPCB Transmit Link 2, negative
13	rbRxLink3p	RPCB Receive Link 3, positive	14	rbTxLink3p	RPCB Transmit Link 3, positive
15	rbRxLink3n	RPCB Receive Link 3, negative	16	rbTxLink3n	RPCB Transmit Link 3, negative
17	rbRxLink4p	RPCB Receive Link 4, positive	18	rbTxLink4p	RPCB Transmit Link 4, positive
19	rbRxLink4n	RPCB Receive Link 4, negative	20	rbTxLink4n	RPCB Transmit Link 4, negative
21	rbRxLink5p	RPCB Receive Link 5, positive	22	rbTxLink5p	RPCB Transmit Link 5, positive
23	rbRxLink5n	RPCB Receive Link 5, negative	24	rbTxLink5n	RPCB Transmit Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.4.2 RSL Type B, Top, Rigid PCB

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	rbTxLink0p	RPCB Transmit Link 0, positive	2	rbRxLink0p	RPCB Receive Link 0, positive
3	rbTxLink0n	RPCB Transmit Link 0, negative	4	rbRxLink0n	RPCB Receive Link 0, negative
5	rbTxLink1p	RPCB Transmit Link 1, positive	6	rbRxLink1p	RPCB Receive Link 1, positive
7	rbTxLink1n	RPCB Transmit Link 1, negative	8	rbRxLink1n	RPCB Receive Link 1, negative
9	rbTxLink2p	RPCB Transmit Link 2, positive	10	rbRxLink2p	RPCB Receive Link 2, positive
11	rbTxLink2n	RPCB Transmit Link 2, negative	12	rbRxLink2n	RPCB Receive Link 2, negative
13	rbTxLink3p	RPCB Transmit Link 3, positive	14	rbRxLink3p	RPCB Receive Link 3, positive
15	rbTxLink3n	RPCB Transmit Link 3, negative	16	rbRxLink3n	RPCB Receive Link 3, negative
17	rbTxLink4p	RPCB Transmit Link 4, positive	18	rbRxLink4p	RPCB Receive Link 4, positive
19	rbTxLink4n	RPCB Transmit Link 4, negative	20	rbRxLink4n	RPCB Receive Link 4, negative
21	rbTxLink5p	RPCB Transmit Link 5, positive	22	rbRxLink5p	RPCB Receive Link 5, positive
23	rbTxLink5n	RPCB Transmit Link 5, negative	24	rbRxLink5n	RPCB Receive Link 5, negative
25	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	28	Reserved	Reserved

2.4.4.3 RSL Type A, Top, Inter-connecting Cable

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	icRxLink0p	Cable Receive Link 0, positive	2	icTxLink0p	Cable Transmit Link 0, positive
3	icRxLink0n	Cable Receive Link 0, negative	4	icTxLink0n	Cable Transmit Link 0, negative
5	icRxLink1p	Cable Receive Link 1, positive	6	icTxLink1p	Cable Transmit Link 1, positive
7	icRxLink1n	Cable Receive Link 1, negative	8	icTxLink1n	Cable Transmit Link 1, negative
9	icRxLink2p	Cable Receive Link 2, positive	10	icTxLink2p	Cable Transmit Link 2, positive
11	icRxLink2n	Cable Receive Link 2, negative	12	icTxLink2n	Cable Transmit Link 2, negative
13	icRxLink3p	Cable Receive Link 3, positive	14	icTxLink3p	Cable Transmit Link 3, positive
15	icRxLink3n	Cable Receive Link 3, negative	16	icTxLink3n	Cable Transmit Link 3, negative
17	icRxLink4p	Cable Receive Link 4, positive	18	icTxLink4p	Cable Transmit Link 4, positive
19	icRxLink4n	Cable Receive Link 4, negative	20	icTxLink4n	Cable Transmit Link 4, negative
21	icRxLink5p	Cable Receive Link 5, positive	22	icTxLink5p	Cable Transmit Link 5, positive
23	icRxLink5n	Cable Receive Link 5, negative	24	icTxLink5n	Cable Transmit Link 5, negative
25	icRxLink6p	Cable Receive Link 6, positive	26	icTxLink6p	Cable Transmit Link 6, positive
27	icRxLink6n	Cable Receive Link 6, negative	28	icTxLink6n	Cable Transmit Link 6, negative

2.4.4.4 RSL Type B, Top, Inter-connecting Cable

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	icTxLink0p	Cable Transmit Link 0, positive	2	icRxLink0p	Cable Receive Link 0, positive
3	icTxLink0n	Cable Transmit Link 0, negative	4	icRxLink0n	Cable Receive Link 0, negative
5	icTxLink1p	Cable Transmit Link 1, positive	6	icRxLink1p	Cable Receive Link 1, positive
7	icTxLink1n	Cable Transmit Link 1, negative	8	icRxLink1n	Cable Receive Link 1, negative
9	icTxLink2p	Cable Transmit Link 2, positive	10	icRxLink2p	Cable Receive Link 2, positive
11	icTxLink2n	Cable Transmit Link 2, negative	12	icRxLink2n	Cable Receive Link 2, negative
13	icTxLink3p	Cable Transmit Link 3, positive	14	icRxLink3p	Cable Receive Link 3, positive
15	icTxLink3n	Cable Transmit Link 3, negative	16	icRxLink3n	Cable Receive Link 3, negative
17	icTxLink4p	Cable Transmit Link 4, positive	18	icRxLink4p	Cable Receive Link 4, positive
19	icTxLink4n	Cable Transmit Link 4, negative	20	icRxLink4n	Cable Receive Link 4, negative
21	icTxLink5p	Cable Transmit Link 5, positive	22	icRxLink5p	Cable Receive Link 5, positive
23	icTxLink5n	Cable Transmit Link 5, negative	24	icRxLink5n	Cable Receive Link 5, negative
25	icTxLink6p	Cable Transmit Link 6, positive	26	icRxLink6p	Cable Receive Link 6, positive
27	icTxLink6n	Cable Transmit Link 6, negative	28	icRxLink6n	Cable Receive Link 6, negative

3 Xilinx Multi-gigabit Transceivers

The RSL interconnection architecture is based on the RocketIO (or Multi-Gigabit) transceivers found in Xilinx Virtex-II Pro FPGAs. This section is intended as a quick introduction to these transceiver cores. For more detailed information refer to the Xilinx documentation listed at the start of this document.

The RocketIO transceivers are very generic. For this reason certain firmware and hardware limitations may be imposed on their functionality to simplify interconnection. These restrictions will be taken note of in this section. The user should take special note of these limitations when design their own custom hardware to interface with Sundance RSL compliant hardware. A typical example of one of these limitations is operating frequency of the RSL link. Even though the RocketIO transceiver may operate anywhere in the range of 0.622 to 3.125 GBits/s the RSL operating frequency is fixed at 3.125GBit/s[1] *(Still to be confirmed by hardware characterization)*

Some of the information in this section was copied straight from [1] and [2] and is copyrighted to Xilinx. These sections are respectively noted in the text by having an *[A]* or [B] accompanying the text.

3.1 Supported Devices

Currently only the Xilinx Virtex-II Pro FPGAs support RocketIO. These RocketIO transceivers are integrated into the silicon of the FPGA. It is not a 'soft core.' The following table lists the supported devices and the amount of links per device:

Device	RocketIO Cores		Device	RocketIO Cores
XC2VP2	4		XC2VP40	0 or 12
XC2VP4	4		XC2VP50	0 or 16
XC2VP7	8		XC2VP70	20
XC2VP20	8		XC2VP100	0 or 20
XC2VP30	8		XC2VP125	0, 20 or 24

Figure 17 – Xilinx Devices Supporting RocketIO

The RocketIO core is highly generic. It is possible to interface this core to many third party manufacturers silicon. The user should carefully compare the electrical specifications of the Xilinx Virtex-II Pro (found in the appropriate Xilinx datasheet listed in the references at the start of this document) and of the device to interface to. Additional hardware in the form of termination, level conversion or isolation might be required.

3.2 RocketIO Features[B]

The RocketIO transceiver's flexible, programmable features allow a multi-gigabit serial transceiver to be easily integrated into any Virtex-II Pro design:

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[1] The effective data throughput is given as 2.5GBit/s at the start of this document under *RSL Features*. Yet the link speed is given as 3.125GBit/s here. This 'discontinuity' is explained in the *Reference Clock* section further on in this document.

- Variable-speed, full-duplex transceiver, allowing 600 Mbps to 3.125 Gbps baud transfer rates
- Monolithic clock synthesis and clock recovery system, eliminating the need for external components
- Automatic lock-to-reference function
- Five levels of programmable serial output differential swing (800 mV to 1600 mV peak-peak), allowing compatibility with other serial system voltage levels
- Four levels of programmable pre-emphasis
- AC and DC coupling
- Programmable 50?/75? on-chip termination, eliminating the need for external termination resistors
- Serial and parallel TX-to-RX internal loopback modes for testing operability
- Programmable comma detection to allow for any protocol and detection of any 10-bit character.

3.3 The Xilinx MGT Core

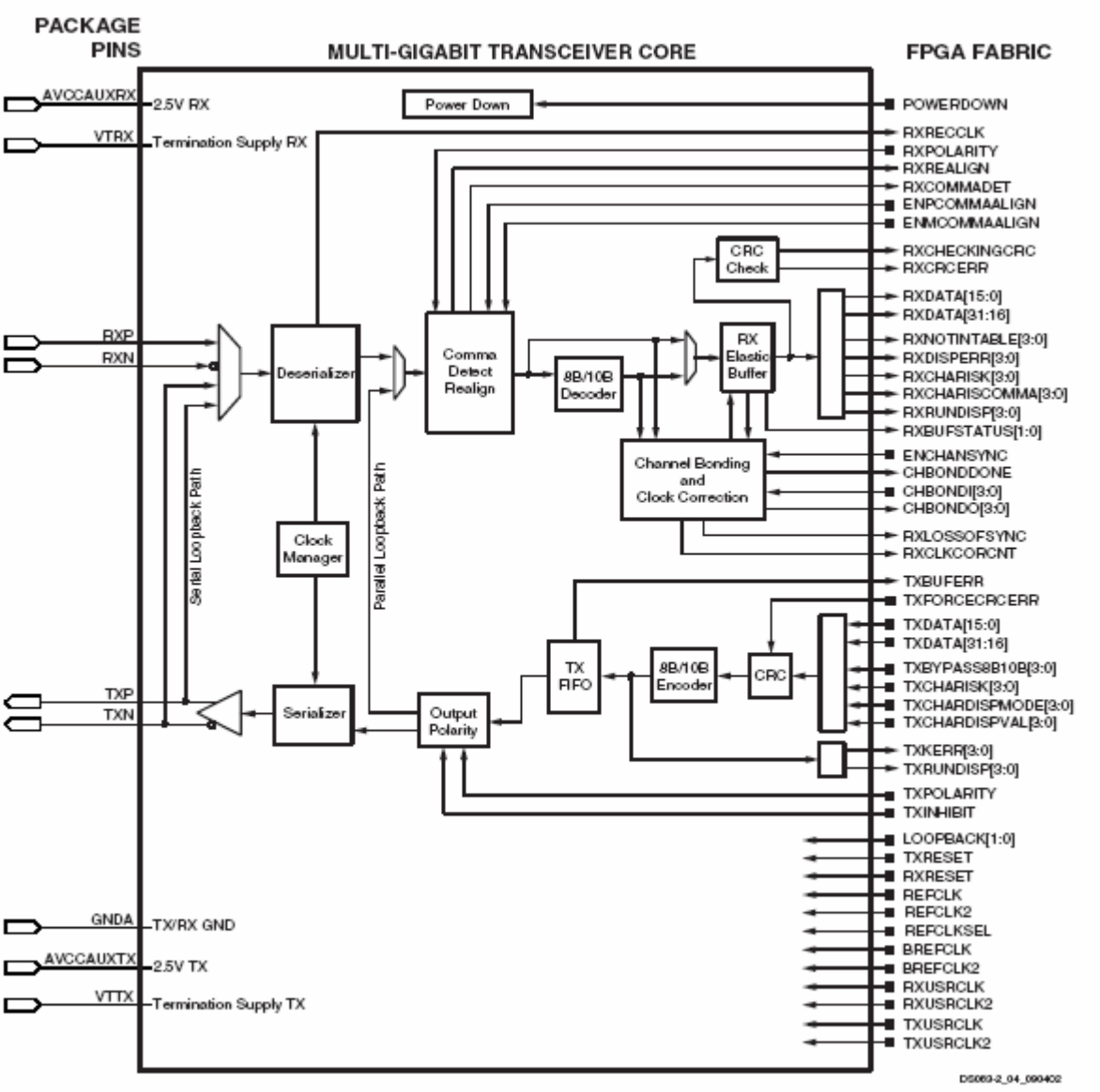

Figure 18 – The Xilinx Multi-Gigabit Transceiver Core[B]

3.3.1 Clock Synthesizer[A]

Synchronous serial data reception is facilitated by a clock/data recovery circuit. This circuit uses a fully monolithic Phase Lock Loop (PLL), which does not require any external components. The clock/data recovery circuit extracts both phase and frequency from the incoming data stream. The recovered clock is presented on output RXRECCLK at 1/20 of the serial received data rate.
The gigabit transceiver multiplies the reference frequency provided on the reference clock input (REFCLK) by 20. The multiplication of the clock is achieved by using a fully monolithic PLL that does not require any external components.

3.3.2 Clock and Data Recovery[A]

The clock/data recovery (CDR) circuits will lock to the reference clock automatically if the data is not present. For proper operation, the frequency of the reference clock must be within ±100 ppm of the nominal frequency.

3.3.3 FPGA Transmit Interface[B]

The FPGA can send either one, two, or four characters of data to the transmitter. Each character can be either 8 bits or 10 bits wide. If 8-bit data is applied, the additional inputs become control signals for the 8B/10B encoder.

3.3.4 8B/10B Encoder[A],2

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters that are used for Gigabit Ethernet, Fibre Channel, and InfiniBand. The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10 bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

3.3.5 Transmit FIFO[A]

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

3.3.6 Serializer[A]

The multi-gigabit transceiver multiplies the reference frequency provided on the reference clock input (REFCLK) by 20. Clock multiplication is achieved by using a fully monolithic
PLL requiring no external components. Data is converted from parallel to serial format and transmitted on the TXP and TXN differential outputs.

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[2] The 8B to 10B encoder ensures that the data stream is always DC balanced (same amount of 1s as 0s). This is required by the PLL to lock onto and maintain lock on the data stream. 8B/10B encoding contains the encoded data, but you can also include control characters into the data stream that is uniquely identifiable. These control characters are referred to as K characters and are used to indicate the start of a data pack, the end of a data packet and control commands for re-syncing, reset, etc

3.3.7 Transmit Termination[A]

On-chip termination is provided at the transmitter, eliminating the need for external termination. Programmable options exist for 50? (default) and 75? termination

3.3.8 Pre-Emphasis and Swing Control[A]

Four selectable levels of pre-emphasis (10% [default], 20%, 25%, and 33%) are available. Optimizing this setting allows the transceiver to drive various distances of PCB or cable at the maximum baud rate. The programmable output swing control can adjust the differential output level between 400 mV and 800 mV in four increments of 100 mV.

3.3.9 Deserializer[A]

The RocketIO transceiver accepts serial differential data on its RXP and RXN inputs. The clock/data recovery circuit extracts the clock and retimes incoming data to this clock. It uses a fully monolithic PLL requiring no external components. The clock/data recovery circuitry extracts both phase and frequency from the incoming data stream. The recovered clock is presented on output RXRECCLK at 1/20 of the received serial data rate.

3.3.10 Comma Detect[A]

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indication is given at the receiver interface. The realignment indicator is a distinct output. The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma–, both, or a unique user-defined and programmed sequence.

3.3.11 Receive Termination[A]

On-chip termination is provided at the receiver, eliminating the need for external termination. The receiver includes programmable on-chip termination circuitry for 50 ? (default) or 75 ? impedance.

3.3.12 8B/10B Decoder[A]

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both “disparity errors” and “out-of-band” errors.

3.3.13 Receive Buffer[A]

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

3.3.14 Transmit Buffer[A]

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency- locked.

3.3.15 CRC[A]

The RocketIO transceiver CRC logic supports the 32-bit invariant CRC calculation used by Infiniband, FibreChannel, and Gigabit Ethernet.

3.4 Reference Clock

The External Reference Clock must be 1/20th the frequency of the desired data rate of the serial link. For 3.125GBit/s operation a reference clock of 156.25MHz is required. For a serial data rate of 2.5BGit/s an external clock of 125MHz is required.

When data is transmitted by the RSL link it is 8B/10B encoded. The effective data throughput of the link is thus only 8/10. If the link is running at 3.125GBit/s the effective data throughput is only 2.5GBit/s. If the link is running at 2.5GBit/s the effective data rate is 2GBit/s.

3.5 RSL Specific Implementations

3.5.1 VHDL Instantiation

The RSL VHDL interface instantiates a subset of the RocketIO transceiver. Some of the default settings are as follows:

- FPGA Transmit Interface: Two character wide interface
- Transmit FIFO: Enabled
- 8B/10B Encoder: Enabled
- Transmit Termination: 50 Ohm
- Pre-Emphasis: 10%
- Swing Control: 400mV
- 8B/10B Decoder: Enabled
- Receive Termination: Enabled
- CRC: Enabled

3.5.2 Hardware implementation

The following hardware implementation is followed by the RSL implementation:

- External Reference Clock: 156.25MHz
- AC/DC Coupling: DC Coupling

4 Electrical Specifications

This section is still outstanding, but will include information on the points mentioned underneath, and on some additional topics not yet listed.

4.1 Signaling Level

4.2 PCB Design Consideration

4.2.1 Routing of differential pairs

4.2.2 Example PCB Layer Stack

5 Generic VHDL Building Blocks

This section is still TBD, but will contain a description of a standard VHDL implementation used to interface to the RocketIO transceivers. From the User's perspective he will only see some type of Memory interface. When he writes data to the memory the VHDL core will take care of delivering the data to the RSL interface and ensuring the safe delivery of the data at the destination. In the same way the VHDL core will take care of all incoming data and place it in a memory type interface for the user to read.

6 Appendix A: Sundance RSL Compliant Modules

The following table list some of the specifications of the Sundance modules that have RSL interfaces. For an updated list please refer to the Sundance website.

No	SMT No	Type	Mounted Devices	Description	RSL Links
1	SMT398-VP7	TIM Module	XC2VP7-6FF896C	Expandable base module with 1GBit DDR SDRAM Memory	8
2	SMT398-VP20	TIM Module	XC2VP20-6FF896C	Expandable base module with 1GBit DDR SDRAM Memory	8
3	SMT398-VP30	TIM Module	XC2VP30-6FF896C	Expandable base module with 1GBit DDR SDRAM Memory	8