Software Defined Radio Development Station (SDR-DS)
Development SDR Hardware

The SDR Development Station
- Host, Baseband, IF hardware - Expandable
- RF Front End Module - Optional
- MathWorks™ Model based software development environment - Optional
- Celoxica’s ESL software - Optional
- Diamond FPGA/DSP RTOS
- Board Support Package (Drivers and API)
- Demo Application
- SCA framework - Optional
- ORB Middleware - Optional
- Documentation

Customers Can:
- Prototype wireless communication systems, 4G and beyond, like 2x2 MIMO data-protocols.
- Develop libraries/software solutions on the DSP
- Implement Down/Up Converters in the FPGA
- Benchmark performance of protocol functions on FPGA and DSP and optimize system design based on cost, size and power
- Source and reuse H/W and S/W IP available from different vendors
- Develop bespoke/custom IF and RF modules to interface to the DSP + FPGA based baseband module
- SCA compliant waveform implementation

From - $9995
Availability – Dec. 06
SDR-DS – Software Architecture

Hardware Task Based Design

Software Task Based Design

VHDL

Diamond FPGA 3L

Diamond DSP 3L

ISE XILINX

Traditional Flow

Code Composer Studio TI

Platform Abstractions & Communication Links

FPGA

DSP

Single multi-tasks application

Configuration file
**Baseband Processing Module**

- **Texas Instruments DSP**
  - TM320DC6416T – 1GHz
  - 133MHz External EMIF

- **Xilinx Virtex-II PRO FPGA**
  - XC2VP30-6
  - Bandwidth FPGA <> DSP
    - Excess of 500MBytes/s
  - 2x PowerPC CPU Cores
  - Serial Rocket I/O
    - Serial Rapid I/O compatible

- **256MBytes of SDRAM**
  - Running at full 133MHz @ 64-bit

- **8MBytes of Flash Memory**
  - Stand-alone application/booting

- **Integrated XDS510-JTAG controller**
  - Enables debug by CCS

- **Scalable, Modular concept**
  - More FPGA or DSP Modules can be added, replaced or upgraded

- **Stand-alone form factor**
  - Only require Power

- **Details of SMT395 DSP/FPGA Module**
Intermediate Frequency Module

Specifications:
- Virtex-4 FPGA, SX35 as default
- Based on Texas Instrument Module (TIM) Interface
- 2 x TI ADC @ 125MSPS (14 bits)
- 2 x TI DAC @ 500MSPS (16 bits)
- On-Board VCO & Crystal & External Ports Clock Circuitry
- Upgradeable to fast converters with a simple daughter Module as defined in the Sundance SLB standard.
- Details of SMT350 ADC/DAC Daughter-Module
- Details of SMT368 FPGA-Base Module
Radio Frequency Module

Specifications:

- Virtex-2 FPGA, ZBT-SRAM
- Input signals are filtered by 1st IF tuned to 70MHz ± 8MHz,
- RF output signal is in the 2.4–2.5 GHz ISM band,
- RF input signal is in the 2.4–2.5 GHz ISM band,
- IF output signal is 70MHz ± 8MHz,
- The 70MHz IF is converted to a 2nd IF of 374 MHz.
- Details of SMT349 RF-Module
Board Support Package

- **Diamond DSP** – Real-Time DSP Solution
  - Multi-Core compatible; scalable to infinitive numbers of DSPs
  - Multi-tasking, Multi-threading on a single DSP
  - Addition to TI’s Code Composer Studio *(required!)*
  - Eclipse compatible

- **Diamond FPGA** – Embedded FPGA Tools
  - Integrate DSP + FPGAs into a coherent software model
  - Addition to Xilinx’s ISE tools *(required!)*
  - Eclipse compatible

- **SMT6040** – MathWorks™ Simulink® Toolbox for VHDL
  - Model-based design; demo examples
  - MathWork compatible *(required!)*

- **SMT6041** - Xilinx System Generator ©
  - Block programming design; demo examples
  - Xilinx tools compatible *(required!)*

- **SMT6050** – MathWorks™ Simulink® Toolbox for DSP
  - Model-based design; demo examples
  - MathWork compatible *(required!)*

- **ESL** - Celoxica solution
  - ’C’-based design flow; migrating ‘C’ code to FPGAs
  - Handel ’C’ compatible *(required!)*
System Design Flow

1st Abstraction level

- Diamond FPGA 3L
- Diamond DSP 3L

2nd Abstraction level

- C-Based Design
  - Celoxica DK Suite
- Model-Based Design
  - XILINX SysGen
  - MATLAB/Simulink
- Hardware Task Based Design
- Software Task Based Design

Sundance’s Platform Abstractions & Communication Links